AMI®

1981
MOS Products Catalog

American Microsystems, Inc., the first commercial producer of MOS/LSI beginning in 1966, is a major designer, manufacturer and marketer of circuits for the consumer, EDP and communications markets.

AMI is the leading designer of custom LSI, makes and markets its proprietary S2000 family of 4-bit microcomputers, is a major alternate source for the S6800 8-bit microprocessor family and the only alternate source for the S9900 16-bit family of microprocessors. We also provide development support through the Phoenix series of low-cost universal microprocessor development stations and the ADS advanced development support tools. The Company provides the market with selected 1K and 4K low power CMOS Static RAMs, plus 8K, 16K, 32K and 64K ROMs for all JEDEC pinouts or as EPROM replacements.

The most experienced designer of systems-oriented MOS/LSI communication circuits, AMI provides components for station equipment, PABX and Central Office Switching systems, data communications and advanced signal processing applications.

AMI is pioneering in same-chip integration of digital and analog circuitry, and is a recognized leader in switched capacitor filter technology.

Processing capability includes N-Channel, advanced silicon gate CMOS and the largest production capability available in P-Channel.

Headquartered in Santa Clara, California, AMI has design centers in Santa Clara, Pocatello, Idaho and Swindon, England. Wafer fabricating plants are in Santa Clara and Pocatello, and assembly facilities are in Seoul, Korea and the Philippines.

Field sales offices are located throughout the United States, in Europe and in the Far East. Their listing, plus those of domestic and international representatives and distributors appear on pages B.29 through B.32 of this publication.

AMI

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S3525A/B	—	—	MT-8865(F)	—	—	—

Memory Products

CMOS RAMs

Vendor	256×4	1K×1	1K×4	4K×1
AMI	S5101	S6508	S6514*	S6504*
FUJITSU	—	—	6514/8414	8404
HARRIS	6561	6508	6514	6504
HITACHI	435101	—	4334	4315
INTERSIL	6551	6508	6514	6504
MOTOROLA	145101	146508	—	146504
NATIONAL	74C920	74C929	6514	6504
NEC	5101	6508	444/6514	—
OKI	573	574	5115	—
RCA	5101	1821	1825	5104
SSS	5101	5102	—	—
TOSHIBA	5101	5508	5514	5504

*To Be Announced

BYTE WIDE NMOS ROMs

Vendor	1K×8-24 Pin	2K×8-24 Pin	4K×8-24 Pin	*4K×8-24 Pin	8K×8-24 Pin	8K×8-28 Pin
AMI	S68308	S6831B	S68332	S2333	S68A364	S2364
AMD	AM9208	AM9216	AM9232	AM9233		
EA	EA8308	EA8316	EA8332	EA8333		
FAIRCHILD	F68B308	3516				
FUJITSU					MB8364	
GI			RO3-9332	RO3-9333	RO3-9364	
HITACHI	HN46830		HN462532			
INTEL	2608	2616		(2332)		(2364)
MARUMAN		MIC2316	MIC2332		MIC2364	
MITSUBISHI	M58730		M58333			
MOS		MPS2316	MPS2332		MPS2364	
MOSTEK		MK34000			MK36000	MK37000
MOTOROLA	MCM68308	MCM68316	MCM68332		MCM68364	
NATIONAL		MM52116	MM52132		MM52164	
NEC	PD2308	PD2316	PD2332		PD2364	
NITRON	NC6550					

*Pin compatible with 2732 EPROM

Source: IC Master 1980

Memory Products

BYTE WIDE NMOS ROMs

Vendor	1K×8-24 Pin	2K×8-24 Pin	4K×8-24 Pin	*4K×8-24 Pin	8K×8-24 Pin	8K×8-28 Pin
OKI PANASONIC ROCKWELL SGS	MSM3770	MSM3870 RO3-9316 M2316	MN2332			
SIEMENS SIGNETICS SMC SYNERTEK	2608	SAB8316 2616 SY2316	SAB8332 2632 ROM4732 SY2332	 SY2333	 2664 SY2364	
TI TOSHIBA		 TMM334	TMS4732 TMM333		TMS4764 	 TMM2364

*Pin compatible with 2732 EPROM

Source: IC Master 1980

S6800 Family

AMI	Fairchild	General Instruments	Hitachi	Motorola	National	Texas Instruments
S1602	—	AY-3-1014	—	—	MM5303N	TMS6011
S2350	—	—	—	—	—	—
S6800	F6800	—	HD46800	MC6800	—	—
S6801	—	—	—	MC6801	—	—
S6802	F6802	—	HD46802	MC6802	—	—
S6805	—	—	HD46805	MC6805	—	—
S6808	F6808	—	HD46808	MC6808	—	—
S6809	—	—	—	MC6809	—	—
S6810	F6810	—	HD46810	MC6810	—	—
S6821	F6821	—	HD46821	MC6821	—	—
S6840	F6840	—	HD46840	MC6840	—	—
S6846	F6846	—	HD46846	MC6846	—	—
S6850	F6850	—	HD46850	MC6850	—	—
S6852	F6852	—	HD46852	MC6852	—	—
S6854	F6854	—	HD46854	MC6854	—	—
S68488	F68488	—	HD468488	MC68488	—	—
S6894	—	—	—	—	—	—
S68045	—	—	—	—	—	—
S68047	—	—	—	—	—	—

S9900 Family

AMI	Texas Instruments
S9900	TMS9900
S9901	TMS9901
S9902	TMS9902
S9903	TMS9903
S9940	TMS9940
S9980	TMS9980
S9981	TMS9981

AMI's Six Step Program for Success in Custom LSI.

No other company can match AMI's track record in developing state-of-the-art custom MOS products. With more than 2,000 custom devices designed and manufactured since 1967, AMI has more experience than any other integrated circuit company in building a wide variety of custom microcircuits.

AMI not only has the experience but the design engineering organization and the advanced production and testing facilities to produce the highest quality MOS/LSI circuits. Because AMI also offers standard memory, microprocessor, telecommunication and consumer products and the widest variety of custom LSI processes in the industry, we're able to be objective in helping customers determine their most cost effective approach.

AMI can participate at any level of the custom LSI process.

We participate at any level in the design of the custom IC, from the classic "we'll-design-and-produce-it-for-you" approach where we have complete responsibility, to the "Customer Tooling" cooperative approach for customers who do their own design but want us to do the manufacturing. We will even enter into long-term, fully-funded joint development agreements, designing ICs for families of end products, joining together your systems designers with our circuit designers.

We've developed a six step program in which you, the customer, can work with us to successfully develop the custom IC for your product by:

1. **Considering All the Factors.**
2. **Looking At the Custom Options.**
3. **Selecting the Right MOS/LSI Process.**
4. **Designing The Best Circuit.**
5. **Fabricating the Optimum Device.**
6. **Testing For Reliable Performance.**

The results are a unique product designed to your complete satisfaction.

Step One: Considering all the Factors.

There are many ways to build your product, so, why do we believe the custom MOS/LSI approach is right for you? For the answer let's look at the alternatives:

Electromechanical. These assemblies suffer compared to MOS circuits: in reliability because moving parts wear; in convenience because of the greater space needed; and because of their limits in handling highly complex functions.

Hardwired Logic. This is more expensive due to the high labor and material cost involved. Much space is needed and power is much higher than for MOS/LSI circuits.

Standard Circuits. Standard ICs perform the same jobs as custom ICs but require more devices, higher assembly costs, more power and space with lower reliability.

Microprocessors. Using standard microprocessors requires several microcircuits, and much of the device's capability may not be needed. A custom circuit, however, can combine all your needed functions on one IC, conserving space and cost.

The custom MOS/LSI decision

The advantages of custom MOS/LSI circuits become more apparent when considered in relation to IC complexity, component count, power consumption and confidentiality (it's your circuit exclusively).

Complexity. An application suitable for custom LSI is usually one needing moderately complex circuits or functions; i.e., more than 15 to 2,000 gates. Fewer than this might not justify the engineering, design, and manufacturing effort required for the custom IC.

Custom LSI may be the only way technically to achieve a desired result, no matter what the development cost.

Component Count. An important consideration affecting cost is the number of components in a system that are eliminated by the substitution of a single custom LSI circuit. A reduction in component count significantly lowers the number of electrical interconnections and increases product reliability.

This factor often reduces troubleshooting problems at the board, subsystem and system levels, minimizes field

repairs and usually reduces warranty costs. The reduction in component count also decreases assembly and initial checkout costs.

Power Consumption. The amount of power required to operate an end product is increasingly an important consideration. MOS/LSI circuits require much less power than the electro-mechanical and hardwired logic alternatives. A custom MOS/LSI solution usually requires less power than the multi-chip alternatives offered by standard circuits and microprocessors. For battery operated designs, we offer custom, high performance/ultra-low power complementary MOS (CMOS) capability.

Confidentiality. Of prime concern in any highly competitive market situation is confidentiality of design. AMI treats each circuit assignment as a highly proprietary project insuring complete security to, and through, the product's manufacturing life.

Step Two: Looking at the Custom Options.

AMI experience has shown that each customer has unique needs based on system requirements and the customer's technical capability regarding design and implementation of non-catalog MOS products. AMI's interface with the customer typically includes one or more of the following non-catalog product capabilities, the combination structured to satisfy the particular customer requirement:

- ☐ AMI designs and manufactures the circuit to meet a customer-developed specification.
- ☐ The customer develops the test specification, circuit design and test program, with AMI manufacturing the circuit to the customer-designed tooling.
- ☐ AMI provides training in integrated circuit design through joint customer/AMI development teams or provides capability through technology transfers to the customer's engineering and manufacturing organizations.
- ☐ Customer-provided schematics or tooling inputs are implemented in semi-custom uncommitted logic arrays.

The total AMI approach

AMI's custom capability encompasses the entire development sequence of a product. The services we provide start with five conceptual planning steps:

- ☐ System Definition;
- ☐ System Design and Partitioning;
- ☐ Preliminary Logic Design/Simulation;
- ☐ Final Logic Design; and
- ☐ LSI Circuit Design.

First, system definition requires the customer to have full knowledge of the system requirements for the custom IC. Working with AMI's application engineers, the two companies form a team to develop a final system which not only meets the needs, but optimizes performance and economics.

Second, system partitioning follows the joint development of system definition. This involves the cataloging of functions into MOS subfunctions, and then into chip functions. At this step the optimum MOS process for the application is chosen. Usually, functional flow charts and timing diagrams are generated at this time as a preliminary step in logic design.

Once partitioning is complete, preliminary logic design and simulation can be done. The chip functions are translated into MOS logic diagrams. Traditional breadboarding techniques are quite often used to verify these logic designs. AMI uses proprietary computerized simulation programs for verification. These programs check the design as well as help reduce time and cost factors for design verification.

Final logic design is next. First, system errors discovered through breadboarding or simulation are corrected. Earlier partitioning may be refined if the final logic design indicates the need. During the final logic design step all system design objectives are analyzed again. MOS logic diagrams are finalized, the chip sizes are estimated, and testing procedures are generated.

And then—the chip design. The topological chip layout is a precise science. The exact dimensions and placement for each transistor and other components must be determined. Here again AMI uses computerized circuit analysis programs to validate chip designs and verify that the design meets the performance objectives. The computerized analysis not only substantiates logic, it is an integral part of the on-going quality assurance program at AMI.

The customer design approach

The Customer-Designed product approach provides all of the advantages of a full custom implementation at lower volumes, since the engineering development is shared between the customer and AMI. This approach allows the customer to maintain complete control over the logic and

electrical requirements and the design schedule during the majority of the development phase. The customer can easily implement changes and improvements due to changes in the total system requirement prior to finalization of the system performance specification.

The customer can develop the tooling and test program within his own facility or by use of independent design capability. In either case AMI provides technical information on its available standard MOS processes, test program formats, pattern generator and data base tape input formats and support for device modeling and simulation through computer timeshare services. Specific questions encountered or technical information required during the design phase is provided through an engineer-to-engineer interface supported by AMI's Customer-Designed product engineers. AMI also offers as part of its services an automated design rule check to insure that customer-designed circuits have the layouts consistent with AMI's MOS process requirements.

From the tooling inputs and completed questionnaires furnished by the customer, AMI will prepare 10X reticles and furnish blow-ups to verify proper accomplishment of the data conversion and preliminary verification of the conformance of the design to the electrical schematic.

Once the customer provides blow-up approval, AMI then completes preparation of the working plates and processes two lots of wafers, verifying that the completed wafers meet process and optical requirements. AMI then ships sample quantities of untested devices or several unsorted wafers, as required. These untested but optically good devices are used by the customer to verify the circuit is the logical and functional equivalent of the schematic.

After the customer approves the untested sample devices, AMI then performs acceptance verification of completely developed test programs supplied by the customer or completes test program development from customer-supplied test vectors, and supplies the necessary hardware for testing as well as the completion of required manufacturing documentation. We finish this task before providing the customer with a small quantity of prototype parts. These prototype parts will have been tested to the completed test program and are guaranteed to be in conformance with the customer-supplied electrical and test specification. Since these devices are identical to those which will be provided in a production phase, the customer provides final approval before the product package is transferred to production. Initial production quantities in excess of pilot requirements can typically be made available within 16 weeks after approval of the prototype units.

Depending on customer requirements and capability, AMI can provide completely assembled and tested units in compliance to portions or all of military specifications 38510 or 883 for application in hostile environments. AMI can also provide untested assemblies as well as dice in wafer or individual form created from tooling provided in the pattern generator or data base input tape form. Wafers provided to process and optical specification can be provided from pattern generator tape, data base tape or working plate inputs. Working plate inputs can also be used to verify, through production of prototype quantities of wafers, process compatibility between another organization's process and AMI's standard process.

. . . But there are other options

We're not biased particularly in favor of custom LSI, especially if it becomes clear it's not the best way to solve a customer problem. AMI is also a major microprocessor supplier in the 4-, 8-, and 16-bit categories: our own family of S2000 single chip microcomputers, the Motorola-designed 6800, and Texas Instrument's 9900 product line, respectively.

By having available both custom LSI and standard microprocessors, we can offer customers alternatives that can also combine the two. For example, to test the market for a new product, we can design a microprocessor-based system which provides a relatively quick, though not necessarily cost effective way to get a product to market. As part of the approach, we customize the microprocessor program or "software," and then, if the product is successful, design and make a custom LSI circuit dedicated to that particular application.

But if a microprocessor—ours or anyone else's—is the best solution, custom LSI is still useful, for microprocessors can't operate alone. They need interface devices. To achieve a system with a minimum chip count, custom devices can be designed to allow the customer to efficiently interface standard microprocessors with the customer's system.

Step Three: Choosing the right MOS/LSI process.

One of the most important decisions to be made in the custom LSI approach is determining the right MOS/LSI process.

Where many of our competitors offer one, and possibly two MOS processes with which to build devices, AMI offers seven custom MOS process options, more than any other company supplying custom circuits. They are:

P-channel high voltage metal gate

This is the most mature process in the industry and because of its relative simplicity, has the lowest cost per wafer. It provides high noise immunity, making it ideal for applications involving mechanical equipment which can generate RF noise and where low power dissipation is not a prime requirement.

P-channel ion implanted metal gate

This is very similar to its high voltage P-channel process, with two additional processing steps. An ion implantation of the gate areas reduces the device thresholds to levels consistent with the low voltage P-channel process while at the same time retaining the high field thresholds of the high voltage process.

A second ion implant in selected gate regions reduces those thresholds to the point of forcing depletion mode transistor operation. The use of depletion mode devices as load transistors greatly increases device speed per unit area, can lower power, improve noise margins, makes bipolar interfacing easier, permits the use of unregulated power supplies, and allows generation of full amplitude signals on chip with only one power supply. This latter feature can be especially useful in converting certain logic implementations to much simpler forms which thereby reduce chip area significantly. This process has been used in several different standard memory products as well as many custom chip applications where speed, noise immunity and wide power supply tolerances are specified.

P-channel silicon gate (SiGate)

This process has two main features: (1) somewhat smaller transistor structures due to a self-aligning fabrication technique that eliminates certain masking tolerance problems, and (2) a partial third layer of interconnect which can sometimes significantly reduce cell area and interconnections between cells. The self-aligning gate structure lowers the effective gate capacitance. The circuit response is faster than regular P-channel low voltage devices, but slower than ion implanted circuits with depletion mode load devices. This process has been mostly used in memory applications and in customer tooled circuits. AMI no longer designs products in this process.

N-channel silicon gate

This process uses ion implantation in the field areas to achieve high field threshold without having to resort to thick field oxides. Then the gate regions are implanted to establish the required control of device thresholds. This process is designed for single supply circuits that do not have stringent performance requirements but must have significant packing densities. This packing density results from the following: (1) for a given device N-channel can charge or discharge a mode faster than P-channel, (2) the self-aligning feature of the process, and, (3) the extra layer of interconnect inherent in silicon gate which can be used to reduce chip interconnect area.

N-channel ion implanted SiGate with depletion loads

This is a high performance process; it offers all the advantages of the N-channel, ion implanted SiGate process plus the increased speed associated with depletion loads. The drawback to this process lies in the increased complexity of the additional processing steps.

Complementary MOS (CMOS)

The CMOS technology has many advantages. Its biggest asset is that CMOS draws very little power. The majority of the power is consumed when switching occurs. Under static conditions or during power down CMOS dissipates virtually no DC power. CMOS is also very fast, and it has very high noise immunity, comparable to ion implanted circuits using depletion mode transistors. Like ion implanted depletion mode circuits, CMOS can work over a very wide single supply power range. The area used per logic function has been larger than with other processes, but this is decreasing with advanced CMOS techniques. CMOS chips are currently used in low power, often battery operated applications such as electronic watches, clocks, and memories where the ability to work at very low power is an absolute requirement, and in automotive electronics, where low standby current and high noise immunity are important. CMOS is also making important inroads into microprocessors and communications circuitry.

Present CMOS technologies include both standard metal gate and silicon gate, as well as a high density, isoplanar silicon gate process.

Five-Micron CMOS

AMI's major second generation 5-micron CMOS process uses an n+ only ubiquitous P-well approach to improve performance, simplify layout and reduce circuit size. This process permits implanting in the field oxide region, thus eliminating guard rings. AMI's process also reduces P-well doping levels below alternative 5-micron processes

and consequently lowers junction capacitances and increases switching speeds.

We use this 5-micron process to design and produce switched capacitor circuits for analog and digital functions. Among the kinds of circuits that can benefit enormously from mixed digital-analog approaches are low-noise, high-gain op amps, high-speed offset-cancelled comparators and high-current line buffers. CMOS linear subsystems have appeared on AMI-designed circuits to perform A to D and D to A conversion, switched capacitor filtering and quasi-adaptive phase lock and auto-zero loops. System level integrated circuits have been designed and fabricated for complex filter functions, DTMF, MF and SF receivers, low and medium speed modems, codecs, voice compression, industrial control and voice synthesis.

Step Four: Designing the best circuit.

A key to AMI's success in the custom LSI business is its Computer-Aided Design (CAD) capability. Our CAD capabilities, the most advanced in the semiconductor industry, are based on a wealth of experience in custom MOS/LSI circuit design work. CAD software and hardware aids are employed throughout the custom IC development cycle, from the early logic design stage to creation of production tooling.

Logic Simulation

Early in the design phase logic simulation is used to verify that the logic is sound. The circuit is extensively simulated to verify logical correctness as well as timing and signal propagation characteristics. Logic simulation is used throughout the design cycle from hierarchical block-level logic design to test program generation.

SIMAD is an MOS oriented four-state logic simulator which supports assignable rise and fall switching delay. It includes such features as:

- ☐ block-oriented input notation, including macros, Boolean expressions, and array notation;
- ☐ basic logic gates, several types of MOS transmission gates, RAMs, ROMs, shift-registers, and user specified combinational logic gates;
- ☐ four-state (ϕ, 1, u, z) simulation;
- ☐ multi-phase user specified clocking schemes;
- ☐ assignable rise and fall delay;
- ☐ race detection and inertial delay simulation;
- ☐ versatile input, output, and simulation control options;
- ☐ checkpoint-restart capability;
- ☐ accurate initialization algorithm;
- ☐ extensive compression and formating of simulation results for automatic test equipment.

Circuit simulation

At the circuit design phase, a circuit simulator containing semiconductor device models is used to identify undesirable circuit behavior. Exact circuit behavior is simulated and the results are used to insure the circuit will operate within allowable tolerances.

The ASPEC circuit simulator can perform non-linear DC, non-linear DC transfer function, non-linear transient and small signal (linear) AC circuit analysis. Built-in component models include independent voltage and current sources; linear elements such as resistance, inductance, capacitance, transconductance, voltage controlled switches and coupled-inductors. Non-linear transistor models for junction field effect transistors (JFETs), MOSFETs, and bipolar junction transistors (BJT) are also available.

The MOSFET model simulates linear and saturation region DC operation; body effect as a function of substrate bias; channel length modulation in saturation; mobility reduction at elevated gate voltages; channel pinchoff; short channel effects; weak inversion; as well as full non-linear voltage-dependent modeling of the MOS capacitors which determine device transient behavior.

Symbolic mask design using SIDS

AMI has developed an advanced symbolic mask design system for MOS ICs. This Symbolic Interactive Design System (SIDS) reduces the total mask design cycle time as much as 50 percent, with half the manpower effort and half the cost of the hand drawn approach. SIDS eliminates hand drafting by using symbols to represent complex multi-level circuit elements.

SIDS circuit masks are designed symbolically on an interactive color CRT terminal. The mask design process is supported by such checking aids as:

- ☐ Design Rule Checking (DRC) which checks for all symbol-to-symbol layout violations;
- ☐ TRACE, which traces a circuit node and visually highlights the node on the color CRT terminal so the user can observe circuit continuity errors.
- ☐ CONTINUITY, which generates a net list from a logic description file, compares it to a net list traced from the symbolic layout, and prints out any continuity differences.

The final SIDS step is the conversion from symbols to polygons (STP) and the generation of the pattern generation (PATGEN) tape.

Hardware design aids

- ☐ On-site Burroughs 7765 large scale computer with multiprocessing capability.
- ☐ Prime minicomputers in Santa Clara, Pocatello and Swindon, England.
- ☐ A Calma GDSII interactive graphics system for digitizing and editing of composite drawings; includes 3 digitizing surfaces and 4 CRT edit stations.
- ☐ High speed, high resolution Electromask pattern generator.
- ☐ Versatec 42 inch high speed electrostatic plotter.
- ☐ Calcomp 748 Flatbed Plotter.

Software design aids

- ☐ ASPEC Circuit Simulator
- ☐ Semiconductor device models tailored to AMI processes
- ☐ Tides Logic Simulator for:
  - — Logic Validation
  - — Pattern Validation
  - — Test Word Generation
- ☐ SIDS for mask design
- ☐ Geometrical Design Rule Checking (DRC) for hand drawn circuits
- ☐ Trace and continuity checking for hand drawn circuits
- ☐ Device test program development aids

Step Five: Fabricating the optimum device.

A partnership

AMI's long history of success in the custom MOS/LSI business is the result of a close, working partnership between AMI and each of our customers.

These customers have taken advantage of orders of magnitude increases in circuit complexity over the years, thereby reducing even further the component count in their systems.

The flexibility of AMI's development program allows the customer to select the interface point best suited to his particular needs. The most common interface points are noted as (*) in the review of the sequence of steps involved in developing a custom MOS/LSI circuit below:

1. System Definition Design (*)
2. Preliminary logic design and simulation(*)
3. Final logic design and system design review
4. Chip circuit design
5. Topological design
6. Artwork generation (*)
7. Mask fabrication (*)
8. Wafer fabrication and map test
9. Wafer sort test (*)
10. Final test and characterization
11. Product assurance tests

Step Six: Testing for reliable performance.

Currently more than 50% of the custom LSI circuits designed by AMI work the first time. The key to this impressive record is a comprehensive program of quality assurance, rigorous testing and constant double checking of each step.

It starts at the initial stages of logic design, with the custom LSI chip designed to incorporate facilities for ease of testing and ends with prototype debugging.

Common test data base

To facilitate the processing of vast quantities of test data, a base of parametric and functional information with run, wafer or die resolution has been created by AMI engineers.

With this data analysis system, each user creates a personal data base secured by user code and information inputted from magnetic tape, cards or remote terminals. Using an interactive command language for manipulation of data, subsets of test information can be retrieved and listed through the use of key attributes—test group, process, product number, test date, test time at start, operator ID, save data, run or lot number. The retrieved data base subset can be analyzed statistically as: histograms, scatter plots, wafer maps, trend charts, tabulations of percentiles, means, standard deviations and correlation coefficients.

Extensive test facilities

AMI maintains sixteen Fairchild Sentry II and 600 automated test systems and three Sentry VII's, plus a wide range of other testers for debugging of protypes,

solving design and testing problems and production testing.

Quality assurance

An on-going activity that pervades the entire design and manufacturing process is AMI's quality assurance program. This includes a special group of inspectors organizationally separate from the production group, whose main responsibility is to examine and test the custom LSI circuits and all the raw materials that go into them. Some of the quality control checkpoints include:

- ☐ final logic design where system objectives are reviewed;
- ☐ chip circuit design, where it is verified that performance meets objectives;
- ☐ working plates check;
- ☐ mask fabrication check;
- ☐ wafer fabrication check;
- ☐ wafer sort;
- ☐ scribe and break with 100% optical inspection;
- ☐ die attach checks;
- ☐ lead bonding followed by 100% preseal optical inspection;
- ☐ seal checks;
- ☐ final tests; and,
- ☐ final electrical/environmental tests.

At each one of these pre-production steps meticulous checks of both design and workmanship are made. And only after the checks at each of these steps are completed is a device considered fully manufacturable. It is then turned over to production with its yield history. In production a similar series of quality control checks is made.

Custom MOS/LSI from AMI

The information in this section has been presented to show not only how and why custom can be used, but also to explain the types of custom services available at AMI, and the level of commitment at AMI to total custom circuit development and to customer tooling processing. If your application can benefit from high quality custom MOS/LSI circuits, AMI is the place to go for design, engineering, manufacturing, and testing capability.

Contact factory for complete data sheet

AMERICAN MICROSYSTEMS, INC.

Communication Products Selection Guide

STATION PRODUCTS

Part No.	Description	Process	Power Supplies	Packages
S2559A/B	Digital Tone Generator	CMOS	3.5V to 13V	16 Pin
S2559C/D	Digital Tone Generator	CMOS	2.75V to 10V	16 Pin
S2559E/F/G/H	Digital Tone Generator	CMOS	2.5V to 10V	16 Pin
S2859	Digital Tone Generator	CMOS	3.0V to 10.0V	16 Pin
S2860	Digital Tone Generator	CMOS	3.5V	16 Pin
S2560A	Pulse Dialer	CMOS	1.5V to 3.5V	18 Pin
S2561, S2561C	Tone Ringer	CMOS	4.0V to 12.0V	18 Pin
S2561A	Tone Ringer	CMOS	4.0V to 12.0V	8 Pin
S2562	Repertory Dialer	CMOS	3.5V to 7.5V	40 Pin

PCM PRODUCTS

Part No.	Description	Process	Power Supplies	Packages
S3501/S3501A	μ-Law Encoder with Filter	CMOS	$\pm$5V	18 Pin
S3502/S3502A	μ-Law Decoder with Filter	CMOS	$\pm$5V	16 Pin
S3503	A-Law Encoder with Filter	CMOS	$\pm$5V	18 Pin
S3504	A-Law Decoder with Filter	CMOS	$\pm$5V	16 Pin
S3505	μ-Law Codec with Filters	CMOS	$\pm$5V	24 Pin
S3505A	μ-Law Codec with Filters	CMOS	$\pm$5V	28 Pin

OTHER PRODUCTS

S2811	Signal Processing Peripheral	VMOS	5V	28 Pin
S2814	Fast Fourier Transformer	VMOS	5V	28 Pin
S3525A/B	DTMF Bandsplit Filter	CMOS	10.0V to 13.5V	18 Pin

PRODUCTS TO BE INTRODUCED IN 1981

S25089	DTMF Generator	Direct replacement for the Mostek MK5089 DTMF generator
S25610	Repertory Dialer	Single chip key-pad to pulse converter with on-chip memory for ten 14-digit numbers. Last number redial feature. Can be directly powered by the telephone line. Uses S2560A pin-out.
S3506	A-Law Codec with Filters	Single chip A-law codec.
S3507	μ-Law Codec with Filters	Similar to S3505 but with enhanced feature set.
S3610	Speech Synthesizer	CMOS LPC synthesizer. Has internal 20K ROM and output amplifier. Generates up to 32 words of speech (approximately 17 seconds).
S3620	Speech Synthesizer	Similar to the 3610 synthesizer except that the memory is external. The number of words generated is directly proportional to the amount of ROM used (13 sec/16K bits).
S3630	128K ROM	16K$\times$8 NMOS ROM. 10μs access time. Has power down feature.

DIGITAL TONE GENERATOR

Features

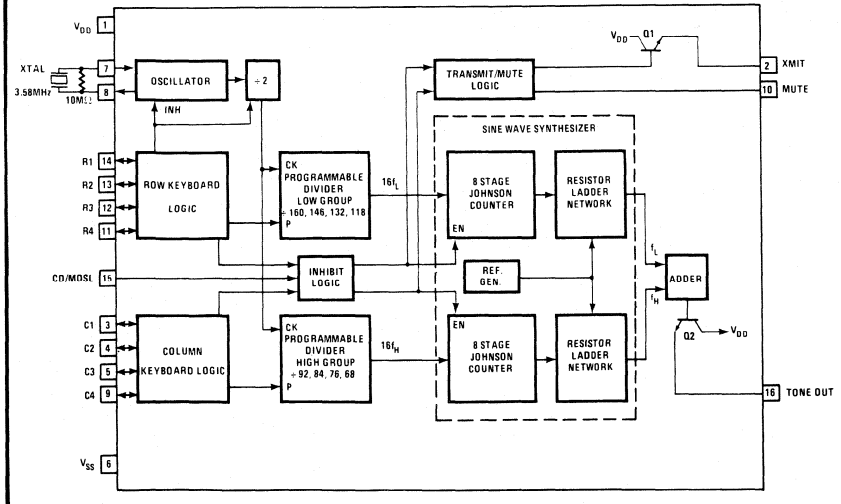
- ☐ **Wide Operating Supply Voltage Range: 3.5 to 13.0 Volts (A, B) 2.75 to 10 Volts (C, D)**
- ☐ **Low Power CMOS Circuitry Allows Device Power to be Derived Directly from the Telephone Lines or from Small Batteries, e.g., 9V**
- ☐ **Uses TV Crystal Standard (3.58 MHz) to Derive all Frequencies thus Providing Very High Accuracy and Stability**
- ☐ **Mute Drivers On Chip**
- ☐ **Interfaces Directly to a Standard Telephone Push-Button or Calculator Type X-Y Keyboard**
- ☐ **The Total Harmonic Distortion is Below Industry Specification**
- ☐ **On Chip Generation of a Reference Voltage to Assure Amplitude Stability of the Dual Tones Over the Operating Voltage and Temperature Range**
- ☐ **Dual Tone as Well as Single Tone Capability**
- ☐ **Four Options Available:**

  A:3.5 to 13.0V Mode Select
  B:3.5 to 13.0V Chip Disable
  C: 2.75 to 10V Mode Select
  D: 2.75 to 10V Chip Disable

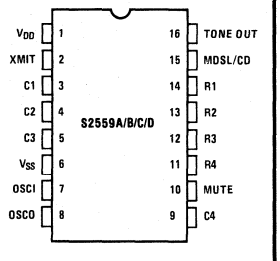
General Description

The S2559 Digital Tone Generator is specifically designed to implement a dual tone telephone dialing system. The device can interface directly to a standard pushbutton telephone keyboard or calculator type X-Y keyboard and operates directly from the telephone lines. All necessary dual-tone frequencies are derived from the widely used TV crystal standard providing very high accuracy and stability. The required sinusoidal waveform for the individual tones is digitally synthesized on the chip. The waveform so generated has very low total harmonic distortion. A voltage reference is generated on the chip which is stable over the operating voltage and temperature range and regulates the signal levels of the dual tones to meet the recommended telephone industry specifications. These features permit the S2559 to be incorporated with a slight modification of the standard 500 type telephone basic circuitry to form a pushbutton dual-tone telephone. Other applications of the device include radio and mobile telephones, remote control, Point-of-Sale, and Credit Card Verification Terminals and process control.

Block Diagram



Pin Configuration



Absolute Maximum Ratings

DC Supply Voltage ($V_{DD}-V_{SS}$) S2559 A, B ..... +13.5V
DC Supply Voltage ($V_{DD}-V_{SS}$) S2559 C, D ..... +10.5V
Operating Temperature ..... −25°C to +70°C
Storage Temperature ..... −65°C to +140°C
Power Dissipation at 25°C 500mW
Input Voltage ..... $-0.6 \leq V_{IN} \leq V_{DD}+0.6$

S2559A & B Electrical Characteristics:

(Specifications apply over the operating temperature range of −25°C to 70°C unless otherwise noted. Absolute values of measured parameters are specified.)

Symbol	Parameter/Conditions		($V_{DD}-V_{SS}$) Volts	Min.	Typ.	Max.	Units
	Supply Voltage						
V_{DD}	Tone Out Mode (Valid Key Depressed)			3.5		13.0	V
	Non Tone Out Mode (No Key Depressed)			3.0		13.0	V
	Supply Current						
I_{DD}	Standby (No Key Selected, Tone, XMIT and MUTE Outputs Unloaded)		3.5		0.4	40	μA
			13.0		1.5	130	μA
	Operating (One Key Selected, Tone, XMIT and MUTE Outputs Unloaded)		3.5		0.95	2.9	mA
			13.0		11	33	mA
	Tone Output						
V_{OR}	Single Tone Mode Output Voltage	Row Tone, $R_L=390\Omega$	5.0	417	596	789	mVrms
		Row Tone, $R_L=240\Omega$	12.0	378	551	725	mVrms
dB_{CR}	Ratio of Column to Row Tone		3.5−13.0	1.75	2.54	3.75	dB
%DIS	Distortion*		3.5−13.0			10	%
	XMIT, MUTE Outputs						
V_{OH}	XMIT, Output Voltage, High (No Key Depressed)(Pin 2)	($I_{OH}=15mA$)	3.5	2.0	2.3		V
		($I_{OH}=50mA$)	13.0	12.0	12.3		V
I_{OF}	XMIT, Output Source Leakage Current, $V_{OF}=0V$		13.0			100	μA
V_{OL}	MUTE (Pin 10) Output Voltage, Low, (No Key Depressed), No Load		3.5		0	0.4	V
			13.0		0	0.5	V
V_{OH}	MUTE, Output Voltage, High, (One Key Depressed) No Load		3.5	3.0	3.5		V
			13.0	13.0	13.5		V
I_{OL}	MUTE, Output Sink Current	$V_{OL}=0.5V$	3.5	0.66	1.7		mA
			13.0	3.0	8.0		mA
I_{OH}	MUTE, Output Source Current	$V_{OH}=2.5V$	3.5	0.18	0.46		mA
		$V_{OH}=9.5V$	13.0	0.78	1.9		mA
	Oscillator Input/Output						
I_{OL}	Output Sink Current One Key Selected	$V_{OL}=0.5V$	3.5	0.26	0.65		mA
		$V_{OL}=0.5V$	13.0	1.2	3.1		mA
I_{OH}	Output Source Current One Key Selected	$V_{OH}=2.5V$	3.5	0.14	0.34		mA
		$V_{OH}=9.5V$	13.0	0.55	1.4		mA

**Distortion measured in accordance with the specifications described in Ref. 1 as the "ratio of the total power of all extraneous frequencies in the voiceband above 500Hz accompanying the signal to the total power of the frequency pair".*

S2559A & B Electrical Characteristics: (Continued)

Symbol	Parameter/Conditions		($V_{DD}-V_{SS}$) Volts	Min.	Typ.	Max.	Units
	Input Current						
I_{IL}	Leakage Sink Current, One Key Selected	V_{IL}=13.0V	13.0			1.0	μA
I_{IH}	Leakage Source Current One Key Selected	V_{IH}=0.0V	13.0			1.0	μA
I_{IL}	Sink Current	V_{IL}=0.5V	3.5	24	93		μA
	No Key Selected	V_{IL}=0.5V	13.0	27	130		μA
t_{START}	Oscillator Startup Time		3.5		3	6	mS
			13.0		0.8	1.6	mS
$C_{I/O}$	Input/Output Capacitance				12	16	pF
					10	14	pF
	Input Currents						
I_{IL}	Row & Column Inputs	Sink Current, V_{IL}=3.5V (Pull-down)	3.5	7	17		μA
		Sink Current V_{IL}= 13.0V (Pull-down)	13.0	150	400		μA
I_{IH}		Source Current, V_{IH}=3.0V (Pull-up)	3.5	90	230		μA
		Source Current, V_{IH}=12.5V (Pull-up)	13.0	370	960		μA
I_{IH}	Mode Select Input (S2559C)	Source Current, V_{IH}=0.0V (Pull-up)	3.5	1.5	3.6		μA
		Source Current, V_{IH}=0.0V (Pull-up)	13.0	23	74		μA
I_{IL}	Chip Disable Input (S2559D)	Source Current, V_{IL}=3.5V (Pull-down)	3.5	4	10		μA
		Sink Current, V_{IL}=13.0V (Pull-down)	13.0	90	240		μA

S2559C & D Electrical Characteristics:

(Specifications apply over the operating temperature range of −25°C to 70°C unless otherwise noted. Absolute values of measured parameters are specified.)

Symbol	Parameter/Conditions		($V_{DD}-V_{SS}$) Volts	Min.	Typ.	Max.	Units
	Supply Voltage						
V_{DD}	Tone Out Mode (Valid Key Depressed)			2.75		10.0	V
	Non Tone Out Mode (No Key Depressed)			2.5		10.0	V
	Supply Current						
I_{DD}	Standby (No Key Selected, Tone, XMIT and MUTE Outputs Unloaded)		3.0		0.3	30	μA
			10.0		1.0	100	μA
	Operating (One Key Selected, Tone, XMIT and MUTE Outputs Unloaded)		3.0		1.0	2.0	mA
			10.0		8	16.0	mA
	Tone Output						
V_{OR}	Single Tone Mode Output Voltage		3.5	250	362	474	mVrms
		Row Tone, R_L=390Ω	5.0	367	546	739	mVrms
		Row Tone, R_L=240Ω	10.0	350	580	730	mVrms

S2559C & D Electrical Characteristics: (Continued)

Symbol	Parameter/Conditions		($V_{DD}-V_{SS}$) Volts	Min.	Typ.	Max.	Units
dB_{CR}	Ratio of Column to Row Tone		3.0–10.0	1.75	2.54	3.75	dB
%DIS	Distortion*		3.0–10.0			10	%
	XMIT, MUTE Outputs						
V_{OH}	XMIT, Output Voltage, High	(I_{OH}=15mA)	3.0	1.5	1.8		V
	(No Key Depressed)(Pin 2)	(I_{OH}=50mA)	10.0	8.5	8.8		V
I_{OF}	XMIT, Output Source Leakage Current, V_{OF}=0V		10.0			100	μA
V_{OL}	MUTE (Pin 10) Output Voltage, Low,		2.75		0	0.5	V
	(No Key Depressed), No Load		10.0		0	0.5	V
V_{OH}	MUTE, Output Voltage, High,		2.75	2.5	2.75		V
	(One Key Depressed) No Load		10.0	9.5	10.0		V
I_{OL}	MUTE, Output Sink Current	V_{OL}=0.5V	3.0	0.53	1.3		mA
			10.0	2.0	5.3		mA
I_{OH}	MUTE, Output Source Current	V_{OH}=2.5V	3.0	0.17	0.41		mA
		V_{OH}=9.5V	10.0	0.57	1.5		mA
	Oscillator Input/Output						
I_{OL}	Output Sink Current	V_{OL}=0.5V	3.0	0.21	0.52		mA
	One Key Selected	V_{OL}=0.5V	10.0	0.80	2.1		mA
I_{OH}	Output Source Current	V_{OH}=2.5V	3.0	0.13	0.31		mA
	One Key Selected	V_{OH}=9.5V	10.0	0.42	1.1		mA
	Input Current						
I_{IL}	Leakage Sink Current, One Key Selected	V_{IL}=10.0V	10.0			1.0	μA
I_{IH}	Leakage Source Current One Key Selected	V_{IH}=0.0V	10.0			1.0	μA
I_{IL}	Sink Current	V_{IL}=0.5V	3.0	24	93		μA
	No Key Selected	V_{IL}=0.5V	10.0	27	130		μA
t_{START}	Oscillator Startup Time		3.5		2	5	mS
			10.0		0.25	4	mS
$C_{I/O}$	Input/Output Capacitance		3.0		12	16	pF
			10.0		10	14	pF
	Input Currents						
I_{IL}	Row & Column Inputs	Sink Current, V_{IL}=3.0V (Pull-down)	3.0	6.5	16		μA
		Sink Current V_{IL}=10.0V (Pull-down)	10.0	9.2	24		μA
I_{IH}		Source Current, V_{IH}=2.5V (Pull-up)	3.0	85	210		μA
		Source Current, V_{IH}=9.5V (Pull-up)	10.0	280	740		μA
I_{IH}	Mode Select Input (S2559C)	Source Current, V_{IH}=0.0V (Pull-up)	3.0	1.4	3.3		μA
		Source Current, V_{IH}=3.0V (Pull-up)	10.0	18	46		μA
I_{IL}	Chip Disable Input (S2559D)	Source Current, V_{IL}=3.0V (Pull-down)	3.0	3.9	9.5		μA
		Sink Current, V_{IL}=10.0V (Pull-down)	10.0	55	143		μA

**Distortion measured in accordance with the specifications described in Ref. 1 as the "ratio of the total power of all extraneous frequencies in the voiceband above 500Hz accompanying the signal to the total power of the frequency pair".*

Table 1. Comparisons of Specified vs Actual Tone Frequencies Generated by S2559

ACTIVE INPUT	OUTPUT FREQUENCY Hz		% ERROR SEE NOTE
	SPECIFIED	ACTUAL	
R1	697	699.1	+0.30
R2	770	766.2	−0.49
R3	852	847.4	−0.54
R4	941	948.0	+0.74
C1	1,209	1,215.9	+0.57
C2	1,336	1,331.7	−0.32
C3	1,477	1,471.9	−0.35
C4	1,633	1,645.0	+0.73

NOTE: % Error does not include oscillator drift.

Table 2. XMIT and MUTE Output Functional Relationship

OUTPUT	'DIGIT' KEY RELEASED	'DIGIT' KEY DEPRESSED	COMMENT
XMIT	V_{DD}	High Impedance	Can source at least 50mA at 10V with 1.5V max. drop
MUTE	V_{SS}	V_{DD}	Can source or sink current

Circuit Description

The S2559 is designed so that it can be interfaced easily to the dual tone signaling telephone system and that it will more than adequately meet the recommended telephone industry specifications regarding the dual tone signaling scheme.

Design Objectives

The specifications that are important to the design of the Digital Tone Generator are summarized below: the dual tone signal consists of linear addition of two voice frequency signals. One of the two signals is selected from a group of frequencies called the "Low Group" and the other is selected from a group of frequencies called the "High Group". The low group consists of four frequencies 697, 770, 852 and 941 Hz. The high group consists of four frequencies 1209, 1336, 1477 and 1633 Hz. A keyboard arranged in a row, column format (4 rows x 3 or 4 columns) is used for number entry. When a push button corresponding to a digit (0 thru 9) is pushed, one appropriate row (R1 thru R4) and one appropriate column (C1 thru C4) is selected. The active row input selects one of the low group frequencies and the active column input selects one of the high group frequencies. In standard dual tone telephone systems, the highest high group frequency of 1633Hz (Col. 4) is not used. The frequency tolerance must be ±1.0%. However, the S2559 provides a better than .75% accuracy. The total harmonic and intermodulation distortion of the dual tone must be less than 10% as seen at the telephone terminals. (Ref. 1.) The high group to low group signal amplitude ratio should be 2.0 ±2dB and the absolute amplitude of the low group and high group tones must be within the allowed range. (Ref. 1.) These requirements apply when the telephone is used over a short loop or long loop and over the operating temperature range. The design of the S2559 takes into account these considerations.

Oscillator

The device contains an oscillator circuit with the necessary parasitic capacitances on chip so that it is only necessary to connect a 10MΩ feedback resistor and the standard 3.58MHz TV crystal across the OSCI and OSCO terminals to implement the oscillator function. The oscillator functions whenever a row input is activated. The reference frequency is divided by 2 and then drives two sets of programmable dividers, the high group and the low group.

Keyboard Interface

The S2559 employs a calculator type scanning circuitry to determine key closures. When no key is depressed, active pull-down resistors are "on" on the row inputs and active pull-up resistors are "on" on the column inputs. When a key is pushed a high level is seen on one of the row inputs, the oscillator starts and the keyboard scan logic turns on. The active pull-up or pull-down resistors are selectively switched on and off as the keyboard scan logic determines the row and the column inputs that are selected. The advantage of the scanning technique is that a keyboard arrangement of SPST switches are shown in Figure 2 without the need for a common line, can be used. Conventional telephone push button keyboards as shown in Figure 1 or X-Y keyboards with common can also be used. The common line of these keyboards can be left unconnected or wired "high".

Logic Interface

The S2559 can also interface with CMOS logic outputs directly. The S2559 requires active "High" logic levels. Since the active pull-up resistors present in the S2559 are fairly low value (500Ω typ), diodes can be used as shown in Figure 3 to eliminate excessive sink current flowing into the logic outputs in their "Low" state.

Tone Generation

When a valid key closure is detected, the keyboard logic programs the high and low group dividers with appropriate divider ratios so that the output of these dividers cycle at 16 times the desired high group and low group frequencies. The outputs of the programmable dividers drive two 8-stage Johnson counters. The symmetry of the clock input to the two divide by 16 Johnson counters allows 32 equal time segments to be generated within each output cycle. The 32 segments are used to digitally synthesize a stair-step waveform to approximate the sinewave function (see Figure 3). This is done by connecting a weighted resistor ladder network between the outputs of the Johnson counter, V_{DD} and V_{REF}. V_{REF} closely tracks V_{DD} over the operating voltage and temperature range and therefore the peak-to-peak amplitude V_P ($V_{DD} - V_{REF}$) of the stairstep function is fairly constant. V_{REF} is so chosen that V_P falls within the allowed range of the high group and low group tones.

Figure 1. Standard Telephone Push Button Keyboard

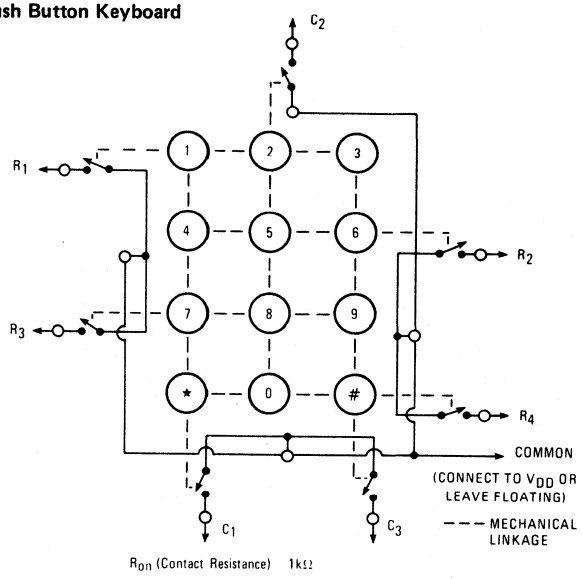


Figure 2. SPST Matrix Keyboard Arranged in the 2 of 8 Row, Column Format

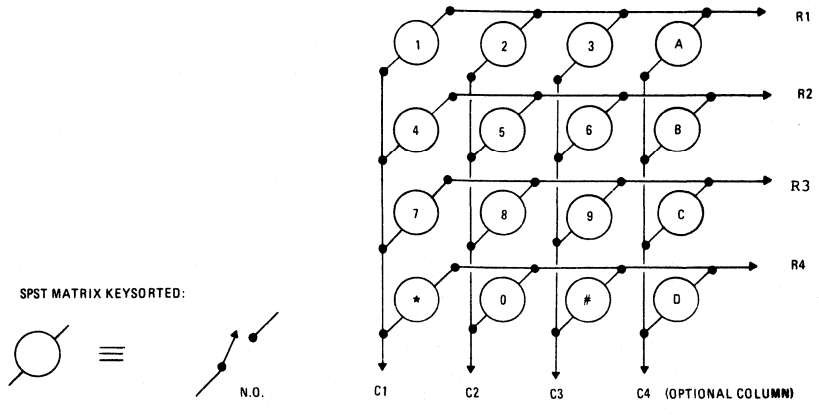
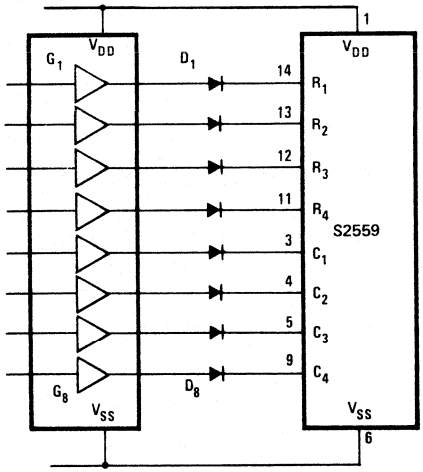
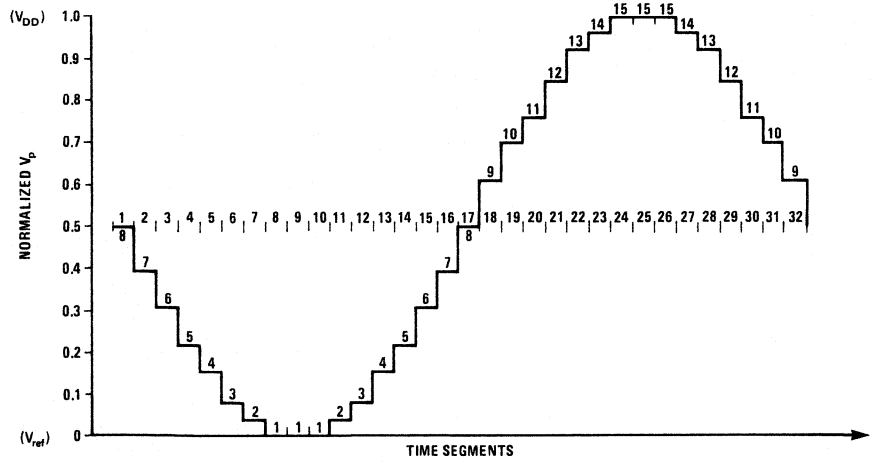


Figure 3. Logic Interface for Keyboard Inputs of the S2559



G1 THRU G8 ANY TYPE CMOS GATE
D1 THRU D8 DIODES TYPE IN914 (OPTIONAL)

Figure 4. Stairstep Waveform of the Digitally Synthesized Sinewave



The individual tones generated by the sinewave synthesizer are then linearly added and drive a bipolar NPN transistor connected as emitter follower to allow proper impedance transformation, at the same time preserving signal level.

Dual Tone Mode

When one row and one column is selected dual tone output consisting of an appropriate low group and high group tone is generated. If two digit keys, that are not either in the same row or in the same column, are depressed, the dual tone mode is disabled and no output is provided.

Single Tone Mode

Single tones either in the low group or the high group can be generated as follows. A low group tone can be generated by activating the appropriate row input or by depressing two digit keys in the appropriate row. A high group tone can be generated by depressing two digit keys in the appropriate column, i.e., selecting the appropriate column input and two row inputs in that column.

Mode Select

S2559A and S2559C have a Mode Select (MDSL) input (Pin 15). When MDSL is left floating (unconnected) or connected to V_{DD}, both the dual tone and single tone modes are available. If MDSL is connected to V_{SS}, the single tone mode is disabled and no output tone is produced if an attempt for single tone is made. The S2559B and S2559D do not have the Mode Select option.

Chip Disable

The S2559B and S2559D have a Chip Disable input at Pin 15 instead of the Mode Select input. The chip disable for the S2559B and S2559D is active "high." When the chip disable is active, the tone output goes to V_{SS}, the row, column inputs go into a high impedance state, the oscillator is inhibited and the MUTE and XMIT outputs go into active states. The effect is the device essentially disconnects from the keyboard. This allows one keyboard to be shared among several devices.

Crystal Specification

A standard television color burst crystal is specified to have much tighter tolerance than necessary for tone generation application. By relaxing the tolerance specification the cost of the crystal can be reduced. The recommended crystal specification is as follows:

Frequency: 3.579545MHz ±0.02%
$R_S \leq 100\Omega$, L_M = 96MHY
C_M = 0.02pF C_h = 5pF

MUTE, XMIT Outputs

The S2559 A, B, C, D have a CMOS buffer for the MUTE output and a bipolar NPN transistor for the XMIT output. With no keys depressed, the MUTE output is "low" and the XMIT output is in the active state so that substantial current can be sourced to a load. When a key is depressed, the MUTE output goes high, while the XMIT output goes into a high impedance state. When Chip Disable is "high" the MUTE output is forced "low" and the XMIT output is in active state regardless of the state of the keyboard inputs.

Amplitude/Distortion Measurements

Amplitude and distortion are two important parameters in all applications of the Digital Tone Generator. Amplitude depends upon the operating supply voltage as well as the load resistance connected on the Tone Output pin. The on-chip reference circuit is fully operational when the supply voltage equals or exceeds 5 volts and as a consequence the tone amplitude is regulated in the supply voltage range above 5 volts. The load resistor value also controls the amplitude. If R_L is low the reflected impedance into the base of the output transistor is low and the tone output amplitude is lower. For R_L greater than 5KΩ the reflected impedance is sufficiently large and highest amplitude is produced. Individual tone amplitudes can be measured by applying the dual tone signal to a wave analyzer (H-P type 3581A) and amplitudes at the selected frequencies can be noted. This measurment also permits verification of the preemphasis between the individual frequency tones.

Distortion is defined as "the ratio of the *total* power of all extraneous frequencies in the *voiceband* above 500Hz accompanying the signal to the power of the frequency *pair*." This ratio must be less than 10% or when expressed in dB must be lower than −20dB. (Ref. 1.) Voiceband is conventionally the frequency band of 300Hz to 3400Hz. Mathematically distortion can be expressed as:

$$\text{Dist.} = \frac{\sqrt{(V_1)^2+(V_2)^2+\ldots+(V_n)^2}}{\sqrt{(V_L)^2+(V_H)^2}}$$

where $(V_1) \ldots (V_n)$ are extraneous frequency (i.e., intermodulation and harmonic) components in the 500Hz to 3400Hz band and V_L and V_H are the individual frequency components of the DTMF signal. The expression can be expressed in dB as:

$$DIST_{dB} = 20 \log \frac{\sqrt{(V_1)^2+(V_2)^2+\ldots(V_n)^2}}{\sqrt{(V_L)^2+(V_H)^2}}$$

$$= 10\left\{\log\left[(V_1)^2+\ldots(V_n)^2\right] - \log\left[(V_L)^2+(V_H)^2\right]\right\} \ldots (1)$$

An accurate way of measuring distortion is to plot a spectrum of the signal by using a spectrum analyzer (H-P type 3580A) and an X-Y plotter (H-P type 7046A). Individual extraneous and signal frequency components are then noted and distortion is calculated by using the expression (1) above. Figure 6 shows a spectrum plot of a typical signal obtained from a S2559D device operating from a fixed supply of 4Vdc and R_L = 10kΩ in the test circuit of Figure 5. Mathematical analysis of the spectrum shows distortion to be −30dB (3.2%). For quick estimate of distortion, a rule of thumb as outlined below can be used.

"As a first approximation distortion in dB equals the difference between the amplitude (dB) of the extraneous component that has the highest amplitude and the amplitude (dB) of the low frequency signal." This rule of thumb would give an estimate of -28dB as distortion for the spectrum plot of Figure 6 which is close to the computed result of −30dB.

In a telephone application amplitude and distortion are affected by several factors that are interdependent. For detailed discussion of the telephone application and other applications of the 2559 Tone Generator, refer to the applications note "Applications of Digital Tone Generator."

Ref. 1: *Bell System Communications Technical Reference, PUB 47001*, "Electrical Characteristics of Bell System Network Facilities at the Interface with Voiceband Ancillary and Data Equipment," August 1976.

Figure 5. Test Circuit for Distortion Measurement

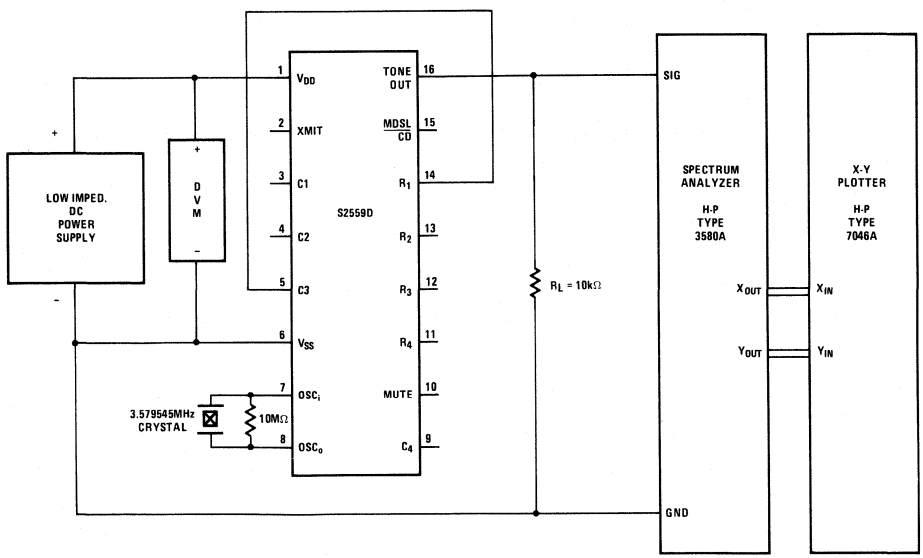
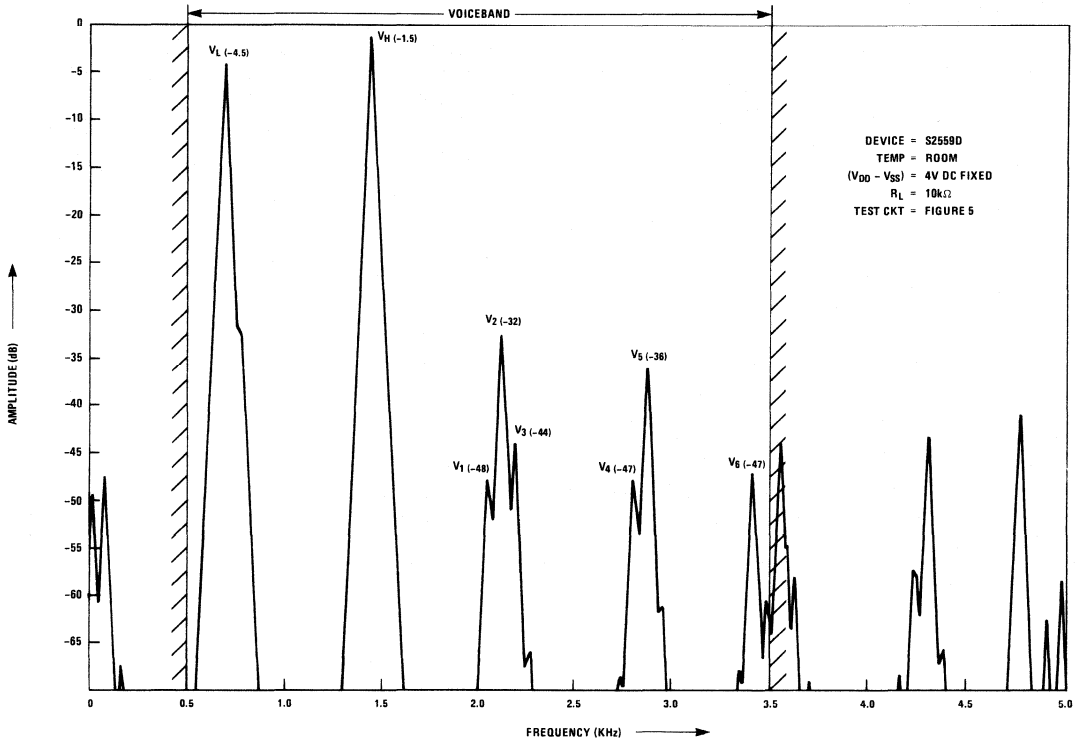


Figure 6. A Typical Spectrum Plot



DTMF TONE GENERATOR

Features

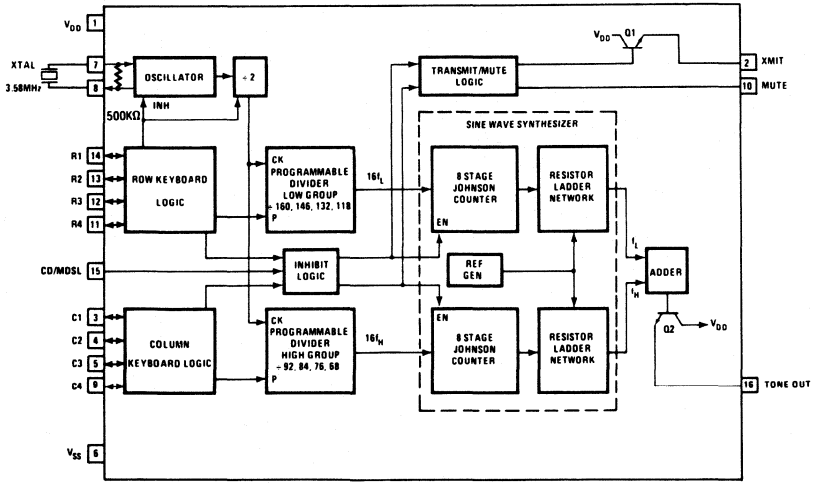
- ☐ Low Output Tone Distortion: 7%
- ☐ Wide Operating Supply Voltage Range: 2.5 to 10 Volts
- ☐ Oscillator Bias Resistor On-Chip
- ☐ Can be Powered Directly from Telephone Line or from Small Batteries
- ☐ Interfaces Directly to a Standard Telephone Push-Button or Calculator Type X-Y Keyboard
- ☐ Four Options Available on Pin 15:
  - Bipolar Output
    - E: Mode Select
    - F: Chip Disable
  - Darlington Output
    - G: Mode Select
    - H: Chip Disable

General Description

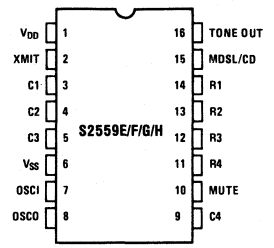
The S2559E, F, G and H are improved members of the S2559 Tone Generator Family. The new devices feature extended operating voltage range, lower tone distortion, and an on-chip oscillator bias resistor. The S2559E and F are pin and functionally compatible with the S2559C and D, respectively.

The S2559 G and H are identical to the E and F, except that there is a Darlington amplifier configuration on the tone out pin, rather than a single bipolar transistor as shown in the block diagram. In many applications this eliminates the need for a transistor in the telephone circuit. Tone distortion in the telephone is also likely to be lower.

Block Diagram



Pin Configuration



Absolute Maximum Ratings

DC Supply Voltage V_{DD}	+6.0V
DC Supply Voltage V_{SS}	−6.0V
Operating Temperature	−20°C to +70°C
Storage Temperature	−55°C to +125°C
Power Dissipation at 25°C	1000mW
Digital Input	$V_{SS}-0.3 \leq V_{IN} \leq V_{DD}+0.3$
Analog Input	$V_{SS}-0.3 \leq V_{IN} \leq V_{DD}+0.3$

S2559E, F, G and H Electrical Characteristics:

(Specifications apply over the operating temperature range of −25°C to +70°C unless otherwise noted. Absolute values of measured parameters are specified.)

Symbol	Parameter/Conditions		($V_{DD}-V_{SS}$) Volts	Min.	Typ.	Max.	Units
	Supply Voltage						
V_{DD}	Tone Out Mode (Valid Key Depressed)			2.5		10.0	V
	Non Tone Out Mode (No Key Depressed)			1.6		10.0	V
	Supply Current						
I_{DD}	Standby (No Key Selected, Tone, XMIT and MUTE Outputs Unloaded)		3.0		0.3	30	μA
			10.0		1.0	100	μA
	Operating (One Key Selected, Tone, XMIT and MUTE Outputs Unloaded)		3.0		1.0	2.0	mA
			10.0		8	16.0	mA
	Tone Output						
S2559E/F V_{OR}	Single Tone Mode Output Voltage	Row Tone, R_L=390Ω	3.5	335	465	565	mVrms
			5.0	365	525	695	mVrms
		Row Tone, R_L=240Ω	10.0	365	535	720	mVrms
S2559G/H V_{OR}	Single Tone Mode Output Voltage	Row Tone, R_L=390Ω	3.5	110	315	495	mVrms
			5.0	325	525	660	mVrms
		Row Tone, R_L=240Ω	10.0	400	575	755	mVrms
dB_{CR}	Ratio of Column to Row Tone		3.5−10.0	1.0	2.0	3.0	dB
%DIS	Distortion*	2559E/F	3.5−10.0			7	%
		2559G/H	4.0−10.0			7	%
	XMIT, MUTE Outputs						
V_{OH}	XMIT, Output Voltage, High (No Key Depressed)(Pin 2)	(I_{OH}=15mA)	3.0	1.5	1.8		V
		(I_{OH}=50mA)	10.0	8.5	8.8		V
I_{OF}	XMIT, Output Source Leakage Current, V_{OF}=0V		10.0			100	μA
V_{OL}	MUTE (Pin 10) Output Voltage, Low, (No Key Depressed), No Load		2.75		0	0.5	V
			10.0		0	0.5	V
V_{OH}	MUTE, Output Voltage, High, (One Key Depressed) No Load		2.75	2.5	2.75		V
			10.0	9.5	10.0		V
I_{OL}	MUTE, Output Sink Current	V_{OL}=0.5V	3.0	0.53	1.3		mA
			10.0	2.0	5.3		mA
I_{OH}	MUTE, Output Source Current	V_{OH}=2.5V	3.0	0.17	0.41		mA
		V_{OH}=9.5V	10.0	0.57	1.5		mA

**Distortion is defined as "the ratio of the total power of all extraneous frequencies, in the VOICE and above 500Hz, to the total power of the DTMF frequency pair".*

S2559E, F, G and H Electrical Characteristics (Continued)

Symbol	Parameter/Conditions		($V_{DD}-V_{SS}$) Volts	Min.	Typ.	Max.	Units
	Oscillator Input/Output						
I_{OL}	Output Sink Current	V_{OL}=0.5V	3.0	0.21	0.52		mA
	One Key Selected	V_{OL}=0.5V	10.0	0.80	2.1		mA
I_{OH}	Output Source Current	V_{OH}=2.5V	3.0	0.13	0.31		mA
	One Key Selected	V_{OH}=9.5V	10.0	0.42	1.1		mA
	Input Current						
I_{IL}	Leakage Sink Current, One Key Selected	V_{IL}=10.0V	10.0			1.0	μA
I_{IH}	Leakage Source Current One Key Selected	V_{IH}=0.0V	10.0			1.0	μA
I_{IL}	Sink Current	V_{IL}=0.5V	3.0	47	93		μA
	No Key Selected	V_{IL}=0.5V	10.0	65	130		μA
t_{START}	Oscillator Startup Time		3.5		2	5	ms
			10.0		0.25	4	ms
$C_{I/O}$	Input/Output Capacitance		3.0		12	16	pF
			10.0		10	14	pF

AMERICAN MICROSYSTEMS, INC.

ADVANCED PRODUCT DESCRIPTION

S25089

DTMF GENERATOR

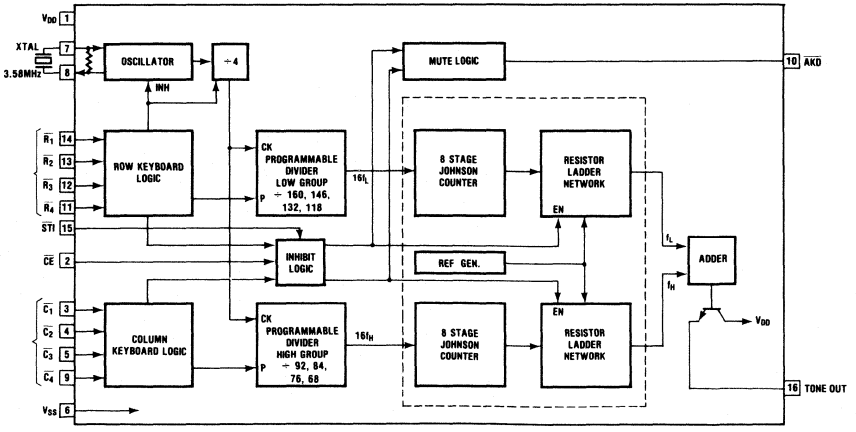
Features

- ☐ Wide Operating Voltage Range: 2.5 to 10 Volts
- ☐ Optimized for Constant Operating Supply Voltages, Typically 3.5V
- ☐ Tone Amplitude Stability is Within ±1.5dB of Nominal Over Operating Temperature Range
- ☐ Low Power CMOS Circuitry Allows Device Power to be Derived Directly From the Telephone Lines or From Small Batteries
- ☐ Uses TV Crystal Standard (3.58MHz) to Derive All Frequencies Thus Providing Very High Accuracy and Stability
- ☐ Specifically Designed for Electronic Telephone Applications
- ☐ Interfaces Directly to a Standard Telephone Push-Button Keyboard With Common Terminal
- ☐ Low Total Harmonic Distortion
- ☐ Dual Tone as Well as Single Tone Capability
- ☐ Direct Replacement for Mostek MK5089 Tone Generator

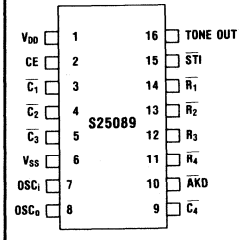
General Description

The S25089 DTMF Generator is specifically designed to implement a dual tone telephone dialing system in applications requiring fixed supply operation and high stability tone output level, making it well suited for electronic telephone applications. The device can interface directly to a standard pushbutton telephone keyboard with common terminal connected to V_{SS} and operates directly from the telephone lines. All necessary dual-tone frequencies are derived from the widely used TV crystal standard providing very high accuracy and stability. The required sinusoidal waveform for the individual tones is digitally synthesized on the chip. The waveform so generated has very low total harmonic distortion. A voltage reference is generated on the chip which is very stable over the operating temperature range and regulates the signal levels of the dual tones to meet the recommended telephone industry specifications.

Block Diagram



Pin Configuration



Absolute Maximum Ratings:

DC Supply Voltage (V_{DD}-V_{SS}) ..... +10.5V
Operating Temperature ..... −25°C to +70°C
Storage Temperature ..... −65°C to +150°C
Power Dissipation at 25°C 500mW
Input Voltage ..... $-0.6 \leq V_{IN} \leq V_{DD}$ +0.6
Input/Output Current (except tone output) 15mA
Tone Output Current 50mA

Electrical Characteristics:

(Specifications apply over the operating temperature range of −25°C to 70°C unless otherwise noted. Absolute values of measured parameters are specified.)

Symbol	Parameter/Conditions			(V_{DD}-V_{SS}) Volts	Min.	Typ.	Max.	Units
	Supply Voltage							
V_{DD}	Tone Out Mode (Valid Key Depressed)				2.5	—	10.0	V
	Non Tone Out Mode ($\overline{AKD}$ Outputs toggle with key depressed)				1.8	—		V
	Supply Current							
I_{DD}	Standby (No Key Selected, Tone and $\overline{AKD}$ Outputs Unloaded)			3.0 10.0	— —	1 5	20 100	μA μA
	Operating (One Key Selected, Tone and $\overline{AKD}$ Outputs Unloaded)			3.0 10.0	— —	.9 3.6	1.25 5	mA mA
	Tone Output							
V_{OR}	Dual Tone	Row	R_L=10kΩ	3.0	−11.0		−8.0	dB
	Mode Output	Tone	R_L=100kΩ	3.5	−10.0		−7.0	dB
dB_{CR}	Ratio of Column to Row Tone			2.5-10.0	2.4	2.7	3.0	dB
%DIS	Distortion*			2.5-10.0	—	—	10	%
NKD	Tone Output—No Key Down						−80	dBm
	$\overline{AKD}$ Output							
I_{OL}	Output On Sink Current		V_{OL}=0.5V	3.0	0.1	1.0	—	mA
I_{OH}	Output Off Leakage Current			10.00		1	10	μA
	OSCILLATOR Input/Output							
I_{OL}	One Key Selected		V_{OL}=0.5V	3.0	0.21	0.52	—	mA
	Output Sink Current		V_{OL}=0.5V	10.0	0.80	2.1	—	mA
I_{OH}	Output Source Current		V_{OH}=2.5V	3.0	0.13	0.31	—	mA
	One Key Selected		V_{OH}=9.5V	10.0	0.42	1.1	—	mA
I_{IL}	Input Current Leakage Sink Current One Key Selected		V_{IL}=10.0V	10.0	—	—	1.0	μA
I_{IH}	Leakage Source Current One Key Selected		V_{IH}=0.0V	10.0	—	—	1.0	μA
I_{IL}	Sink Current		V_{IL}=0.5V	3.0	24	58	—	μA
	No Key Selected		V_{IL}=0.5V	10.0	27	66	—	μA

*Distortion measured in accordance with the specifications described in REF. 1 as the "ratio of the total power of all extraneous frequencies in the voiceband above 500Hz accompanying the signal to the total power of the frequency pair".

Electrical Characteristics: (Continued)

Symbol	Parameter/Conditions		(V_{DD}-V_{SS}) Volts	Min.	Typ.	Max.	Units
	OSCILLATOR Input/Output (Continued)						
t_{START}	Oscillator Startup Time with Crystal as Specified		3.4 10.0	— —	2 0.25	4 0.75	ms ms
$C_{I/O}$	Input/Output Capacitance		3.0 10.0	— —	12 10	16 14	pF pF
	Row, Column and Chip Enable Inputs						
V_{IL}	Input Voltage, Low		—	$V_{SS}-0.6$		$.2(V_{DD}-V_{SS})$	V
V_{IH}	Input Voltage, High		—	$.8(V_{DD}-V_{SS})$	—	$V_{DD}+0.6$	V
I_{IH}	Input Current	$V_{IH}=0.0V$	3.0	30	90	150	μA
	(Pull up)	$V_{IH}=0.0V$	10.0	100	300	500	μA

Oscillator

The S25089 contains an oscillator circuit with the necessary parasitic capacitances and feedback resistor on chip so that it is only necessary to connect a standard 3.58MHz TV crystal across the OSC_i and OSC_0 terminals to implement the oscillator function. The oscillator functions whenever a row input is activated. The reference frequency is divided by 4 and then drives two sets of programmable dividers, the high group and the low group.

Crystal Specification

A standard television color burst crystal is specified to have much tighter tolerance than necessary for tone generation application. By relaxing the tolerance specification the cost of the crystal can be reduced. The recommended crystal specification is as follows:

Frequency: 3.579545MHz ±0.02%
R_S 100Ω, $L_M=96MH_Y$
$C_M=0.02pF$ $C_H=5pF$ $C_L=12pF$

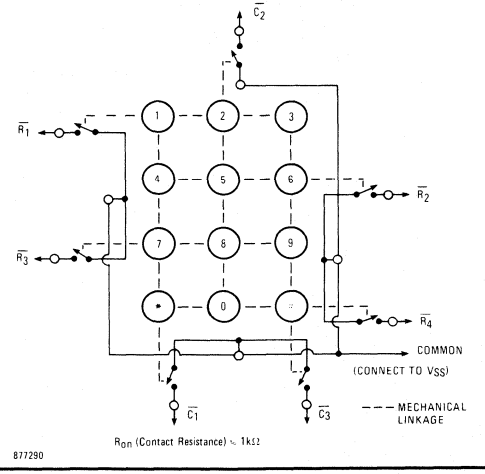
Keyboard Interface

The S25089 can interface with the standard telephone pushbutton keyboard (see Figure 1) with common. The common of the keyboard must be connected to V_{SS}.

Logic Interface

The S25089 can also interface with CMOS logic outputs directly (see Figure 2). The S25089 requires active "Low" logic levels. Low levels on a row and a column input corresponds to a key closure. The pull-up resistors present on the row and column inputs are in the range of 20kΩ -100kΩ.

Figure 1. Standard Telephone Push Button Keyboard



Tone Generation

When a valid key closure is detected, the keyboard logic programs the high and low group dividers with appropriate divider ratios so that the output of these dividers cycle at 16 times the desired high group and low group

frequencies. The outputs of the programmable dividers drive two 8-stage Johnson counters. The symmetry of the clock input to the two divided by 16 Johnson counters allows 32 equal time segments to be generated within each output cycle. The 32 segments are used to digitally synthesize a stair-step waveform to approximate the sinewave function (see Figure 3). This is done by connecting a weighted resistor ladder network between the outputs of the Johnson counter, V_{DD} and V_{REF}. V_{REF} closely tracks V_{DD} over the operating voltage and temperature range and therefore the peak-to-peak amplitude VP (V_{DD}-V_{REF}) of the stair-step function is fairly constant. V_{REF} is so chosen that VP falls within the allowed range of the high group and low group tones.

The individual tones generated by the sinewave synthesizer are then linearly added and drive an NPN transistor connected as an emitter follower to allow proper impedance transformation at the same time preserving signal level. This allows the device to drive varying resistive loads without significant variation in tone amplitude. For example, a load resistor change from 10kΩ to 1kΩ causes a decrease in tone amplitude of less than 1dB.

Dual Tone Mode

When one row and one column is selected, dual tone output consisting of an appropriate low group and high group tone is generated. If two digit keys that are not either in the same row or in the same column are depressed, the dual tone mode is disabled and no output is provided.

Single Tone Mode

Single tones either in the low group or the high group can be generated as follows. A low group tone can be generated by depressing two digit keys in the appropriate row. A high group tone can be generated by depressing two digit keys in the appropriate column, i.e., selecting the appropriate column input and two row inputs in that column.

Inhibiting Single Tones

The $\overline{STI}$ input (pin 15) is used to inhibit the generation of other than dual tones. It has an internal pull down to V_{SS} supply. When this input is left unconnected or connected to V_{SS}, single tone generation as described in the preceding paragraph (Single Tone Mode) is suppressed with all other functions operating normally. When this input is connected to V_{DD} supply, single or dual tones may be generated as previously described (Single Tone Mode, Dual Tone Mode).

Chip Enable Input (CE, Pin 2)

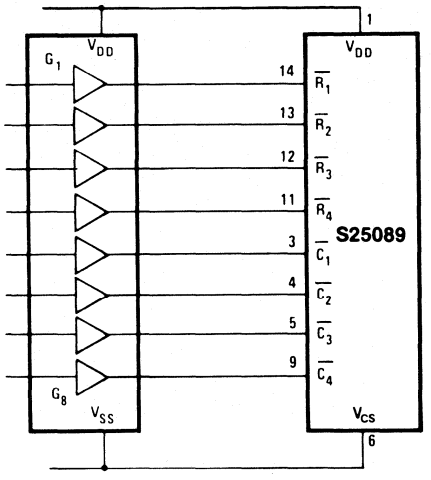
The chip enable input has an internal pull-up to V_{DD} supply. When this pin is left unconnected or connected to V_{DD} supply the chip operates normally. When connected to V_{SS} supply, tone generation is inhibited. All other chip functions operate normally. With a load resistor connected to the tone output pin (pin 16) the voltage level on this output will be at V_{SS} in this mode.

Table 1. Comparison of Specified Vs. Actual Tone Frequencies Generated by S25089

ACTIVE INPUT	OUTPUT FREQUENCY Hz		%ERROR SEE NOTE
	SPECIFIED	ACTUAL	
R1	697	699.1	+0.30
R2	770	766.2	−0.49
R3	852	847.4	−0.54
R4	941	948.0	+0.74
C1	1209	1215.9	+0.57
C2	1336	1331.7	−0.32
C3	1477	1471.9	−0.35
C4	1633	1645.0	+0.73

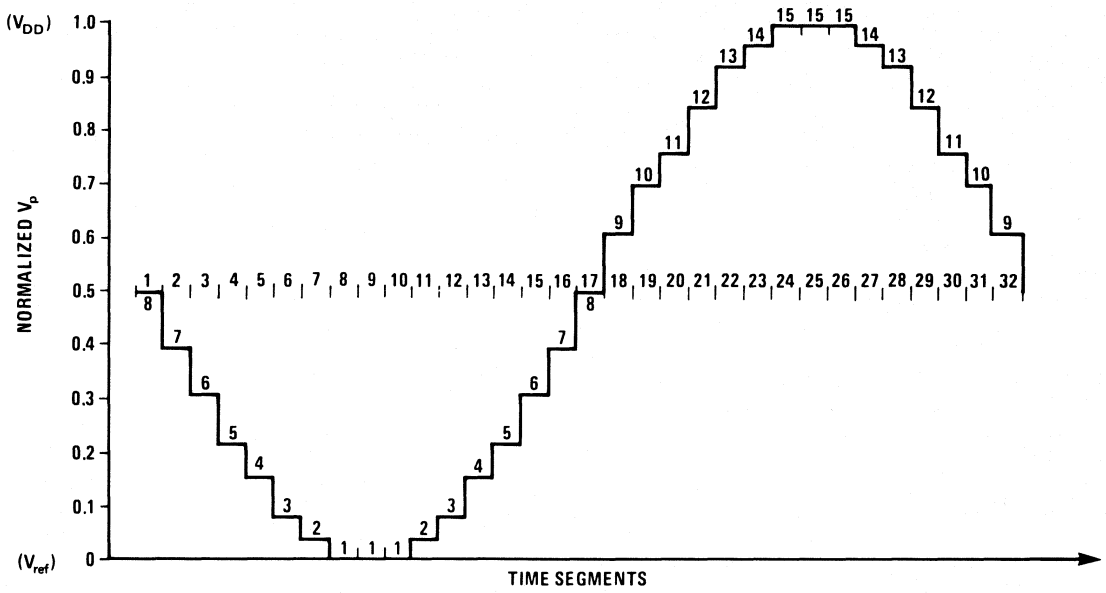
NOTE: %ERROR DOES NOT INCLUDE OSCILLATOR DRIFT

Figure 2. Logic Interface for Keyboard Inputs of the S25089



G1 THRU G8 ANY TYPE CMOS GATE

Figure 3. Stairstep Waveform of the Digitally Synthesized Sinewave



Reference Voltage

The structure of the reference voltage employed in the S25089 is shown in Figure 4. It has the following characteristics:

a) V_{REF} is proportional to the supply voltage. Output tone amplitude, which is a function of (V_{DD} - V_{REF}), increases with supply voltage (Figure 5).
b) The temperature coefficient of V_{REF} is low due to a single V_{BE} drop. Use of a resistive divider also provides an accuracy of better than 1%. As a result, tone amplitude variations over temperature and unit to unit are held to less than ±1.0dB over nominal.
c) Resistor values in the divider network are so chosen that V_{REF} is above the V_{BE} drop of the tone output transistor even at the low end of the supply voltage range. The tone output clipping at low supply voltages is thus eliminated, which improves distortion performance.

$\overline{AKD}$ (Any Key Down or Mute) Output

The $\overline{AKD}$ output (pin 10) consists of an open drain N channel device (see Figure 6.) When no key is depressed the $\overline{AKD}$ output is open. When a key is depressed the $\overline{AKD}$ output goes to V_{SS}. The device is large enough to sink a minimum of 100μA with voltage drop of 0.2V at a supply voltage of 3.5V.

Figure 4. Structure of the Reference Voltage

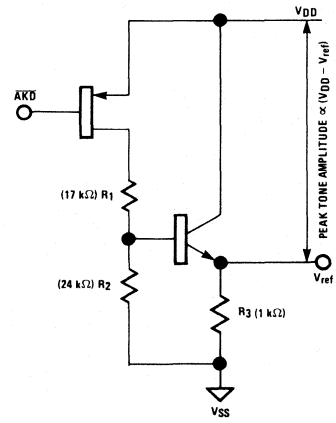


Figure 5. Typical Tone Output Amplitude Vs Supply Voltage ($R_L = 10k$)

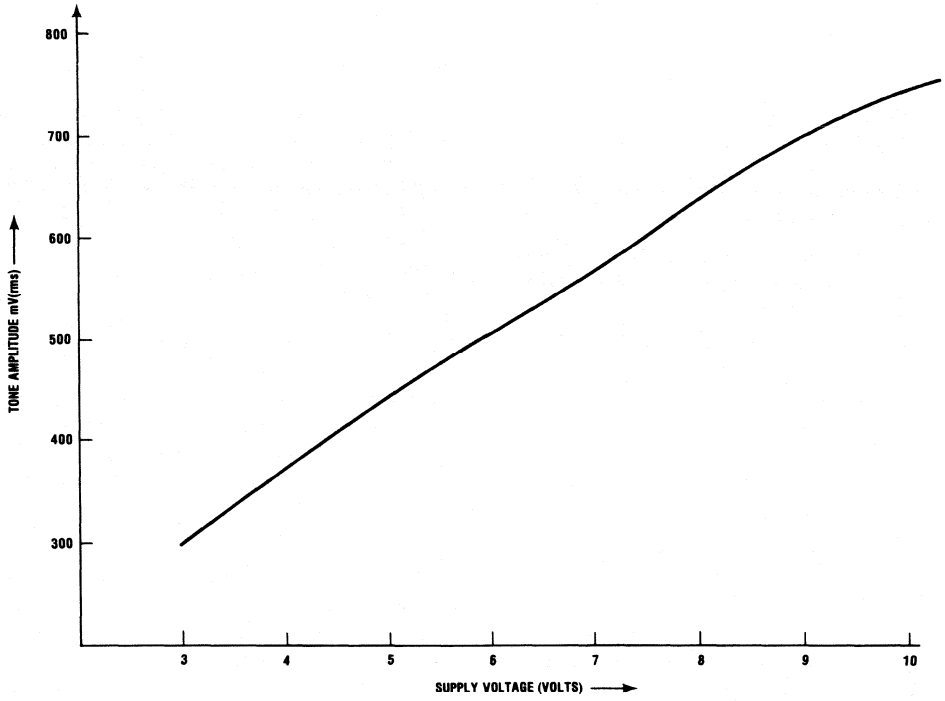
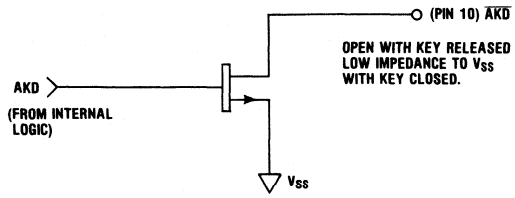


Figure 6. $\overline{AKD}$ Output Structure



AMERICAN MICROSYSTEMS, INC.

S2859

DIGITAL TONE GENERATOR

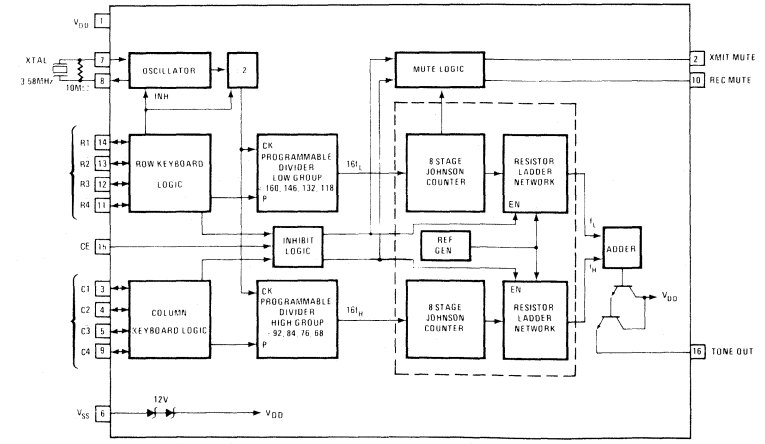
Features

- ☐ **Wide Operating Supply Voltage Range: 3.0 to 10 Volts**
- ☐ **Low Power CMOS Circuitry Allows Device Power to be Derived Directly from the Telephone Lines or from Small Batteries, e.g., 9V**
- ☐ **Uses TV Crystal Standard (3.58 MHz) to Derive all Frequencies thus Providing Very High Accuracy and Stability**
- ☐ **Timing Sequence for XMIT, REC MUTE Outputs**
- ☐ **Interfaces Directly to a Standard Telephone Push-Button or Calculator Type X-Y Keyboard with Common Terminal**
- ☐ **The Total Harmonic Distortion is Below Industry Specification**
- ☐ **On Chip Generation of a Reference Voltage to Assure Amplitude Stability of the Dual Tones Over the Operating Voltage and Temperature Range**
- ☐ **Dual Tone as Well as Single Tone Capability**
- ☐ **Darlington Configuration Tone Output**

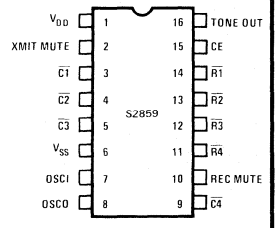
General Description

The S2859 Digital Tone Generator is specifically designed to implement a dual tone telephone dialing system. The device can interface directly to a standard pushbutton telephone keyboard or X-Y keyboard with common terminal connected to V_{SS} and operates directly from the telephone lines. All necessary dual-tone frequencies are derived from the widely used TV crystal standard providing very high accuracy and stability. The required sinusoidal waveform for the individual tones is digitally synthesized on the chip. The waveform so generated has very low total harmonic distortion. A voltage reference is generated on the chip which is stable over the operating voltage and temperature range and regulates the signal levels of the dual tones to meet the recommended telephone industry specifications. These features permit the S2859 to be incorporated with a slight modification of the standard 500 type telephone basic circuitry to form a pushbutton dual-tone telephone. Other applications of the device include radio and mobile telephones, remote control, point-of-sale, and credit card verification terminals and process control.

Block Diagram



Pin Configuration



Absolute Maximum Ratings:

DC Supply Voltage ($V_{DD}-V_{SS}$)	+10.5V
Operating Temperature	−25 °C to +70 °C
Storage Temperature	−55 °C to +125 °C
Power Dissipation at 25 °C	500mW
Input Voltage	$-0.6 \leq V_{IN} \leq V_{DD}+0.6$
Input/Output Current (except tone output)	15mA
Tone Output Current	50mA

Electrical Characteristics:

(Specifications apply over the operating temperature range of −25 °C to 70 °C unless otherwise noted. Absolute values of measured parameters are specified.)

Symbol	Parameter/Conditions			($V_{DD}-V_{SS}$) Volts	Min.	Typ.	Max.	Units
	Supply Voltage							
V_{DD}	Tone Out Mode (Valid Key Depressed)				3.0	—	10.0	V
	Non Tone Out Mode (Mute Outputs Toggle With Key Depressed)				2.2	—	10.0	V
V_Z	Internal Zener Diode Voltage, I_Z = 5mA			—	—	12.0	—	V
	Supply Current							
I_{DD}	Standby (No Key Selected,			3.0	—	0.001	0.3	mA
	Tone and Mute Outputs Unloaded)			10.0	—	0.003	1.0	mA
	Operating (One Key Selected,			3.0	—	1.3	2.0	mA
	Tone and Mute Outputs Unloaded)			10.0	—	11	18	mA
	Tone Output							
V_{OR}	Single Tone	Row	R_L=100Ω	5.0	366	462	581	mVrms
	Mode Output Voltage	Tone	R_L=100Ω	10.0	370	482	661	mVrms
dB_{CR}	Ratio of Column to Row Tone			3.0−10.0	1.0	2.0	3.0	dB
%DIS	Distortion*			3.0−10.0	—	—	10	%
	REC, XMIT MUTE Outputs							
I_{OH}	Output Source Current		V_{OH}=1.2V	2.2	0.43	1.1	—	mA
			V_{OH}=2.5V	3.0	1.3	3.1	—	mA
			V_{OH}=9.5V	10.0	4.3	11	—	mA

**Distortion measured in accordance with the specifications described in Ref. 1 as the "ratio of the total power of all extraneous frequencies in the voiceband above 500Hz accompanying the signal to the total power of the frequency pair".*

Electrical Characteristics: (Continued)

Symbol	Parameter/Conditions		(V_{DD} – V_{SS}) Volts	Min.	Typ.	Max.	Units
	OSCILLATOR Input/Output						
I_{OL}	One Key Selected	V_{OL} = 0.5V	3.0	0.21	0.52	–	mA
	Output Sink Current	V_{OL} = 0.5V	10.0	0.80	2.1	–	mA
I_{OH}	Output Source Current	V_{OH} = 2.5V	3.0	0.13	0.31	–	mA
	One Key Selected	V_{OH} = 9.5V	10.0	0.42	1.1	–	mA
I_{IL}	Input Current Leakage Sink Current One Key Selected	V_{IL} = 10.0V	10.0	–	–	1.0	μA
I_{IH}	Leakage Source Current One Key Selected	V_{IH} = 0.0V	10.0	–	–	1.0	μA
I_{IL}	Sink Current	V_{IL} = 0.5V	3.0	24	58	–	μA
	No Key Selected	V_{IL} = 0.5V	10.0	27	66	–	μA
t_{START}	Oscillator Time		3.0 10.0	– –	2 0.25	5 0.75	ms ms
$C_{I/O}$	Input/Output Capacitance		3.0 10.0	– –	12 10	16 14	pF pF
	Row, Column and Chip Enable Inputs						
V_{IL}	Input Voltage, Low		3.0 10.0	– –	– –	0.75 3.0	V V
V_{IH}	Input Voltage, High		3.0 10.0	2.4 7.0		– –	V V
I_{IH}	Input Current	V_{IH} = 0.0V	3.0	20	60	100	μA
	(Pull up)	V_{IH} = 0.0V	10.0	66	200	336	μA

Circuit Description

The S2859 is designed so that it can be interfaced easily to the dual tone signaling telephone system and that it will more than adequately meet the recommended telephone industry specifications regarding the dual tone signaling scheme.

Design Objectives

The specifications that are important to the design of the Digital Tone Generator are summarized below: the dual tone signal consists of linear addition of two voice frequency signals. One of the two signals is selected from a group of frequencies called the "Low Group" and the other is selected from a group of frequencies called the "High Group". The low group consists of four frequencies 697, 770, 852 and 941 Hz. The high group consists of four frequencies 1209, 1336, 1477 and 1633 Hz. A keyboard arranged in a row, column format (4 rows x 3 or 4 columns) is used for number entry. When a push button corresponding to a digit (0 thru 9) is pushed, one appropriate row (R1 thru R4) and one appropriate column (C1 thru C4) is selected. The active row input selects one of the low group frequencies and the active column input selects one of the high group frequencies. In standard dual tone telephone systems, the highest high group frequency of 1633Hz (Col. 4) is not used. The frequency tolerance must be ±1.0%. However, the S2859 provides a better than .75% accuracy. The total harmonic and intermodulation distortion of the dual tone must be less than 10% as seen at the telephone terminals. (Ref. 1.) The high group to low group signal amplitude ratio should be 2.0 ±2dB and the absolute amplitude of the low group and high group tones must be within the allowed range. (Ref. 1.) These requirements apply when the telephone is used over a short loop or long loop and over the operating temperature range. The design of the S2859 takes into account these considerations.

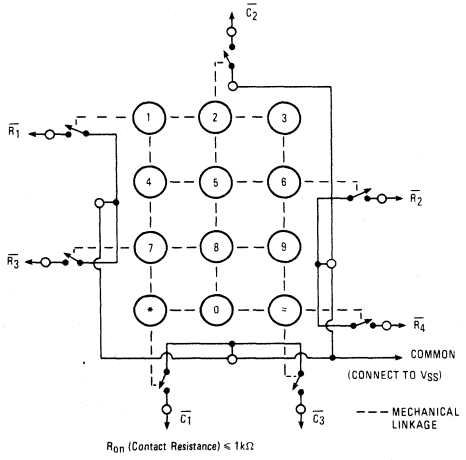
Oscillator

The device contains an oscillator circuit with the necessary parasitic capacitances on chip so that it is only necessary to connect a 10MΩ feedback resistor and the standard 3.58MHz TV crystal across the OSCI and OSCO terminals to implement the oscillator function. The oscillator functions whenever a row input is activated. The reference frequency is divided by 2 and then drives two sets of programmable dividers, the high group and the low group.

Keyboard Interface

The S2859 can interface with either the standard telephone pushbutton keyboard (see Figure 1) or an X-Y keyboard with common. The common of the keyboard must be connected to V_{SS}.

Figure 1. Standard Telephone Push Button Keyboard



Logic Interface

The S2859 can also interface with CMOS logic ouputs directly. (See Figure 2.) The S2859 requires active "Low" logic levels. Low levels on a row and a column input corresponds to a key closure. The pull-up resistors present on the row and column inputs are in the range of 33kΩ — 150kΩ.

Tone Generation

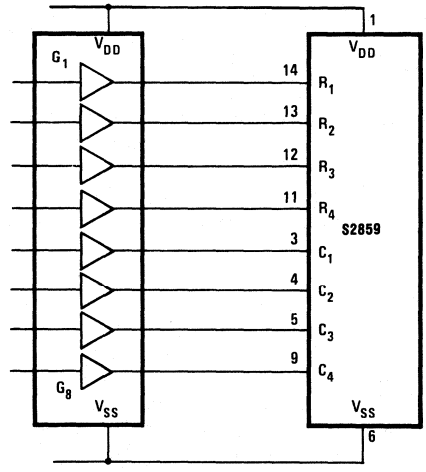
When a valid key closure is detected, the keyboard logic programs the high and low group dividers with appropriate divider ratios so that the output of these dividers cycle at 16 times the desired high group and low group frequencies. The outputs of the programmable dividers drive two 8-stage Johnson counters. The symmetry of the clock input to the two divide by 16 Johnson counters allows 32 equal time segments to be generated within each output cycle. The 32 segments are used to digitally synthesize a stair-step waveform to approximate the sinewave function (see Figure 3). This is done by connecting a weighted resistor ladder network between the outputs of the Johnson counter, V_{DD} and V_{REF}. V_{REF} closely tracks V_{DD} over the operating voltage and temperature range and therefore the peak-to-peak amplitude VP (V_{DD} – V_{REF}) of the stair-step function is fairly constant. V_{REF} is so chosen that VP falls within the allowed range of the high group and low group tones.

Table 1. Comparisons of Specified Vs. Actual Tone Frequencies Generated by S2859

ACTIVE INPUT	OUTPUT FREQUENCY Hz		%ERROR
	SPECIFIED	ACTUAL	SEE NOTE
R1	697	699.1	+0.30
R2	770	766.2	−0.49
R3	852	847.4	−0.54
R4	941	948.0	+0.74
C1	1209	1215.9	+0.57
C2	1336	1331.7	−0.32
C3	1477	1471.9	−0.35
C4	1633	1645.0	+0.73

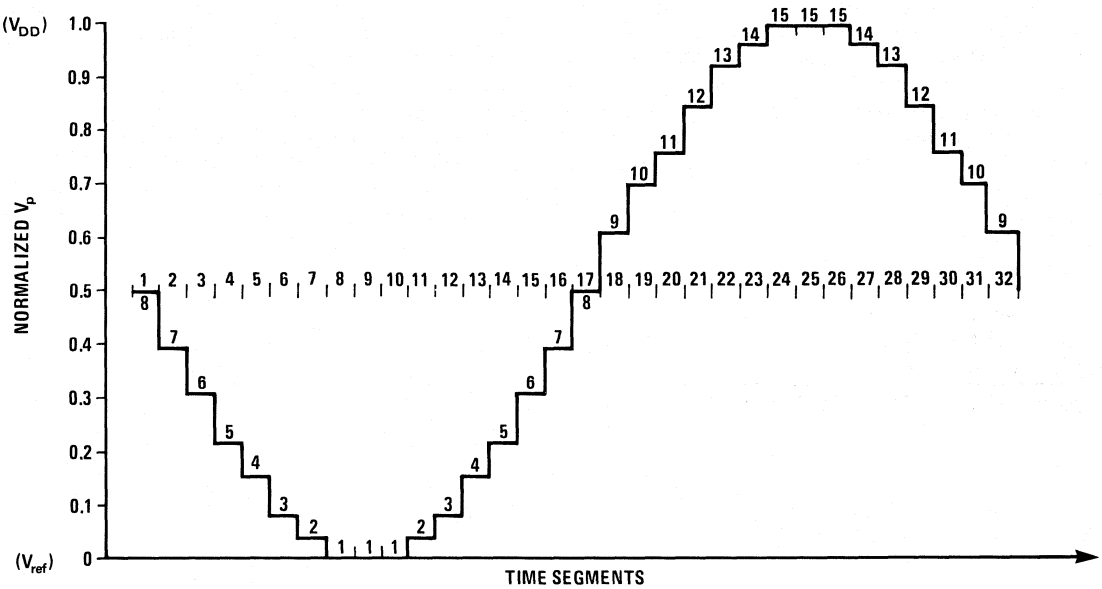
NOTE: %ERROR DOES NOT INCLUDE OSCILLATOR DRIFT

Figure 2. Logic Interface for Keyboard Inputs of the S2859



G1 THRU G8 ANY TYPE CMOS GATE

Figure 3. Stairstep Waveform of the Digitally Synthesized Sinewave



The individual tones generated by the sinewave synthesizer are then linearly added and drive a Darlington NPN transistor connected as an emitter follower to allow proper impedance transformation at the same time preserving signal level.

Dual Tone Mode

When one row and one column is selected dual tone output consisting of an appropriate low group and high group tone is generated. If two digit keys, that are not either in the same row or in the same column, are depressed, the dual tone mode is disabled and no output is provided.

Single Tone Mode

Single tones either in the low group or the high group can be generated as follows. A low group tone can be generated by depressing two digit keys in the appropriate row. A high group tone can be generated by depressing two digit keys in the appropriate column, i.e., selecting the appropriate column input and two row inputs in that column.

Chip Enable

The S2859 has a chip enable input at pin 15. The chip enable for the S2859 is active "High". When the chip enable is "Low", the tone output goes to V_{SS}, the oscillator is inhibited and the MUTE outputs go into an open state.

Crystal Specification

A standard television color burst crystal is specified to have much tighter tolerance than necessary for tone generation application. By relaxing the tolerance specification the cost of the crystal can be reduced. The recommended crystal specification is as follows:

Frequency: 3,579545MHz ±0.02%

R_S 100Ω, L_M = 96MHY

C_M = 0.02pF C_H = 5pF C_L = 12pF

MUTE Outputs

The S2859 has P-Channel buffers for the REC MUTE and XMIT MUTE outputs. With no keys depressed,

the MUTE outputs are open. When a key is depressed, the MUTE outputs go high. When chip enable is "Low" the MUTE outputs are forced in the "open" state regardless of the state of the keyboard.

Timing Sequence

Figure 4 illustrates the sequence in which the MUTE outputs operate when a key is depressed and released. When a valid key is depressed the REC MUTE output goes high first. The XMIT MUTE output goes high after a delay of about 1.6ms. This allows the receiver to be muted prior to the muting of the transmitter and generation of the dual tone. This prevents an undesirable click to be heard in the earpiece due to the momentary interruption of the direct current flowing through the network during the transition time when the transmitter is disconnected and dual tone applied. On release of the key the XMIT MUTE output goes open first, simultaneously the dual tone output is removed. The receiver at this time is still muted so that the click due to the momentary interruption of the direct current during the release of the key is not heard at the earpiece. The REC MUTE output goes open after a delay of about 1.7ms which reconnects the receiver to the network. The leading and trailing edge delays are guaranteed for supply voltages exceeding 3.0 volts. Below 3.0 volts the REC, XMIT MUTE outputs and tone output coincide with each other.

Amplitude/Distortion Measurements

Amplitude and distortion are two important parameters in all applications of the digital tone generator. Amplitude depends upon the operating supply voltage as well as the load resistance connected on the tone output pin. The on-chip reference circuit is fully operational when the supply voltage equals or exceeds 4 volts and as a consequence the tone amplitude is regulated in the supply voltage range above 4 volts. The load resistor value also controls the amplitude. If R_L is low the reflected impedance into the base of the output transistor is low and the tone output amplitude is lower. For R_L greater than 1KΩ the reflected impedance is sufficiently large and highest amplitude is produced. Individual tone amplitudes can be measured by applying the dual tone signal to a wave analyzer (H-P type 3580A) and amplitudes at the selected frequencies can be noted. This measurement also permits verification of the pre-emphasis between the individual frequency tones.

Distortion is defined as "the ratio of the total power of all extraneous frequencies in the voiceband above 500Hz accompanying the signal to the power of the frequency pair". This ratio must be less than 10% or when expressed in dB must be lower than −20dB. (Ref. 1.) Voiceband is conventionally the frequency band of 300Hz to 3400Hz. Mathematically distortion can be expressed as:

$$\text{Dist.} = \frac{\sqrt{(V_1)^2+(V_2)^2+\ldots+(V_N)^2}}{\sqrt{(V_L)^2+(V_H)^2}}$$

where $(V_1) \ldots (V_N)$ are extraneous frequency (i.e., intermodulation and harmonic) components in the 500 Hz to 3400Hz band and V_L and V_H are the individual frequency components of the DTMF signal. The expression can be expressed in dB as:

$$\text{DIST}_{dB} = 20 \log \frac{\sqrt{(V_1)^2+(V_2)^2+\ldots+(V_N)^2}}{\sqrt{(V_L)^2+(V_H)^2}}$$

$$= 10\{\log[(V_1{}^2+\ldots(V_N)^2] - \log[(V_L)^2+(V_H)^2]\} \ldots (1)$$

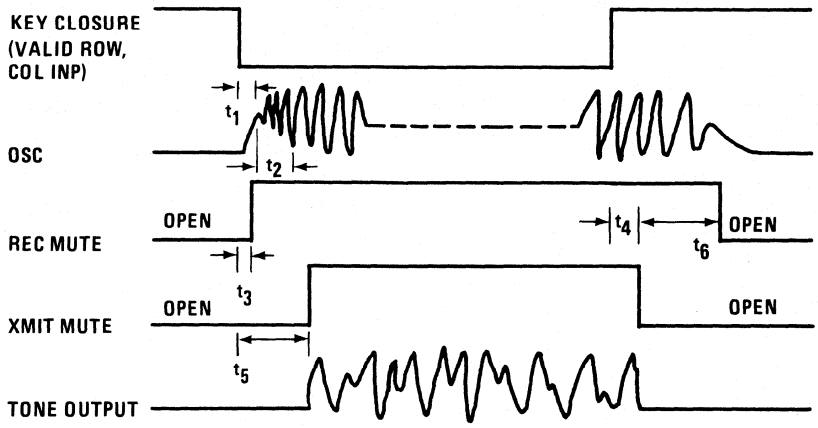
Table 2. Truth Table

INPUTS					OUTPUTS	
KEYS DEPRESSED	NUMBER OF COLUMNS LOW	NUMBER OF ROWS LOW	CHIP ENABLE	TONE	REC MUTE	XMIT MUTE
X	X	X	0	0	OPEN	OPEN
NONE	0	0	1	0	OPEN	OPEN
ONE	1	1	1	R+C	1	1
TWO OR MORE KEYS IN COLUMN	1	2 OR 3 OR 4	1	C	1	1
TWO OR MORE KEYS IN ROW	2 OR 3 OR 4	1	1	R	1	1
MULTI KEY	OTHER COMBINATIONS	OTHER COMBINATIONS	1	0	OPEN	OPEN
NOTE 1	4	3	1	R+C	A	B

X DON'T CARE A: 16 (ROW FREQ) B: 16 (COL FREQ)

NOTE 1: THIS MODE IS USED FOR TEST PURPOSES ONLY. IT IS INITIATED BY CONNECTING ALL COLUMN INPUTS AND THREE OUT OF FOUR ROW INPUTS TO Vss. THE ROW INPUT THAT IS CONNECTED TO V_{DD} ROUTES THE CORRESPONDING 16 TIMES ROW FREQUENCY TO THE REC MUTE OUTPUT AND THE APPROPRIATE 16 TIMES COLUMN FREQUENCY (i.e., R_1 SELECTS C_1 etc.) TO THE XMIT MUTE OUTPUT.

Figure 4. Timing Diagram for ($V_{DD} - V_{SS}$) ≥ 3.0V

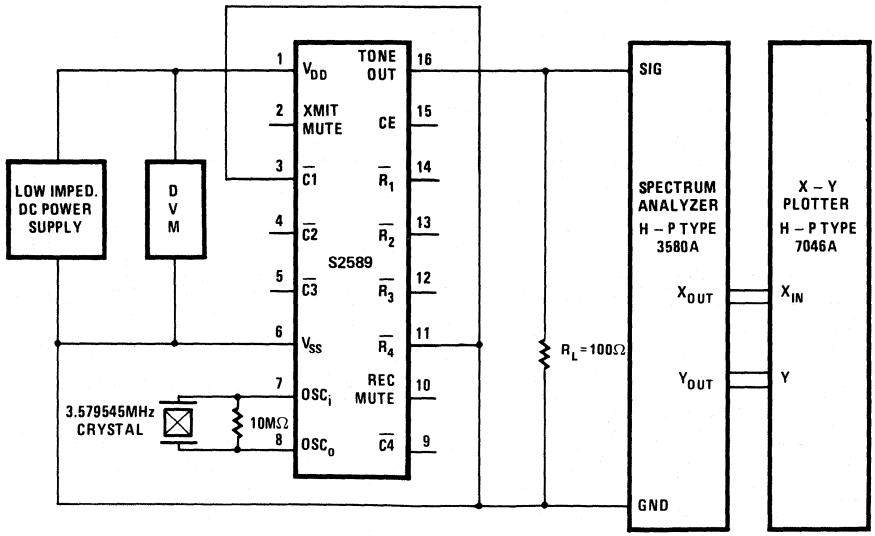


$t_4 \cong 1.7mS$

$1.3mS \leq t_5 \leq 1.6mS \quad 0 < t_6 \leq 1.7mS$

(EXTERNAL PULL-DOWN RESISTOR ASSUMED ON MUTE OUTPUTS)

Figure 5. Test Circuit for Distortion Measurement



DIGITAL TONE GENERATOR

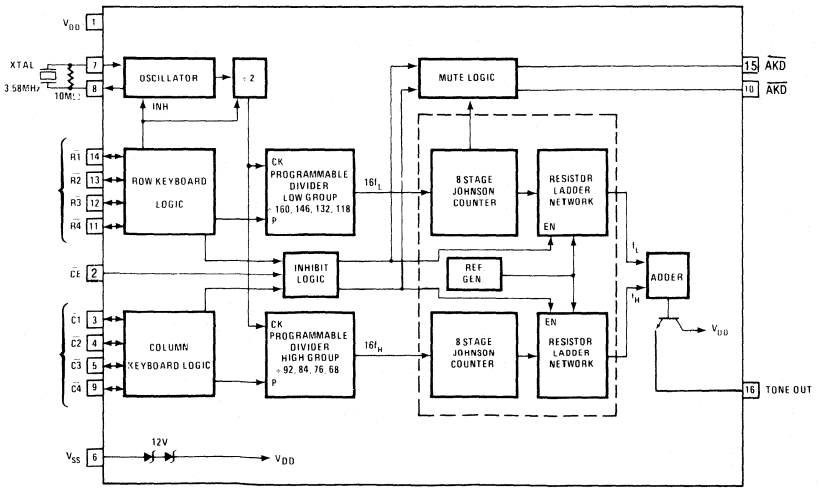
Features

- ☐ **Optimized for Constant Operating Supply Voltages, Typically 3.5V**
- ☐ **Tone Amplitude Stability is Within ±1.3 dB of Nominal Over Operating Temperature Range**
- ☐ **Low Power CMOS Circuitry Allows Device Power to be Derived Directly from the Telephone Lines or from Small Batteries**
- ☐ **Uses TV Crystal Standard (3.58 MHz) to Derive all Frequencies thus Providing Very High Accuracy and Stability**
- ☐ **Specifically Designed for Electronic Telephone Applications**
- ☐ **Interfaces Directly to a Standard Telephone Push-Button or Calculator Type X-Y Keyboard with Common Terminal**
- ☐ **The Total Harmonic Distortion is Below Industry Specification**
- ☐ **Dual Tone as Well as Single Tone Capability**

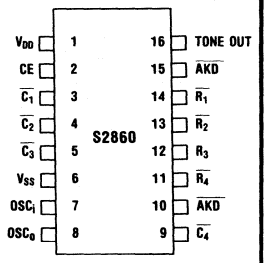
General Description

The S2860 Digital Tone Generator is specifically designed to implement a dual tone telephone dialing system in applications requiring fixed supply operation and high stability tone output level, making it well suited for electronic telephone applications. The device can interface directly to a standard pushbutton telephone keyboard or X-Y keyboard with common terminal connected to V_{SS} and operates directly from the telephone lines. All necessary dual-tone frequencies are derived from the widely used TV crystal standard providing very high accuracy and stability. The required sinusoidal waveform for the individual tones is digitally synthesized on the chip. The waveform so generated has very low total harmonic distortion. A voltage reference is generated on the chip which is very stable over the operating temperature range and regulates the signal levels of the dual tones to meet the recommended telephone industry specifications.

Block Diagram



Pin Configuration



AMERICAN MICROSYSTEMS, INC.

S2560A

PULSE DIALER

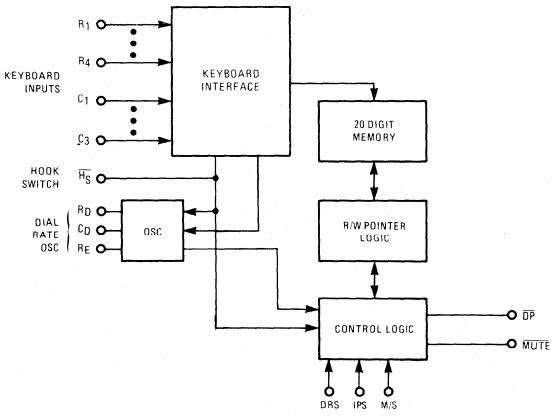
Features

- ☐ **Low Voltage CMOS Process for Direct Operation From Telephone Lines**
- ☐ **Inexpensive R-C Oscillator Design Provides Better than ±5% Accuracy Over Temperature and Unit to Unit Variations**
- ☐ **Dialing Rate Can Be Varied By Changing the Dial Rate Oscillator Frequency**
- ☐ **Dial Rate Select Input Allows Changing of the Dialing Rate by a 2:1 Factor Without Changing Oscillator Components**
- ☐ **Two Selections of Mark/Space Ratios (33-1/3/66-2/3 or 40/60)**
- ☐ **Twenty Digit Memory for Input Buffering and for Redial With Access Pause Capability**
- ☐ **Mute and Dial Pulse Drivers on Chip**
- ☐ **Accepts DPCT Keypad with Common Arranged in a 2 of 7 Format; Also Capable of Interface to SPST Switch Matrix**

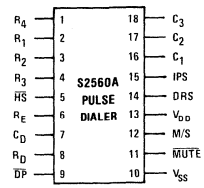
General Description

The S2560A Pulse Dialer is a CMOS integrated circuit that converts pushbutton inputs to a series of pulses suitable for telephone dialing. It is intended as a replacement for the mechanical telephone dial and can operate directly from the telephone lines with minimum interface. Storage is provided for 20 digits, therefore, the last dialed number is available for redial until a new number is entered. IDP is scaled to the dialing rate such as to produce smaller IDP at higher dialing rates. Additionally, the IDP can be changed by a 2:1 factor at a given dialing rate by means of the IDP select input.

Block Diagram



Pin Configuration



Absolute Maximum Ratings:

Supply Voltage	+5.5V
Operating Temperature Range	−25°C to +70°C
Storage Temperature Range	−65°C to +150°C
Voltage at any Pin	V_{SS} −0.3V to V_{DD} +0.3V
Lead Temperature (Soldering, 10sec)	300°C

Electrical Characteristics:

Specifications apply over the operating temperature and $1.5V \leq V_{DD}$ to $V_{SS} \leq 3.5V$ unless otherwise specified.

Symbol	Parameter	$V_{DD}-V_{SS}$ (Volts)	Min.	Max.	Units	Conditions
	Output Current Levels					
I_{OLDP}	$\overline{DP}$ Output Low Current (Sink)	3.5	125		μA	V_{OUT} = 0.4V
I_{OHDP}	$\overline{DP}$ Output High Current (Source)	1.5 3.5	20 125		μA μA	V_{OUT} = 1V V_{OUT} = 2.5V
I_{OLM}	$\overline{MUTE}$ Output Low Current (Sink)	3.5	125		μA	V_{OUT} = 0.4V
I_{OHM}	$\overline{MUTE}$ Output High Current (Source)	1.5 3.5	20 125		μA μA	V_{OUT} = 1V V_{OUT} = 2.5V
I_{OLT}	Tone Output Low Current (Sink)	1.5	20		μA	V_{OUT} = 0.4V
I_{OHT}	Tone Output High Current (Source)	1.5	20		μA	V_{OUT} = 1V
V_{DR}	Data Retention Voltage		1.0		V	"On Hook" $\overline{HS}$ = V_{DD}. Keyboard open, all other input pins to V_{DD} or V_{SS}
I_{DD}	Quiescent Current	1.0		750	nA	
I_{IL}, I_{IH}	Input Current Average (Keyboard Inputs)	3.5		60	μA	One row end one col. input connected to V_{DD}. Other keyboard inputs open.
I_{DD}	Operating Current	1.5 3.5		100 500	μA μA	$\overline{DP}$, $\overline{MUTE}$ open, $\overline{HS}$ = V_{SS} ("Off Hook") Keyboard processing and dial pulsing at 10 pps at conditions as above
fo	Oscillator Frequency	1.5		10	kHz	
Δfo/fo	Frequency Deviation	1.5 to 2.5 2.5 to 3.5	−3 −3	+3 +3	% %	Fixed R-C oscillator components $50K\Omega \leq R_D \leq 750K\Omega$; $100pF \leq C_D{}^* \leq 1000pF$; $750k\Omega \leq R_E \leq 5M\Omega$ *300pF most desirable value for C_D
	Input Voltage Levels					
V_{IH}	Logical "1"		80% of $(V_{DD}-V_{SS})$	V_{DD} +0.3	V	
V_{IL}	Logical "0"		V_{SS} −0.3	20% of $(V_{DD}-V_{SS})$	V	
C_{IN}	Input Capacitance Any Pin			7.5	pF	

The device power supply should always be turned on before the input signal sources, and the input signals should be turned off before the power supply is turned off ($V_{SS} \leq V_I \leq V_{DD}$ as a maximum limit). This rule will prevent over-dissipation and possible damage of the input-protection diode when the device power supply is grounded. When power is first applied to the device, the device should be in "On Hook" condition ($\overline{HS}$=1). This is necessary because there is no internal power or reset on chip and for proper operation all internal latches must come up in a known state. In applications where the device is hard wired in "Off Hook" ($\overline{HS}$)=0) condition, a momentary "On Hook" condition can be presented to the device during power up by use of a capacitor resistor network as shown in Figure 6.

Functional Description

The pin function designations are outlined in Table 1.

Oscillator

The device contains an oscillator circuit that requires three external components: two resistors (R_D and R_E) and one capacitor (C_D). All internal timing is derived from this master time base. To eliminate clock interference in the talk state, the oscillator is only enabled during key closures and during the dialing state. It is disabled at all other times including the "on hook" condition. For a dialing rate of 10 pps the oscillator should be adjusted to 2400 Hz. Typical values of external components for this are R_D and R_E=750kΩ and C_D=270 pF. It is recommended that the tolerance of resistors to be 5% and capacitor to be 1% to insure a ±10% tolerance of the dialing rate in the system.

Keyboard Interface (2560A)

The S2560A employs a scanning technique to determine a key closure. This permits interface to a DPCT keyboard with common connected to V_{DD} (Figure 1), logic interface (Figure 2) and interface to a SPST switch matrix (Figure 7). A high level on the appropriate row and column inputs constitutes a key closure for logic interface. When using a SPST switch matrix, it is necessary to add small capacitors (30 pF) from the column inputs to V_{SS} to insure that the oscillator is shut off after a key is released or after the dialing is complete.

OFF Hook Operation: The device is continuously powered through a 150kΩ resistor during Off hook operation. The DP output is normally high and sources base drive to transistor Q_1 to turn ON transistor Q_2. Transistor Q_2 replaces the mechanical dial contact used in the rotary dial phones. Dial pulsing begins when the user enters a number through the keyboard. The $\overline{DP}$ output goes low shutting the base drive to Q_1 OFF causing Q_2 to open during the pulse break. The $\overline{MUTE}$ output also goes low during dial pulsing allowing muting of the receiver through transistors Q_3 and Q_4. The relationship of dial pulse and mute outputs are shown in Figure 3.

ON Hook Operation: The device is continuously powered through a 10—20MΩ resistor during the ON hook operation. This resistor allows enough current from the tip and ring lines to the device to allow the internal memory to hold and thereby providing storage of the last number dialed.

The dialing rate is derived by dividing down the dial rate oscillator frequency. Table 2 shows the relationship of the dialing rate with the oscillator frequency and the dial rate select input. Different dialing rates can be derived by simply changing the external resistor value. The dial rate select input allows changing of the dialing rate by a factor of 2 without the necessity of changing the external component values. Thus, with the oscillator adjusted to 2400Hz, dialing rates of 10 or 20 pps can be achieved. Dialing rates of 7 and 14 pps similarly can be achieved by changing the oscillator frequency to 1680Hz.

The Inter-Digit Pause (IDP) time is also derived from the oscillator frequency and can be changed by a factor of 2 by the IDP select input. With IDP select pin wired to V_{SS}, an IDP of 800ms is obtained for dial rates of 10 and 20 pps. IDP can be reduced to 400ms by wiring the IDP select pin to V_{DD}. At dialing rates of 7 and 14 pps, IDP's of 1143ms and 572ms can be similarly obtained. If the IDP select pin is connected to the dial rate select pin, the IDP is scaled to the dial rate such that at 10 pps an IDP of 800ms is obtained and at 20 pps an IDP of 400ms is obtained.

The user can enter a number up to 20 digits long from a standard 3x4 double contact keypad with common (Figure 1). It is also possible to use a logic interface as shown in Figure 2 for number entry. Antibounce protection circuitry is provided on chip (min. 20ms.) to prevent false entry.

Any key depressions during the on-hook condition are ignored and the oscillator is inhibited. This insures that the current drain in the on-hook condition is very low and used to retain the memory.

Normal Dialing

The user enters the desired numbers through the keyboard after going off hook. Dial pulsing starts as soon as the first digit is entered. The entered digits are stored sequentially in the internal memory. Since the device is designed in a FIFO arrangement, digits can be entered at a rate considerably faster than the output rate. Digits can be entered approximately once every 50ms while the dialing rate may vary from 7 to 20 pps. The number entered is retained in the memory for future redial. Pauses may be entered when required in the dial sequence by pressing the "#" key, which provides access pauses for future redial. Any number of access pauses may be entered as long as the total entries do not exceed twenty.

Auto Dialing

The last number dialed is retained in the memory and therefore can be redialed out by going off hook and pressing the "#" key. Dial pulsing will start when the key is depressed and finish after the entire number is dialed out unless an access pause is detected. In such a case, the dial pulsing will stop and will resume again only after the user pushes the "#" key.

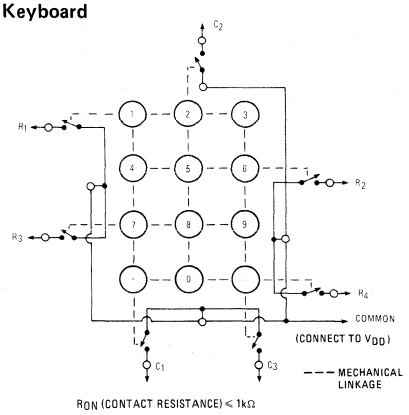
Table 1. S2560A Pin/Function Descriptions

Pin	Number	Function
Keyboard (R_1, R_2, R_3, R_4, C_1, C_2, C_3)	7	These are 4 row and 3 column inputs from the keyboard contacts. These inputs are open when the keyboard is inactive. When a key is pushed, an appropriate row and column input must go to V_{DD} or connect with each other. A logic interface is also possible as shown in Figure 3. Active pull up and pull down networks are present on these inputs when the device begins keyboard scan. The keyboard scan begins when a key is pressed and starts the oscillator. Debouncing is provided to avoid false entry (typ. 20ms).
Inter-Digit Pause Select (IPS)	1	One programmable line is available that allows selection of the pause duration that exists between dialed digits. It is programmed according to the truth table shown in Table 3. Note that preceding the first dialed pulse is an inter-digit time equal to the selected IDP. Two pauses either 400ms or 800ms are available for dialing rates of 10 and 20 pps. IDP's corresponding to other dialing rates can be determined from Tables 2 and 3.
Dial Rate Select (DRS)	1	A programmable line allows selection of two different output rates such as 7 or 14 pps, 10 or 20 pps, etc. See Tables 2 and 3.
Mark/Space (MS)	1	This input allows selection of the mark/space ratio, as per Table 3.
Mute Out ($\overline{\text{MUTE}}$)	1	A pulse is available that can provide a drive to turn on an external transistor to mute the receiver during the dial pulsing.

Table 1. (Continued)

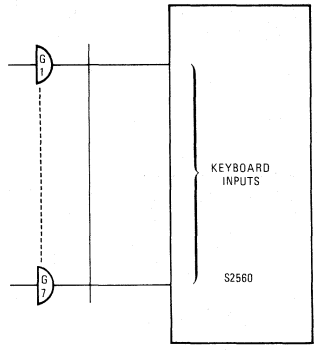
Pin	Number	Function
Dial Pulse Out ($\overline{DP}$)	1	Output drive is provided to turn on a transistor at the dial pulse rate. The normal output will be "low" during "space" and "high" otherwise.
Dial Rate Oscillator	3	These pins are provided to connect external resistors R_D, R_E and capacitor C_D to form an R-C oscillator that generates the time base for the Key Pulser. The output dialing rate and IDP are derived from this time base.
Hook Switch ($\overline{HS}$)	1	This input detects the state of the hook switch contact; "off hook" corresponds to V_{SS} condition.
Power (V_{DD}, V_{SS})	2	These are the power supply inputs. The device is designed to operate from 1.5V to 3.5V.
	18	

Figure 1. Standard Telephone Pushbutton Keyboard



RON (CONTACT RESISTANCE) < 1kΩ

Figure 2. Logic Interface For the S2560



G1 through G7 any CMOS type logic gates

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Figure 3. Timing

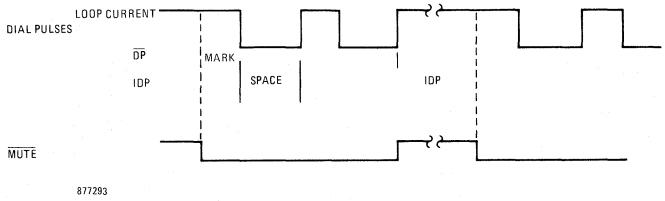

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Table 2. Table for Selecting Oscillator Component Values for Desired Dialing Rates and Inter-Digit Pauses

Dial Rate Desired	Osc. Freq. (Hz)	R_D (kΩ)	R_E (kΩ)	C_D (pF)	Dial Rate (pps)		IDP (ms)	
					DRS=V_{SS}	DRS=V_{DD}	IPS=V_{SS}	IPS=V_{DD}
5.5/11	1320	Select components in the ranges indicated in table of electrical specifications			5.5	11	1454	727
6/12	1440				6	12	1334	667
6.5/13	1560				6.5	13	1230	615
7/14	1680				7	14	1142	571
7.5/15	1800				7.5	15	1066	533
8/16	1920				8	16	1000	500
8.5/17	2040				8.5	17	942	471
9/18	2160				9	18	888	444
9.5/19	2280				9.5	19	842	421
10/20	2400	750	750	270	10	20	800	400
(f_d/240)/ (f_d/120)	f_d				(f_d/240)	(f_d/120)	$\left(\frac{1920}{f_i} \times 10^3\right)$	$\left(\frac{960}{f_i} \times 10^3\right)$

Notes:

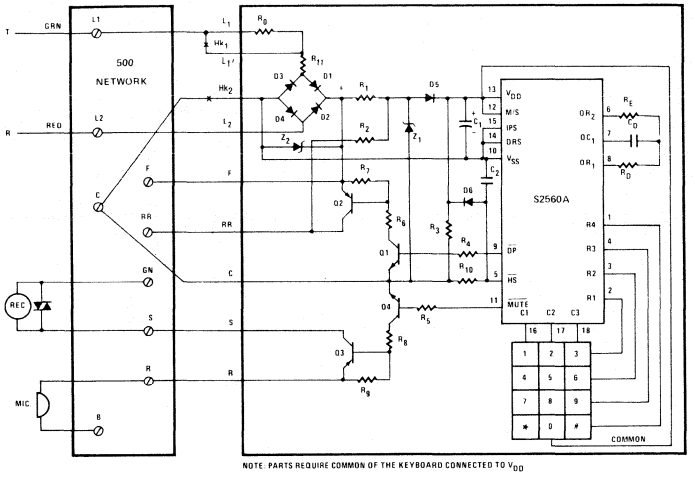
1. IDP is dependent on the dialing rate selected. For example, for a dialing rate of 10 pps, an IDP of either 800ms or 400ms can be selected. For a dialing rate of 14 pps, and IDP of either 1142ms or 571ms can be selected.

Table 3.

Function	Pin Designation	Input Logic Level	Selection
Dial Pulse Rate Selection	DRS	V_{SS} V_{DD}	(f/240) pps (f/120) pps
Inter-Digit Pause Selection	IPS	V_{DD} V_{SS}	$\frac{960}{f}$ s $\frac{1920}{f}$ s
Mark/Space Ratio	M/S	V_{SS} V_{DD}	33-1/3/66-2/3 40/60
On Hook/Off Hook	$\overline{HS}$	V_{DD} V_{SS}	On Hook Off Hook

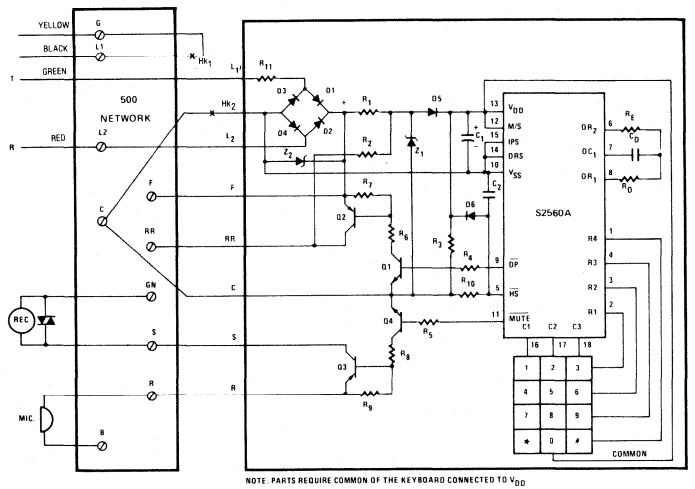
Note: f is the oscillator frequency and is determined as shown in Figure 5.

Figure 4. Pulse Dialer Circuit with Redial



$R_0 = 10 - 20M\Omega$, $R_1 = 150k\Omega$, $R_2 = 2k\Omega$
$R_3 = 470k\Omega$, R_4, $R_5 = 10k\Omega$, $R_{10} = 47k\Omega$
R_6, $R_8 = 2k\Omega$, R_7, $R_9 = 30k\Omega$, $R_{11} = 20\Omega$, 2W
$Z_1 = 3.9V$, $D_1 - D_4 =$ IN4004, D_5, $D_6 =$ IN914, $C_1 = 15\mu F$
$R_E = R_D = 750k\Omega$, $C_D = 270pF$, $C_2 = 0.01\mu F$
Q_1, $Q_4 =$ 2N5550 TYPE Q_2, $Q_3 =$ 2N5401 TYPE
$Z_2 =$ 1N5379 110V ZENER OR 2X1N4758

Figure 5. Pulse Dialer Circuit with Redial (Single Hook Switch Contact Application for PABX)



$R_1 = 10$-$20M\Omega$, $R_2 = 2k\Omega$
$R_3 = 470k\Omega$, R_4, $R_5 = 10k\Omega$
R_6, $R_8 = 2k\Omega$, R_7, $R_9 = 30k\Omega$
$R_{10} = 47k\Omega$, $R_{11} = 20\Omega$, 2W
$Z_1 = 3.9V$, $D_1 - D_4 =$ IN4004
D_5, $D_6 =$ 1N914, $C_1 = 15\mu F$
R_E, $R_D = 750k\Omega$, $C_D = 270pF$
$C_2 = 0.01\mu F$, Q_1, $Q_4 =$ 2N5550
Q_2, $Q_3 =$ 2N5401
$Z_2 =$ 150V ZENER OR VARISTOR TYPE GE MOV150

Figure 6. Circuit for Applying Momentary "On Hook" Condition During Power Up

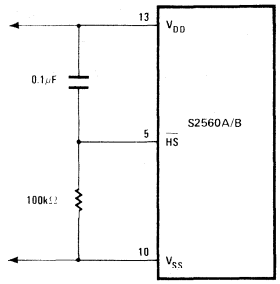
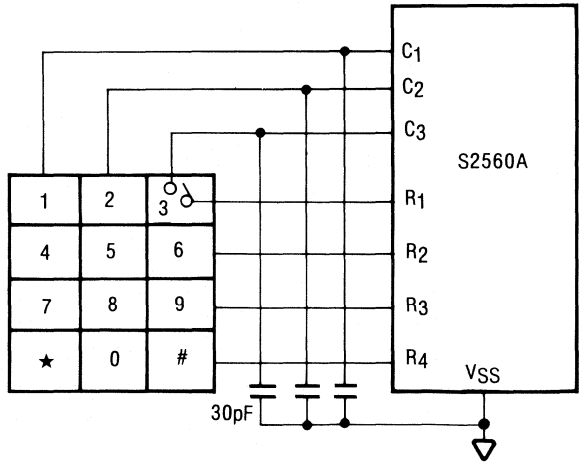


Figure 7. SPST Switch Matrix Interface



TONE RINGER

Features

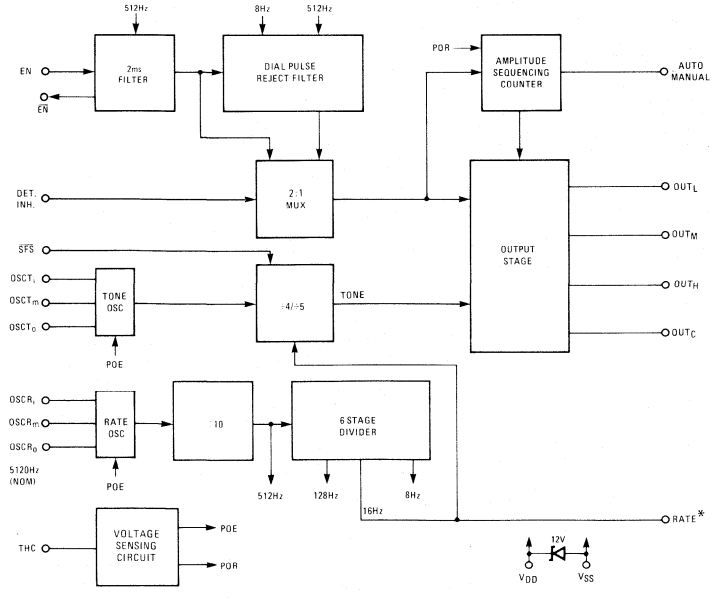
- ☐ CMOS Process for Low Power Operation
- ☐ Operates Directly from Telephone Lines with Simple Interface
- ☐ Also Capable of Logic Interface for Non-Telephone Applications
- ☐ Provides a Tone Signal that Shifts Between Two Predetermined Frequencies at Approximately 16Hz to Closely Simulate the Effects of the Telephone Bell
- ☐ Push-Pull Output Stage Allows Direct Drive, Eliminating Capacitive Coupling and Provides Increased Power Output
- ☐ 25mW Output Drive Capability at 10V Operating Voltage
- ☐ Auto Mode Allows Amplitude Sequencing such that the Tone Amplitude Increases in Each of the First Three Rings and Thereafter Continues at the Maximum Level
- ☐ Single Frequency Tone Capability

General Description

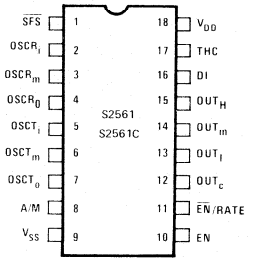
The S2561 Tone Ringer is a CMOS integrated circuit that is intended as a replacement for the mechanical telephone bell. It can be powered directly from the telephone lines with minimum interface and can drive a speaker to produce sound effects closely simulating the telephone bell.

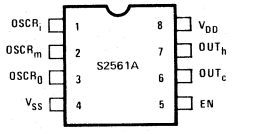
Data subject to change at any time without notice. These sheets transmitted for information only.

Block Diagram



Pin Configuration





Absolute Maximum Ratings

Supply Voltage	+12.0V*
Operating Temperature Range	−25°C to +70°C
Storage Temperature Range	−40°C to +125°C
Voltage at any Pin	V_{SS} −0.3V to V_{DD} +0.3V
Lead Temperature (Soldering, 10sec)	300°C

**This device incorporates a 12V internal zener diode across the V_{DD} to V_{SS} pins. Do NOT connect a low impedance power supply directly across the device unless the supply voltage can be maintained below 12V or current limited to <25mA.*

Electrical Characteristics

Specifications apply over the operating temperature and $3.5V \leq V_{DD}$ to $V_{SS} < 12.0V$ unless otherwise specified.

Symbol	Parameter	Min.	Max.	Units	Conditions
V_{DS}	Operating Voltage (V_{DD} to V_{SS})	8.0	12.0	V	Ringing, THC pin open
V_{DS}	Operating Voltage	4.0		V	"Auto" mode, non-ringing
I_{DS}	Operating Current		500	μA	Non-ringing, V_{DD}=10V, THC pin open, DI pin open or V_{SS}
I_{OHC}	Output Drive Output Source Current (OUT_H, OUT_C outputs)	5		mA	V_{DD}=10V, V_{OUT}=8.75V
I_{OLC}	Output Sink Current (OUT_H, OUT_C outputs)	5		mA	V_{DD}=10V, V_{OUT}=0.75V
I_{OHM}	Output Source Current (Out_M output)	2		mA	V_{DD}=10V, V_{OUT}=8.75V
I_{OLM}	Output Sink Current (OUT_M output)	2		mA	V_{DD}=10V, V_{OUT}=0.75V
I_{OHL}	Output Source Current (OUT_L output)	1		mA	V_{DD}=10V, V_{OUT}=8.75V
I_{OLL}	Output Sink Current (OUT_L output)	1		mA	V_{DD}=10V, V_{OUT}=0.75V
	CMOS to CMOS				
V_{IH}	Input Logic "1" Level	0.7 V_{DD}	V_{DD}+0.3	V	All inputs
V_{IL}	Input Logic "0" Level	V_{SS}−0.3	0.3 V_{DD}	V	All inputs
V_{OHR}	Output Logic "1" Level (Rate output)	0.9 V_{DD}		V	I_O=10μA (Source)
V_{OLR}	Output Logic "0" Level (Rate output)		0.5	V	I_O=10μA (Sink)
V_{OZ}	Output Leakage Current (OUT_H, OUT_M outputs in high impedance state)		1 1	μA μA	V_{DD}=10V, V_{OUT}=0V V_{DD}=10V, V_{OUT}=10V
C_{IN}	Input Capacitance		7.5	pF	Any pin
Δfo/fo	Oscillator Frequency Deviation	−5	+5	%	Fixed RC component values $1M\Omega \leq R_{ri}$, $R_{ti} \leq 5M\Omega$; $100k\Omega \leq R_{rm}$, $R_{tm} \leq 750k\Omega$; $150pF \leq C_{ro}$, $C_{to} \leq 3000pF$; 330pF recommended value of C_{ro} and C_{to}, supply voltage varied from 9V±2V (over temperature and unit-unit variations)
R_{LOAD}	Output Load Impedance Connected Across OUT_H and OUT_C	600		Ω	Tone Frequency Range=300Hz to 3400Hz
I_{IH}, I_L	Leakage Current, $V_{IN}=V_{DD}$ or V_{SS}		100	nA	Any input, except DI pin V_{DD}=10V
V_{TH}	POE Threshold Voltage	6.5	8	V	
V_Z	Internal Zener Voltage	11	13	V	I_Z=5mA

The device power supply should always be turned on before the input signal sources, and the input signals should be turned off before the power supply is turned off ($V_{SS} \leq V_I \leq V_{DD}$ as a maximum limit). This rule will prevent over-dissipation and possible damage of the input-protection diode when the device power supply is grounded

Functional Description

The S2561 is a CMOS device capable of simulating the effects of the telephone bell. This is achieved by producing a tone that shifts between two predetermined frequencies (512 and 640 Hz) with a frequency ratio of 5:4 at a 16 Hz rate.

Tone Generation: The output tone is derived from a tone oscillator that uses a 3 pin R-C oscillator design consisting of one capacitor and two resistors. The oscillator frequency is divided alternately by 4 or 5 at the shift rate. Thus, with the oscillator adjusted for 5120Hz, a tone signal is produced that alternates between 512Hz and 640Hz at the shift rate. The shift rate is derived from another 3 pin R-C oscillator which is adjusted for a nominal frequency of 5120Hz. It is divided down to 16Hz which is used to produce the shift in the tone frequency. It should be noted that in the special case where both oscillators are adjusted for 5120Hz, it is only necessary to have one external R-C network for one oscillator with the other oscillator driven from it. The oscillators are designed such that for fixed R-C component values an accuracy of ±5% can be obtained over the operating supply voltage, temperature and unit-unit variations. See Table 1 for component and frequency selections. In the single frequency mode, activated by connecting the $\overline{SFS}$ input to V_{SS} only the higher frequency continuous tone is produced by using a fixed divider ratio of 4 and by disabling the shift operation.

Ring Signal Detection: In the following description it is assumed that both the tone and rate oscillators are adjusted for a frequency of 5120 Hz. Ringing signal (nominally 42 to 105 VAC, 20 Hz, 2 sec on/4 sec off duty cycle) applied by the central office between the telephone line pair is capacitively coupled to the tone ringer circuitry as shown in Figure 2. Power for the device is derived from the ringing signal itself by rectification (diodes D1 thru D4) and zener diode clamping (Z_2). The signal is also applied to the EN input after limiting and clamping by a resistor (R_2) and internal diodes to V_{DD} and V_{SS} supplies. Internally the signal is first squared up and then processed thru a 2ms filter followed by a dial pulse reject filter. The 2ms filter is a two stage shift register clocked by a 512 Hz signal derived from the rate oscillator by a divide by 10 circuit. The squared ring signal (typically a square wave) is applied to the D input of the first stage and also to reset inputs of both stages. This provides for rejection of spurious noise spikes. Signals exceeding a duration of 2ms only can pass through the filter. The dial pulse reject filter is clocked at 8 Hz derived from the rate oscillator by a divide by 640 circuit. This circuit is designed to pass any signal that has at least two transitions in a given 125ms time period. This insures that signals below 8 Hz will be rejected with certainty. Signals over 16 Hz will be passed with certainty and between 8 Hz and 16 Hz there is a region of uncertainty. By adjusting the rate oscillator to a different frequency the break points in frequencies can be varied. For instance for break points of 10 Hz and 20 Hz the rate oscillator can be adjusted to 6400 Hz. Of course this also increases the tone shift rate to 20 Hz. The action of the dial pulse reject filter minimizes the dial pulse interference during dialing although it does not completely eliminate it due to the rather large region of uncertainty associated with this type of discrimination circuitry. The dial pulse filter also has the characteristic that an input signal is not detected unless its duration exceeds 125ms. This insures that the tone ringer will not respond to momentary bursts of ringing less than 125 milliseconds in duration (Ref 1).

In logic interface applications, the 2ms filter and the dial pulse reject filter can be inhibited by wiring the Det. INHIBIT pin to V_{DD}. This allows the tone ringer to be enabled by a logic '1' level applied at the "ENABLE" input without the necessity of a 20Hz ring signal.

Voltage Sensing: The S2561 contains a voltage sensing circuit that enables the output stage and the rate and tone oscillators, only when the supply voltage exceeds a predetermined value. Typical value of this threshold is 7.3 volts. This produces two benefits. First, it insures that the audible intensity of the output tone is fairly constant throughout the ringing period; and secondly, it insures proper circuit operation during the "auto" mode operation by reducing the power consumption to a minimum when the supply voltage drops below 7.3 volts. This extends the supply voltage decay time beyond 4 seconds (off period of the ring signal) with an adequate filter capacitor and insures the proper functioning of the "amplitude sequencing" counter. It is important to note that the operating supply voltage should be well above the threshold value during the ringing period and that the filter capacitor should be large enough so that the ripple on the supply voltage does not fall below the threshold value. A supply voltage of 10 to 12 volts is recommended.

In applications where the tone ringer is continuously powered and below the threshold level, the internal threshold can be bypassed by connecting the THC pin to V_{DD}. The internal threshold can also be reduced

Functional Description (Continued)

by connecting an external zener diode between the THC and V_{DD} pins.

Auto Mode: In the "auto" mode, activated by wiring the "auto/manual" input to V_{SS}, an amplitude sequencing of the output tone can be achieved. Resistors R_L and R_M are inserted in series with the Out_L and Out_M outputs, respectively, and paralleled with the Out_H output (Figure 1). Load is connected across Out_H and Out_C pins. R_L is chosen to be higher than R_M. In this manner the first ring is of the lowest amplitude, second ring is of medium amplitude and the third and consecutive rings thereafter are at maximum amplitude. For the proper functioning of the "amplitude sequencing" counter the device must have at least 4.0 volts across it throughout the ring sequence. The filter capacitor is so chosen that the supply voltake will not drop below 4.0 volts during the off period. At the end of a ring sequence when the off period substantially exceeds the 4 second duration, the counter will be reset. This will insure that the amplitude sequencing will start correctly beginning a new ring sequence. The counter is held in reset during the "manual" mode operation. This produces a maximum ring amplitude at all times.

Output Stage: The output stage is of push-pull type consisting of buffers L, M, H and C. The load is connected across pins Out_H and Out_C (Figure 2). During ringing, the Out_H and Out_C outputs are out of phase with each other and pulse at the tone rate. During a non-ringing state, all outputs are forced to a known level such as ground which insures that there is no DC component in the load. Thus, direct coupling can be used for driving the load. The major benefit of the push-pull arrangement is increased power output. Four times as much power can be delivered to the load for the same operating voltage. Buffers M and H are three-state. In the "auto" mode buffer M is active only during the second ring and in the "high impedance" state at all other times. Buffer H is active beginning the third ring. In the "manual" mode buffers H, L and C are active at all times while buffer M is in a high impedance state. The output buffers are so designed that they can source or sink 5mA at a V_{DD} of 10 volts without appreciable voltage drop. Care has been taken to make them symmetrical in both source and sink configurations. Diode clamping is provided on all outputs to limit the voltage spikes associated with transformer drive in both directions V_{DD} and V_{SS}.

Normal protection circuits are present on all inputs.

Table 1. S2561/S2561C Pin/Function Descriptions

Pin	Number	Function
Power (V_{DD}*, V_{SS}*)	2	These are the power supply pins. The device is designed to operate over the range of 3.5 to 12.0 volts. A range of 10 to 12 volts is recommended for the telephone application.
Ring Enable (EN*, $\overline{EN}$)	2	These pins are for the 20Hz ring enable input. They can also be used for DC level enabling by wiring the DI pin to V_{DD}. $\overline{EN}$ is available for the S2561 only.
Auto/Manual (A/M)	1	"Auto" mode for amplitude sequencing is implemented by wiring this pin to V_{SS}. "Manual" mode results when connected to V_{DD}. The amplitude sequencing counter is held in reset during the "manual" mode.
Outputs (Out_L, Out_M, Out_H^*, Out_C^*)	4	These are the push-pull outputs. Load is directly connected across Out_H and Out_C outputs. In the "auto" mode, resistors R_L and R_M can be inserted in series with the Out_L and Out_M outputs for amplitude sequencing (see Figure 1).
Oscillators Rate Oscillator ($OSCR_i^*$, $OSCR_m^*$ $OSCR_o^*$)	3	These pins are provided to connect external resistors RR_i, RR_m and capacitor CR_o to form an R-C oscillator with a nominal frequency of 5120Hz. See Table 2 for components selection.

Table 1 (Continued)

Pin	Number	Function
Tone Oscillator ($OSCT_i$, $OSCT_m$, $OSCT_o$)	3	These pins are provided to connect external resistors RT_i, RT_m and capacitor CT_o to form an R-C oscillator from which the tone signal is derived. With the oscillator adjusted to 5120Hz, a tone signal with frequencies of 512Hz and 640Hz results. See Table 2 for components selection.
Threshold Control (THC)	1	The internal threshold voltage is brought out to this pin for modification in non-telephone applications. It should be left open for telephone applications. For power supplies less than 9V connect to V_{DD}.
Rate	1	This is an optional output for the S2561C version which replaces the $\overline{EN}$ output. This is a 16Hz output that can be used by external logic as shown in Figure 3-A to produce a 2sec on/4sec off waveform.
Detector Inhibit (DI)	1	When this pin is connected to V_{DD}, the dial pulse reject filter is disabled to allow DC level enabling of the tone ringer. This pin should be hardwired to V_{SS} in normal telephone-type applications.
Single Frequency Select ($\overline{SFS}$)	1	When this pin is connected to V_{SS}, only a single frequency continuous tone is produced as long as the tone ringer is enabled. In normal applications this pin should be hardwired to V_{DD}.
	$\overline{18}$	

**Pinouts of 8 pin S2561A package.*

Table 2. Selection Chart for Oscillator Components and Output Frequencies

Tone/Rate Oscillator Frequency (Hz)	Oscillator Components R_I (kΩ)	R_M (kΩ)	C_O (pF)	Rate (Hz)	Tone (Hz)
5120	1000	200	330	16	512/640
6400	Select components in the ranges indicated in the table of electrical charateristics			20	640/800
3200				10	320/400
8000				25	800/1000
fo				$\frac{fo}{320}$	$\frac{fo}{10}/\frac{fo}{8}$

Applications

Typical Telephone Application: Figure 2 shows the schematic diagram of a typical telephone application for the S2561 tone ringer circuit. Power is derived from the telephone lines by the network formed by capacitor C_1, resistor R_1, diode bridge d_1 through d_4, and filter capacitor C_2. C_2 is chosen to be large enough so as to insure that the power supply ripple during ringing does not fall below the internal threshold level (typ. 7.3 volts) and to provide large enough decay time during the off period. A typical value of C_2 may be 47μF. C_1 and R_1 are chosen to satisfy the Ringer Equivalence Number (REN) specification (Ref. 1). For REN = 1 the resistor should be a minimum of 8.2kΩ. It must be noted that the amount of power that can be delivered to the load depends upon the selection of C_1 and R_1.

The device is enabled by limiting the incoming ring signal through resistors R_2, R_3 and diodes d_5 and d_6. Zener diode Z_1 (typ. 9-27 volts) may be required in certain applications where large voltage transients may occur on the line during dial pulsing. The internal 2ms filter and the dial pulse reject filter will suppress any undesirable components of the signal and will only respond to the normal 20Hz ring signal. Ring signals with frequencies above 16Hz will be detected.

The configuration shown will produce a tone with frequency components of 512Hz and 540 Hz with a shift rate of approximately 16 Hz and deliver at least 25mW to an 8Ω speaker through a 2000Ω:8Ω transformer. If "manual" mode is used, a potentiometer may be inserted in series with the transformer primary to provide volume control. If "automatic" mode is used, resistors R_L and R_M can be chosen to provide desired amplitude sequencing. Typically, signal power will be down $20 \log \left(\frac{R_{LOAD}}{R_L + R_{LOAD}} \right)$ dB during the first ring, and down $20 \log \left(\frac{R_{LOAD}}{R_M + R_{LOAD}} \right)$ dB during the second ring with maximum power delivered to the load beginning the third and consecutive rings.

In applications where dial pulse rejection is not necessary, such as in DTMF telephone systems, the ENABLE pin may be connected directly to V_{DD}. Det. Inh pin must be connected to V_{DD} to allow DC level enabling of the ringer.

Non-Telephone Applications: The configuration shown in Figure 3-A may be used in non-telephone applications where it is desired to simulate the telephone bell. The internal threshold is bypassed by wiring THC to V_{DD}. The rate output (16Hz) is divided down by a 7 stage divider type 4024 to produce two signals: a 2 second on/2 second off signal and a 4 second on/4 second off signal. The first signal is connected to the EN pin and the second to the DI pin to produce a 2 second on/4 second off telephone-type ring signal. The ring sequence is initiated by removing the reset on the divider. If "auto" mode is used, a reset signal must be applied to the "amplitude sequencing" counter at the end of a ring sequence so that the circuit will respond correctly to a new ring sequence. This is done by temporarily connecting the "auto/manual" input to V_{SS}.

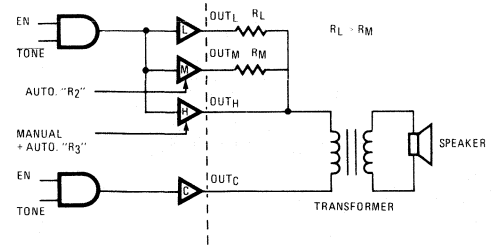
Figure 3-B shows a typical application for alarms, buzzers, etc. Single frequency mode is used by connecting the $\overline{SFS}$ input to V_{SS}. A suitable on/off rate can be determined by using the 7 stage divider circuit. If continuous tone is not desired, the 16Hz output can be used to gate the tone on and off by wiring it into the ENABLE input.

Many other configurations are possible depending upon the user's specific application.

Reference 1. Bell system communications technical reference:

PUB 47001 of August 1976
"Electrical characteristics of Bell System Network Facilities at the interface with Voiceband Ancillary and Data Equipment" — Sections 2.6.1 and 2.6.3.

Figure 1-A. Output Stage Connected for Auto Mode Operation



877276

Figure 1-B. Output Stage Connected for Manual Mode Operation.

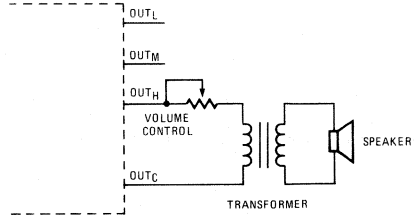


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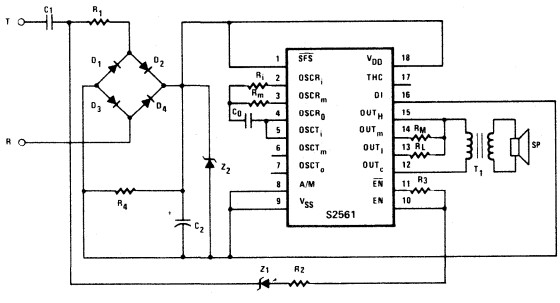
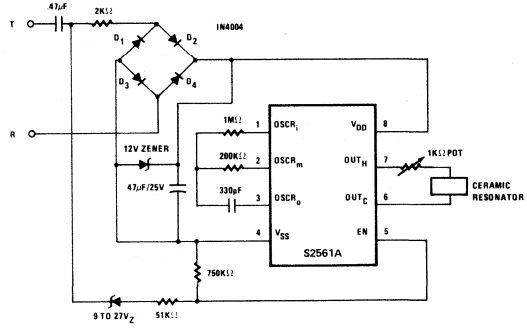
Figure 2. Typical Telephone Application of the S2561 and S2561A





C_1	.47μF/200V	R_1	2KΩ	R_i	1MΩ	R_L	18KΩ	SP	8ΩSPEAKER
C_2	.47μF/25V	R_2	51KΩ	R_m	200KΩ	R_M	3.3KΩ	T_1	2000Ω/8ΩXFMR
D_1–D_4	IN4004	R_3	10MΩ	C_0	300pF	R_4	100KΩ	Z_1	9 TO 27V ZENER
Z_2	IN4742 12V ZENER								

Figure 3-A. Simulation of the Telephone Bell in Non-Telephone Applications.

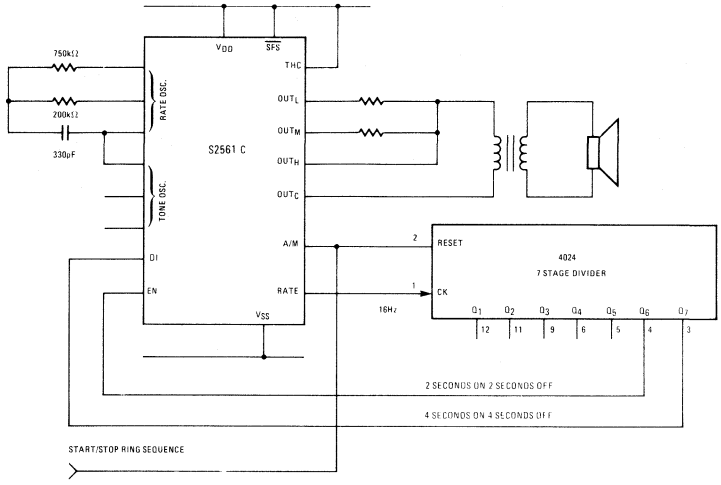
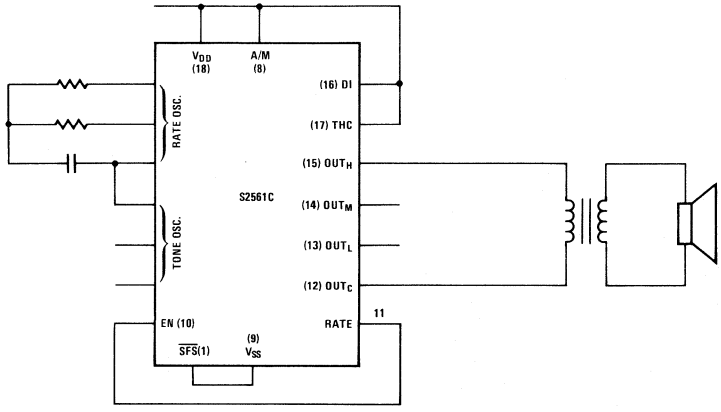


Figure 3-B. Single Frequency Tone Application in Alarms, Buzzers, Etc.



AMERICAN MICROSYSTEMS, INC.

S2562

REPERTORY DIALER

COMMUNICATIONS

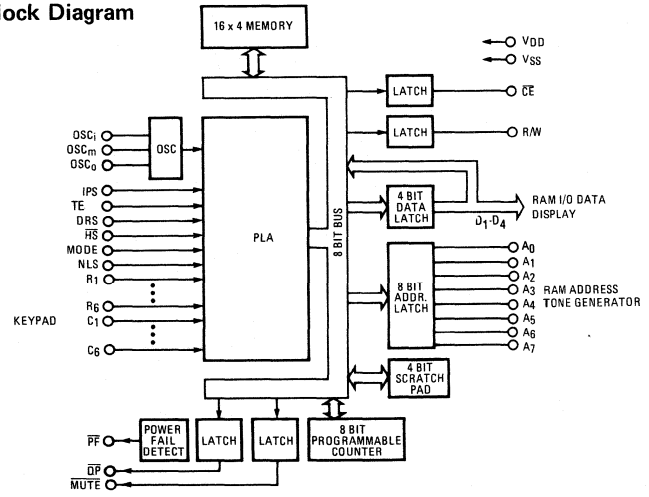
Features

- ☐ CMOS Process Achieves Low Power Operation
- ☐ 8 or 16 Digit Number Capability (Pin Programmable)
- ☐ Dial Pulse and Mute Output
- ☐ Tone Outputs Obtained by Interfacing with Standard AMI S2559 Tone Generator
- ☐ Two Selections of Dial Pulse Rate
- ☐ Two Selections of Inter-Digit Pause
- ☐ Memory Storage of 32 8-Digit Numbers or 16 16-Digit Numbers with Standard AMI S5101 RAM
- ☐ 16-Digit Memory for Input Buffering and for Redial with Access Pause Capability
- ☐ Accepts the Standard Telephone DPCT Keypad or SPST Switch X-Y Matrix Keyboards; Also Capable of Logic Interface
- ☐ Ignores Multi Key Entries
- ☐ Inexpensive, but Accurate R-C Oscillator Design Provides Better Than ± 3% Accuracy Over Supply Voltage, Temperature and Unit-Unit Variations and Allows Different Dialing Rates, IDP and Tone Drive Timing by Changing the Time Base
- ☐ Power Fail Detection
- ☐ BCD Output with Update for Number Display Applications

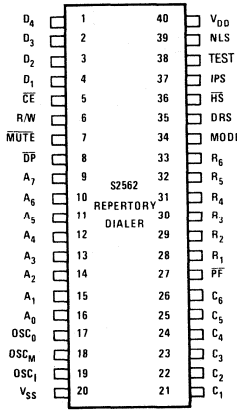
General Description

The S2562 Repertory Dialer is a CMOS integrated circuit that can perform storing or retrieving, normal dialing, redialing or auto dialing and displaying of one of several telephone numbers. It is intended to be used with the AMI standard S5101—256x4 RAM that functions as telephone number storage. With one S5101 up to 32 8-digit or 16 16-digit numbers can be stored. It can provide either dial pulses or DTMF tones with the addition of the AMI S2559 tone generator for either the dial or tone line applications.

Block Diagram



Pin Configuration



Absolute Maximum Ratings:

Supply Voltage	13.5V
Operating Supply Voltage Range ($V_{DD}-V_{SS}$)	3.5V to 7.5V
Operating Temperature Range	−25°C to +70°C
Storage Temperature Range	−40°C to +125°C
Voltage at any Pin	V_{SS} −0.3V to V_{DD} +0.3V
Lead Temperature (Soldering, 10sec)	200°C

Electrical Characteristics:
Specifications apply over the operating temperature range and $4.5V \leq V_{DD}$ to $V_{SS} \leq 5.5V$ unless otherwise specified. Absolute values of measured parameters are specified.

Symbol	Characteristics	Min.	Max.	Units	Conditions
	Output Drive				
I_{OLDP}	$\overline{DP}$ Output Sink Current	400		μA	$V_{OUT}=0.4V$, $V_{DD}=5V$
I_{OHDP}	$\overline{DP}$ Output Source Current	400		μA	$V_{OUT}=3.6V$, $V_{DD}=5V$
I_{OLM}	$\overline{MUTE}$ Output Sink Current	400		μA	$V_{OUT}=0.4V$, $V_{DD}=5V$
I_{OHM}	$\overline{MUTE}$ Output Source Current	400		μA	$V_{OUT}=3.6V$, $V_{DD}=5V$
I_{OHPF}	$\overline{PF}$ Output Source Current	100		μA	$V_{OUT}=3.6V$, $V_{DD}=5V$
	CMOS to CMOS				
V_{IL}	Logic "0" Input Voltage		1.5	V	All inputs, $V_{DD}=5V$
V_{IH}	Logic "1" Input Voltage	3.5		V	All inputs, $V_{DD}=5V$
V_{OL}	Logic "0" Output Voltage		0.5	V	All outputs except $\overline{DP}$, $\overline{MUTE}$, $\overline{PF}$, $I_O=-10\mu A$, $V_{DD}=5V$
V_{OH}	Logic "1" Output Voltage	4.5		V	All outputs except $\overline{DP}$, $\overline{MUTE}$, $\overline{PF}$, $I_O=-10\mu A$, $V_{DD}=5V$
	Current Levels				
I_{DD}	Quiescent Current		25	μA	Standby, $V_{DD}=5V$
I_{DD}	Operating Current		500	μA	All valid input combinations, $\overline{DP}$, $\overline{MUTE}$, $\overline{PF}$ outputs open $V_{DD}=5V$
I_{IH}	Input Current Any Pin (keyboard inputs)	10	100	μA	$V_{IN}=V_{DD}$, $V_{DD}=5V$
I_{IL}, I_{IH}	Input Current All Other Pins		100	μA	$V_{IN}=V_{SS}$ or V_{DD}, $V_{DD}=5V$
I_{OZ}	Output Current in High Impedance State		1 1	μA μA	$V_{DD}=5V$, $V_{OUT}=0V$ data outputs (D1-D4) $V_{DD}=5V$, $V_{OUT}=5V$
fo	Oscillator Frequency	4	10	kHz	$V_{DD}=5V$ (min. duty cycle 30/70)
Δfo/fo	Frequency Deviation	−3	+3	%	$V_{DD}-V_{SS}$ from 4.5V to 5.5V. Fixed R-C oscillator components $50k\Omega \leq R_M \leq 750k\Omega$; $1M\Omega \leq R_I \leq 5M\Omega$; $150pF \leq C_O$ 3000pF; 330pF most desirable value for C_O, fo < 10kHz over the operating temperature and unit-unit variations
C_{IN}	Input Capacitance, Any Pin		7.5	pF	
V_{TRIP}	Supply Voltage at which $\overline{PF}$ Output Goes Low	2.5	4.5	V	

The device power supply should always be turned on before the input signal sources, and the input signals should be turned off before the power supply is turned off ($V_{SS} \leq V_I \leq V_{DD}$ as a maximum limit). This rule will prevent over-dissipation and posible damage of the input-protection diode when the device power supply is grounded. Power should be applied to the device in "on hook" condition.

Functional Description

The S2562 is a CMOS controller designed for storing or retrieving, normal dialing, redialing or auto dialing and displaying of one of several telephone numbers. It is intended to be used with the AMI standard S5101 256x4 RAM that functions as a telephone number storage. A single S5101 RAM will store up to 32 8-digit or 16 16-digit telephone numbers. The S2562 can be programmed to work with either 8-digit or 16-digit numbers by means of the Number Length Select (NLS) input.

The S2562 uses an inexpensive, but accurate R-C oscillator as a time base from which the dialing rate and inter-digit pause duration (IDP) are derived. Different dialing rates and IDP durations can be implemented by simply adjusting the oscillator frequency. The dialing rate and IDP can be further changed by a 2:1 factor by means of the dialing rate select (DRS) and inter-digit pause select (IPS) inputs. Thus, for the oscillator frequency of 8kHz, dialing rates of 10 and 20 pps and IDP's of 400 and 800ms can be achieved. The mark/space ratio is fixed independent of the time base at 40/60. Over supply voltage (5V±10%), operating temperature range and unit-unit variations, timing accuracy of ±3% can be achieved. A mute output is also available for muting of the receiver during dial pulsing. See Figure 5 for timing relationship.

The S2562 can be programmed by means of the MODE input for dual tone signaling applications as well. In this mode, it can interface directly with the AMI standard S2559 Tone Generator to produce the required DTMF signals. The tone on/off rate during an auto dial operation in this mode is derived from the time base. For the oscillator frequency of 8kHz, a tone drive rate of 50ms on, 50ms off is obtained. Different rates can be implemented by adjusting the time base as desired. See Tables 2 and 3 for the various combinations. In the tone mode, the mute output is used to gate the tone generator on and off. The 8 address lines that are normally used for addressing the RAM are also used to address the tone generator row, column inputs. Figure 6 shows a typical system application.

The S2562 can perform the following functions:

Normal Dialing

The user enters the desired number digits through the keyboard after going off hook. Dial pulsing starts as soon as the first digit is entered. The entered digits are stored sequentially in the internal memory. Since the device is designed in a FIFO arrangement, digits can be entered at a rate considerably faster than the output rate. Digits can be entered approximately once every 50ms while the dialing rate may vary from 7 to 20 pps. Debouncing is provided on the keyboard entries to avoid false entries. The number entered is retained for future redial. Pauses may be entered when required in the dial sequence by pressing the "#" key, which provides access pauses for future redial. Any number of access pauses may be entered as long as the total entries do not exceed the total number of digits (8 or 16).

An update pulse is generated to update the display digit as a new entry is made.

Redialing

The last number entered is retained in the internal memory and can be redialed by going "off hook" and depressing the "redial" (RDL) key. The RDL key is a unique 2 of 12 matrix location (R5, C3). The number being redialed out is displayed as it is dialed out.

In the tone mode, the redial tone drive rate depends upon the time base as discussed before.

Storing of a Normally Dialed or Redialed Number into the External Memory

After the normal dialing or redialing operation, the telephone number can be stored in the external memory for future repertory dialing use by going on hook and initiating the following key sequence.

1. Push "store" (ST) button.
2. Depress the single digit key corresponding to the desired address location.

Note that the "ST" key is a unique 2 of 12 matrix location (R_5, C_1).

Storing of a Telephone Number into the External Memory

This operation is performed "on hook" and no outdialing occurs. A telephone number can be stored in the desired address location by initiating the following key sequence.

1. Push the "*" key (This instructs the device to accept a new number for storage into the internal memory).
2. Enter the digits (including any access pauses) corresponding to the desired number. Digits will be displayed as they are entered.
3. Push the "ST" key.
4. Push the single digit key corresponding to the desired address location.

The entire sequence can be repeated to store as many numbers as desired. However, any memory locations not addressed with a telephone number "store" operation must be addressed with the following sequence.

1. Push the "*" key.
2. Push the "ST" key.
3. Push the single digit key corresponding to the first unused memory location.
4. Push the "ST" key.

5. Push the single digit key corresponding to the next unused memory location.

Steps 4. and 5. are repeated until all remaining memory locations have been addressed.

It should be noted that accessing all memory locations is required only for initial system set-up. This insures that no memory location will contain invalid data from memory power-up. If a memory location were to have invalid, power-up induced data and that location was addressed by the S2562, the S2562 would enter a "Halt" state and cease its normal program activities. To exit from this condition it is necessary to go "on hook" and perform a "store" operation.

Displaying of a Stored Telephone Number

This is an "on hook" operation Either the last dialed number or the number stored in the external memory can be displayed one digit at a time. The key sequence for displaying the last dialed number is as follows:

Push the "RDL" key.

The number in the external memory can be displayed as follows:

1. Push the "R" key.
2. Push the single digit key corresponding to the desired address location.

Note that the "R" key is a unique 2 of 12 matrix location (R_5, C_2).

The number is displayed one digit at a time at a rate determined by the time base. With a time base of 8kHz the display will be on 500ms, off 500ms. The display is updated by producing an update pulse. The update pulse must be decoded with external logic (one inverter and one 2-input gate) as shown in Figure 6.

The display is blanked by outputting an illegal (non BDC) code such as 1111. The 4511-type BCD to 7 segment decoder driver latch will blank the display when the illegal code is detected. When other driver circuits are employed, external logic must be used to detect the illegal code. Table 4 gives a list of display codes used by S2562.

Repertory Dialing

This is the most common mode of usage and allows the user to dial automatically any number stored in the memory. This mode is initiated by the following key sequence after going off hook.

1. Push the "*" key.
2. Push the single digit key corresponding to the desired address location.

The number is displayed as it is dialed out. In the tone mode, the tone driver rate is dependent on the time base as described earlier.

Pause

Note that the out dialing in the repertory or redial operation continues unless an access pause is detected. The outpulsing will stop and resume only when the user terminates the access pause by pushing the "*" key again.

Power Fail Detection

This output is normally high. When the supply voltage falls below a predetermined value, it goes low. The output can then drive a suitable latching device that will switch the memory to either the tip and ring or an auxiliary battery supply.

Memory Expansion

The memory can be expanded by paralleling additional S5101 RAM's. External logic must be used to enable the desired RAM corresponding to a desired address location. The S2562 can drive up to 2 RAM's without the need of buffering address and data lines.

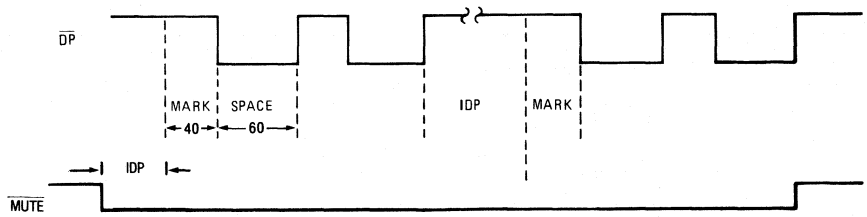
Keybounce Protection

When a key closure is detected by the S2562, an internal timeout (4ms at fo=8kHz) is started. Any transitions that occur during this timeout will reset the timer to zero so that a key will only be accepted as valid after a noise free timeout period. The key must remain closed for an additional 16ms before released. Thus, the total make time of the key must be at least 20ms. The key must be released for at least 1ms before a new key is activated. Any transitions occurring when the key is released are ignored as long as the make time does not exceed 4ms.

Function	Pin Designation	Input Logic Level	Selection
Dial Rate Selection	DRS	V_{SS} V_{DD}	(fo/800) pps (fo/400) pps
Inter-Digit Pause Selection	IPS	V_{DD} V_{SS}	(3200/fo) S (6400/fo) S
Test Input	TEST	V_{SS} V_{DD}	Test Mode Normal Mode
Hook Switch	$\overline{HS}$	V_{DD} V_{SS}	On Hook Off hook
Mode Selection	MODE	V_{SS} V_{DD}	Dial pulse Tone Drive*
Number Length Selection	NLS	V_{SS} V_{DD}	8 digits 16 digits

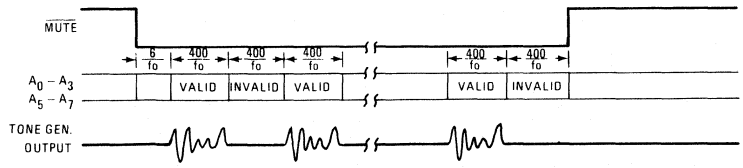
*For tone mode also set DRS=V_{SS}, IPS=V_{SS} and Test=V_{DD}.
Note: fo is the oscillator frequency and is determined as shown in Table 2.

Mute and Dial Pulse Output Timing Relationship



Mute will reset i) when the number of digits dialed out equals either the number of digits entered or the maximum selected (8 or 16) or ii) when an access pause is detected.

Figure 5B. Mute and Tone Output Timing Relationship



Mute output will reset i) when the number of digits dialed out equals the number of digits entered or equals the maximum selected (8 or 16) or ii) when an access pause is detected. In the normal dialing mode when digits are entered one at a time the mute output will reset between digits provided the time between entered digits exceeds $\frac{400}{fo}$. In both the normal dialing or automatic dialing mode tone will be output for a fixed duration of $\frac{400}{fo}$ (50msec for fo = 8kHz).

Figure 6. Typical Application of the S2562

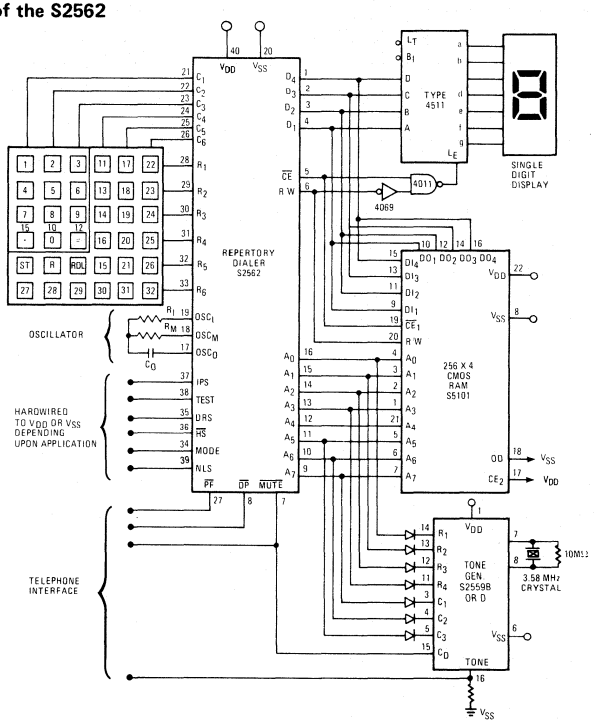


Table 4. Display Codes

D_4	D_3	D_2	D_1	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	Not Used
1	0	1	1	Not Used
1	1	0	0	# (Pause)
1	1	0	1	Not Used
1	1	1	0	Beginning of Number
1	1	1	1	Blank

AMERICAN MICROSYSTEMS, INC.

ADVANCED PRODUCT DESCRIPTION

S3501/S3501A, S3502/S3502A

SINGLE CHANNEL μ-LAW PCM CODEC/FILTER SET

COMMUNICATIONS

January 1980

Features

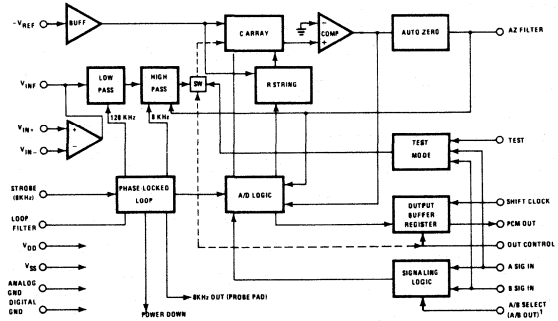
- ☐ **CMOS Process for Low Power Dissipation And Wide Supply Voltage Range**
- ☐ **Full Independent Encoder with Filter and Decoder with Filter Chip Set**
- ☐ **Meets or Exceeds AT&T D3 and CCITT G. 711 and G. 733 Specifications**
- ☐ **On-Chip Dual Band Width Phase-Lock Loop Derives All Timing and Provides Automatic Power Down**
- ☐ **Low Absolute Group and Relative Delay Distortion**
- ☐ **Single Negative Polarity Voltage Reference Input**
- ☐ **Encoder with Filter Chip Has Built-In Dual Speed Auto Zero Circuit with Rapid Acquisition During Power Up that Eliminates Long Term Drift Errors and Need for Trimming**
- ☐ **Serial Data Rates from 56kb/s to 3.152Mb/s at 8kHz Nominal Sampling Rate**
- ☐ **Programmable Gain Input/Output Amplifier Stage**
- ☐ **CCIS* Compatible A/B Signaling Option—S3501A/S3502A**

General Description

The S3501 and S3502 form a monolithic CMOS Companding Encoder/Decoder chip set designed to implement the per channel voice frequency CODECS used in PCM Channel Bank and PBX systems requiring a μ-255 law transfer characteristic. Each chip contains two sections: (1) a band-limiting filter, and (2) an analog ↔digital conversion circuit that conforms to the μ-255 law transfer characteristic. Transmission and reception of 8-bit data words containing the analog information is performed at 1.544Mb/s rate with analog sampling occurring at 8kHz rate. A strobe input is provided for synchronizing the transmission and reception of time multiplexed PCM information of several channels over a single transmission line.

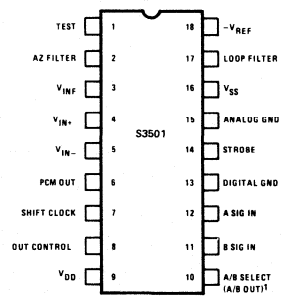
**Common Channel Interoffice Signaling*

S3501 Block Diagram Encoder with Filter



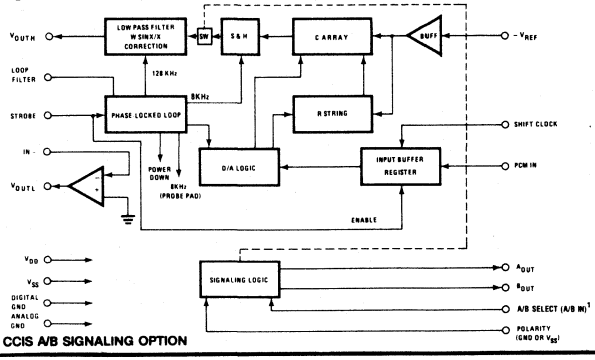
1 CCIS A/B SIGNALING OPTION

Pin Configuration



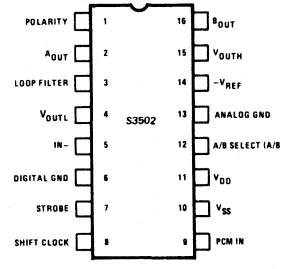
1 CCIS A/B SIGNALING OPTION-S3501A

S3502 Block Diagram Decoder with Filter



1 CCIS A/B SIGNALING OPTION

Pin Configuration



1 CCIS A/B SIGNALING OPTION-S3502A

S3501 Encoder with Filter Functional Description

S3501 Encoder with Filter chip consists of (1) a bandpass filter with D3 filter characteristic, (2) an analog to digital converter that uses a capacitor array, (3) a phaselock loop that generates all internal timing signals from the externally supplied strobe signal and (4) control logic that performs miscellaneous logic functions.

The band-limiting filter is a 5th order low pass elliptic filter followed by a third order Chebyshev high pass filter. The combined response characteristic (Figure 3) exceeds the D3 filter specifications. Note that the loss below 65Hz is at least 25dB which helps minimize the effect of power frequency induced noise.

The analog to digital converter utilizes a capacitor array based on charge redistribution technique (Ref. 1) to perform the analog to digital conversion with a μ-255 law transfer characteristic (see Figure 4).

The timing signals required for the band-pass filter (128kHz and 8kHz) and analog to digital converter (1.024MHz) are generated by a phase-lock loop comprising a VCO, a frequency divider, a loop filter and a lock detector. The loop locks to the externally supplied 8kHz strobe pulses. In the absence of the strobe pulses, the lock detector detects the unlocked condition and forces the device into a power-down mode thereby reducing power dissipation to a minimum. Thus power-down mode is easily implemented by simply gating the strobe pulses "off" when the channel is idle. The lock-up time, when strobe pulses are gated "on", is approximately 20ms. During this time the device outputs an idle code (all 1's) until lock-up is achieved. Note that signaling information is not transmitted during this time.

The control logic implements the loading of the output shift register, gating and shifting of the data word, signaling logic and other miscellaneous functions. A new analog sample is acquired on the rising edge of the strobe pulse. The data word representing the previous analog sample is loaded into the output shift register at this time and shifted out on the positive transitions of the shift clock during the strobe "on" time. (See Figure 1.) The signaling information is latched immediately after the A/B select input makes a transition. The "A" signaling input is selected after a positive transition and the "B"signaling input is selected after a negative transition. Signaling information is transmitted in the eighth bit position (LSB) of the next frame. (See Figures 1 and 2.) In the CCIS compatible A/B signaling option, the A bit is transmitted during the first data bit time. B bit is transmitted during the remaining 7-bit times. (See Figures 1 and 2.)

"All zero" code suppression is provided so that negative input signal values between the decision value numbers 127 and 128 are encoded as "00000010".

S3501 Encoder with Filter Pin Function Descriptions

Strobe: (Refer to Figure 1 for timing diagram.) This TTL compatible input is typically driven by a pulse stream of 8kHz rate. Its active state is defined as a logic 1 level and should be active for a duration of 8 clock cycles of the shift clock. A logic "1" initiates the following functions: (1) instructs the device to acquire a new analog sample on the rising edge of the signal (logic 0 to logic 1 transition); (2) instructs the device to output the data word representing the previous analog sample onto the PCM-out pin serially at the shift clock rate during its active state; (3) forces the PCM-out buffer into an active state. A logic "0" forces the PCM-out buffer into a high impedance state if the Out Control pin is wired to V_{DD}. This input provides the sync information to the phase-lock loop from which all internal timing is developed. The absence of the strobe conveys power-down status to the device. (See functional description of the phase-lock loop for details.)

Shift Clock: This TTL compatible input is typically a square wave signal at 1.544MHz. The device can operate with clock rates from 56kHz (as in the single channel 7-bit PCM system) to 3.152MHz (as in the T1-C carrier system). Data is shifted out of the PCM-out buffer on the rising edges of the clock after a valid logic 0 to logic 1 transition of the strobe signal.

PCM-Out: This is an open drain buffer capable of driving one low power Schottkey (74ls) TTL load with a suitable external pull-up resistor (1kΩ). This buffer is in active state (as controlled by the value of the data bit) whenever the strobe signal is a logic 1 and is in a high impedance state when the strobe input is a logic 0 and if the out control pin is wired to V_{DD} supply. When the out control is wired to V_{SS} the state of the output buffer is controlled by the value of the data bit being shifted out. For 56kHz and 64kHz PCM systems where output data is a continuous bit stream, the out control pin should be connected to V_{SS}.

A/B Select: (S3051 only) (Refer to Figure 2 for timing diagram.) This TTL compatible input is provided in order to select the path for the signaling information. It is a transition sensitive input. A positive transition on this input prior to the negative transition of the strobe input selects the "A" signaling input and is transmitted as the eighth bit in the subsequent frame. Similarly, a negative transition causes selection and transmission of informa-

tion on the "B" signaling input. Because it is a transition sensitive input, tying it to V_{DD} or V_{SS} disables A/B signaling.

A SIG IN, B SIG IN: These two TTL compatible inputs are provided to allow multiplexing of signaling information into the transmitted PCM data word in the eighth bit position in accordance with the timing diagram of Figure 2.

A/B Out: This is an open drain buffer capable of driving one low power Schottkey (74ls) TTL load with a suitable external pull-up resistor (5kΩ). This is an optional output for implementing CCIS compatible A/B signaling. (See Figure 2b.) During data bit 1 time, A signaling bit is output. During remaining 7-bit times, B signaling bit is output. This output is in a high impedance state when strobe is not present.

Out Control: This is a CMOS compatible input and must be wired to either the V_{DD} or V_{SS} (except in 'test' mode). When connected to the V_{DD} supply, it allows the strobe input to control the active/high impedance state of the PCM-out buffer. When connected to V_{SS}, the PCM-out buffer is always in the active state. For continuous analog-to-PCM operation at 56 or 64kb/sec, out control should be tied to V_{SS}.

V_{IN-}, V_{IN+}, V_{INF}: These three pins are provided for connecting analog signals in the range of $-V_{REF}$ to $+V_{REF}$ to the device. V_{IN-} and V_{IN+} are the inputs of a high input impedance op amp and V_{INF} is the output of this op amp. These three pins allow the user complete control over the input stage so that the input stage can be connected as a unity gain amplifier, amplifier with gain, amplifier with adjustable gain or as a differential input amplifier. The adjustable gain configuration will facilitate calibration of the transmit channel and testing of the encoder in a stand alone situation. The input stage also allows the user to construct an anti-aliasing filter to provide sufficient suppression at 128kHz. (See Design Considerations on page 13.)

$-V_{REF}$: The input provides the conversion reference for the analog to digital conversion circuit. a value of -3 volts is required. The reference must maintain 100ppM/°C regulation over the operating temperature range. A high input impedance buffer is provided on this input which facilitates bussing of the same reference voltage to several devices.

AZ Filter: A capacitor C_{AZ} (nominal .022μF) is required from this pin to analog ground for the functioning of the on-chip auto zero circuit. The most significant bit (sign bit) is filtered by the auto zero circuit and fed back to the input of the A/D converter to compensate for filter output offset variations. This technique insures that the long term average of the sign bit will be zero.

Analog Ground, Digital Ground: Two separate pins are provided for connection of analog signals referenced to analog ground and digital signals referenced to digital ground. This minimizes switching noise associated with the digital signals from affecting the analog signals.

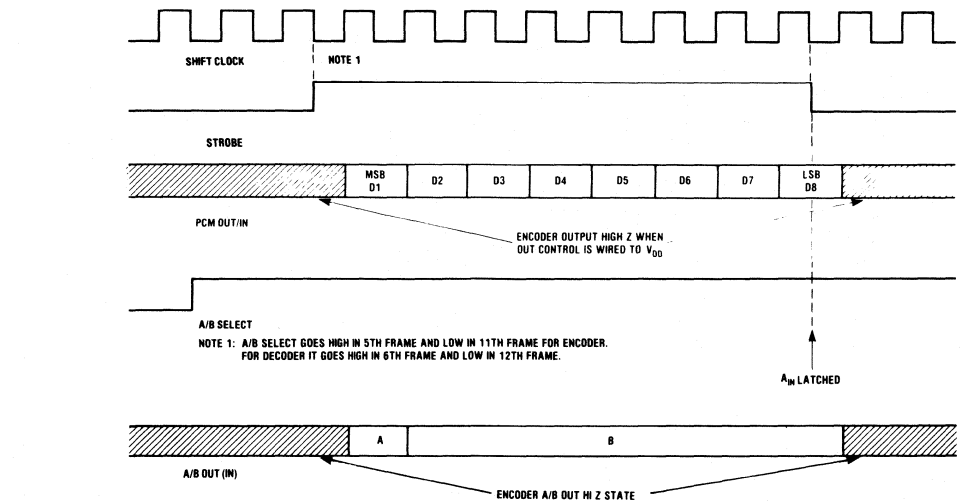
V_{DD}, V_{SS}: These are positive and negative supply pins.

Loop Filter: A capacitor C_{LOOP} (nominal .1μF) is required from this pin to digital ground to provide filtering of the phase comparator output.

Test: This pin is provided to allow for separate testing of the filter and encoder sections of the circuit. The circuit functions normally when this pin is connected to V_{SS}. When this pin is connected to V_{DD}, test mode results. In this mode when A SIG IN and B SIG IN inputs are connected to V_{SS} the filter output is disconnected from the encoder input. The encoder input is connected instead to the Out Control pin. For all other logical combinations of the A SIG IN and B SIG IN inputs the filter output is connected to the Out Control pin.

Ref. 1: *"A Two Chip PCM Voice CODEC with Filters,"* IEEE Journal of Solid State Circuits December 1979.

Figure 1-A. Typical Waveforms in a Time Multiplexed System



NOTE 2: IDLE CHANNEL NOISE CAN BE REDUCED BY AVOIDING COINCIDENCE BETWEEN THE FALLING EDGE OF THE SHIFT CLOCK AND RISING EDGE OF STROBE SIGNAL.

Figure 1-B. Waveform Detail

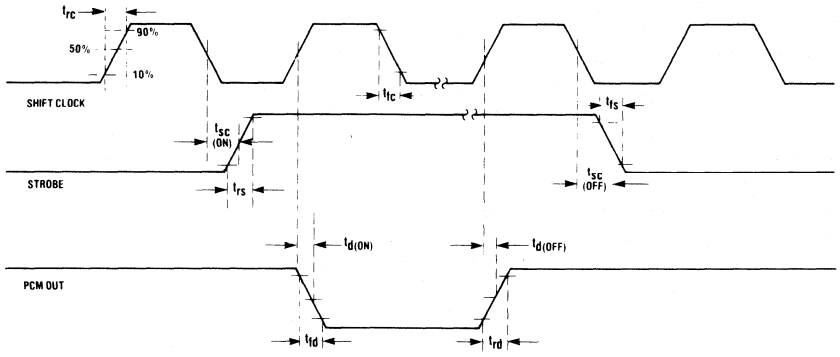
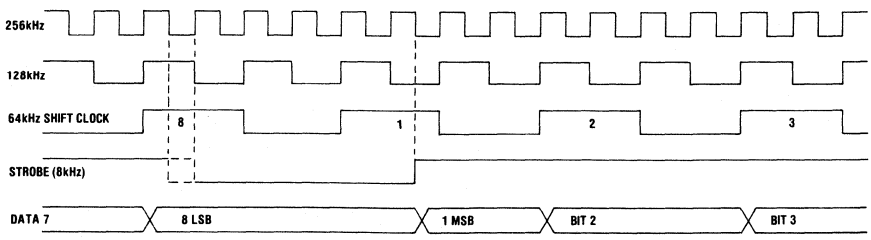
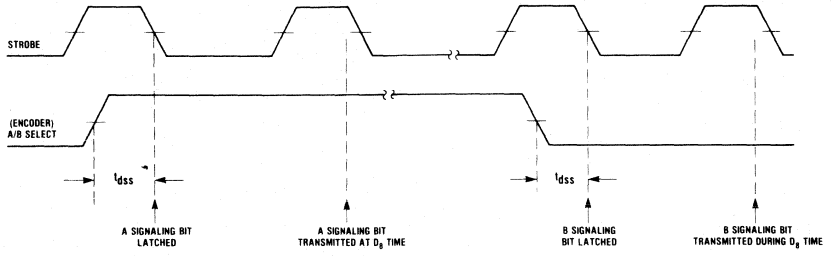


Figure 1-C. 64kHz Continuous Bit Stream Application



NOTES:
1. OUT CONTROL IS WIRED TO V_{SS} FOR CONTINUOUS BIT STREAM OPERATION.
2. THE NEGATIVE TIME OF THE STROBE SHOULD EXCEED ONE SHIFT CLOCK PERIOD.
3. THE CLOCK AND STROBE EDGES SHOULD BE SEPARATED BY AT LEAST 200ns.

Figure 2-A. Encoder A/B Signalling Waveforms



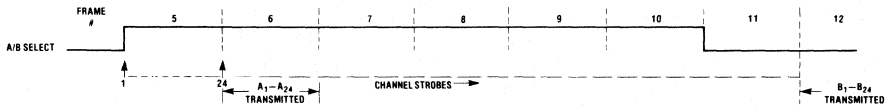


Figure 2-B. CODEC System Timing Diagram

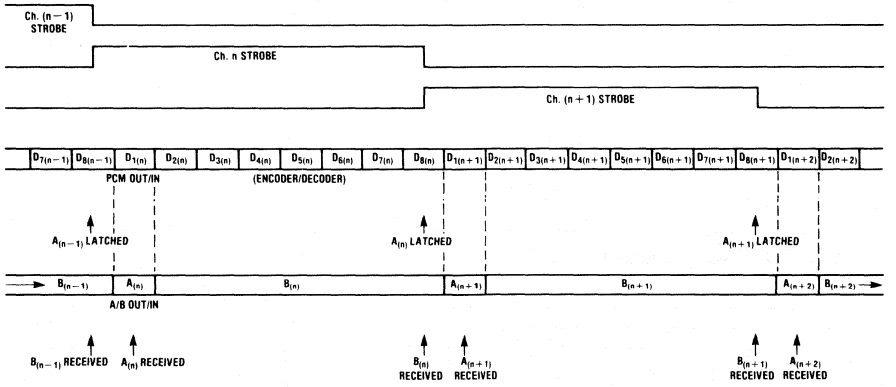
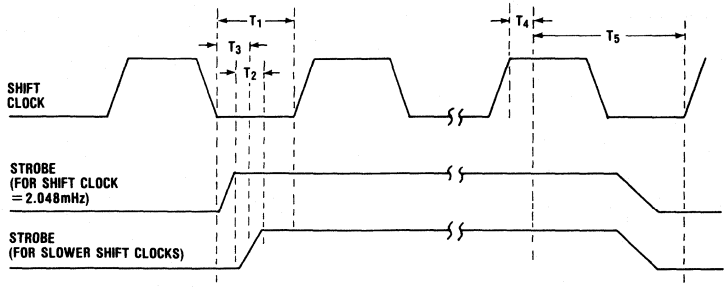


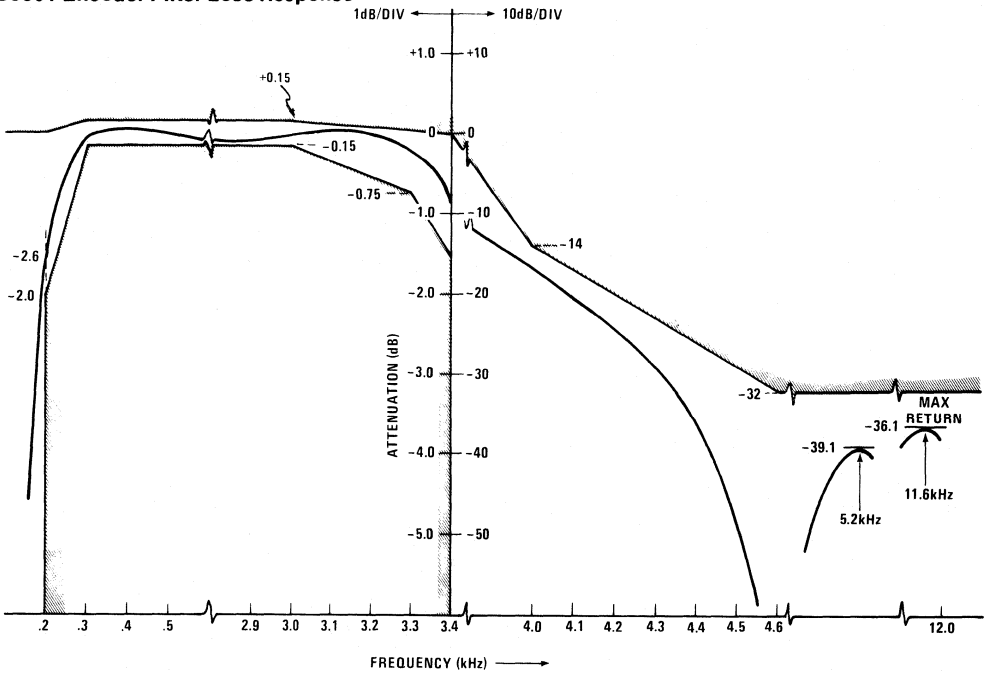
Figure 2-C.



NOTES:

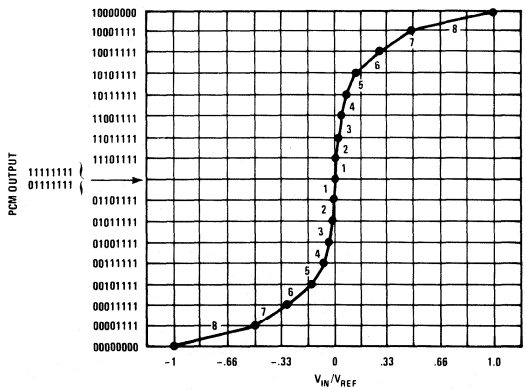
1. THE RISING EDGE OF THE STROBE MUST BE WITHIN T_1 AND THE FALLING EDGE WITHIN T_5. $T_4 = 200$ns.
2. FOR A 2.048mHz SHIFT CLOCK, IDLE CHANNEL NOISE WILL BE MINIMIZED IF THE RISING EDGE OF THE STROBE OCCURS IN T_3. $T_3 = 100$ns.
3. FOR SLOWER SHIFT CLOCK RATES, IDLE CHANNEL NOISE IS MINIMIZED IF THE RISING EDGE OCCURS IN T_2. FOR EXAMPLE, T_2 IS 125ns FOR A 1.544mHz SHIFT CLOCK.
4. ADJUSTING THE FALLING EDGE OF THE SHIFT CLOCK WILL NOT AFFECT IDLE CHANNEL NOISE.

Figure 3. S3501 Encoder Filter Loss Response

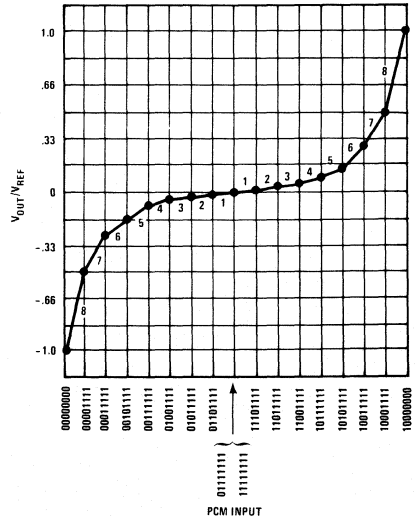


Note: Attenuation at frequencies below 65Hz is at least 25dB

Figure 4. μ-255 Law Transfer Characteristics



S3501 Transfer Characteristics



S3502 Transfer Characteristics

S3501 Absolute Maximum Ratings

DC Supply Voltage V_{DD}	+6.0V
DC Supply Voltage V_{SS}	−6.0V
Operating Temperature	0°C to +70°C
Storage Temperature	−55°C to +125°C
Power Dissipation at 25°C	250mW
Digital Input	$-0.3 \le V_{IN} \le V_{DD} + 0.3$
Analog Input	$-V_{REF} \le V_{IN} \le V_{REF}$
$-V_{REF}$	$V_{SS} \le V_{REF} \le 0$

S3501 Electrical Operating Characteristics ($T_A = 25°C$)

Power Supply Requirements

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V+	Positive Supply	4.75	5.0	5.25	V	See Figure 9
V−	Negative Suppply	−4.75	−5.0	−5.25	V	
$-V_{REF}$	Negative Reference	−2.4	−3	−3.25	V	
P_{OPR}	Power Dissipation (Operating)		60	100	mW	
P_{STBY}	Power Dissipation (Standby)		15		mW	

S3501 AC Characteristics (Refer to Figures 1 and 2)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
f_{SC}	Shift Clock Frequency	0.056	1.544	3.152	MHz	
D_{SC}	Shift Clock Duty Cycle	40	50	60	%	
t_{rc}	Shift Clock Rise Time			100	ns	
t_{fc}	Shift Clock Fall Time			100	ns	
t_{rs}	Strobe Rise Time			100	ns	
t_{fs}	Strobe Fall Time			100	ns	
t_{sc}(On)	Shift Clock to Strobe (On) Delay	0+		(1/2 CP)−	Shift Clock Period	
t_{sc} (Off)	Shift Clock to Strobe (Off) Delay	0+		(1/2 CP)−	Shift Clock Period	
t_d (On)	Shift Clock to PCM Out (On) Delay		140	170	ns	1kΩ, 50pF
t_d (Off)	Shift Clock to PCM Out (Off) Delay		140	170	ns	
t_{rd}	PCM Output Rise Time $C_L = 50pF$		100	125	ns	1kΩ Pull-Up on PCM Out selected for desired rise time
t_{fd}	PCM Output Fall Time $C_L = 50pF$		50	70	ns	
t_{dss}	A/B Select to Strobe Trailing Set Up Time	100			ns	
t_L	Phase-Lock Loop Lock Up Time		20	90	ms	
t_j	P—P Jitter of Strobe Rising Edge			5	μs	

S3501 Encoder DC Characteristics (5V Power Supply, $-V_{REF}=-3.0V$ see Figure 9.)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
R_{INA}	Analog Input Resistance	10			MΩ	V_{IN-}, V_{IN+} Inputs
C_{IN}	Input Capacitance			10	pF	V_{IN-}, V_{IN+},V_{INF} Inputs
I_{INL}	Logic Input Low Current (Shift Clock, Strobe)			1	μA	$V_{IL}=0.8V$
I_{INH}	Logic Input High Current			1	μA	$V_{IH}=2.0V$
V_{IL}	Logic Input "Low" Voltage			0.8	V	
V_{IH}	Logic Input "High" Voltage	2.2			V	
I_{REF-}	Negative Reference Current		150	300	nA	
R_{REF-}	Negative Reference Input Resistance	10			MΩ	
V_{OL}	Logic Output "Low" Voltage (PCM Out)			0.8	V	$I_{OL}=5mA$
V_{OL}	Logic Output "Low" Voltage (A/B Out)			0.8	V	$I_{OL}=.1mA$
I_{OH}	PCM Output Off Leakage Current			100	nA	$V_O=0$ to 5V

S3501 Analog Performance Characteristics

Parameter	Min.	Typ.	Max.	Unit	Condition Analog Input= (dBmO)
Signal to Distortion	35	40		dB	0
	35	40		dB	−20
	35	39		dB	−25
	35	38		dB	−30
	32	35		dB	−35
	29	32		dB	−40
	25	28		dB	−45
Gain Tracking		0±.02	±0.25	dB	−10
		0±0.02	±0.25	dB	−20
		0±0.03	±0.25	dB	−25
		0±0.03	±0.25	dB	−30
		−.02±0.04	±0.25	dB	−35
		−.02±0.06	±0.50	dB	−40
		−.02±0.09	±0.50	dB	−45
		−.02±0.13	±0.50	dB	−50
Idle Channel Noise		12.5	19	dBrncO	Analog Input to Analog GND

S3502 Decoder with Filter Functional Description

S3502 Decoder with Filter consists of (1) a digital to analog converter that uses a capacitor array; (2) a low pass filter with D3 filter characteristic; (3) a phase-lock loop that generates all internal timing signals from the externally supplied strobe signal and (4) control logic that performs miscellaneous logic functions.

The digital to analog converter uses a capacitor array based on charge redistribution technique (Ref. 1) to perform the D/A conversion with a μ-255 law transfer characteristic (See Figure 4).

The timing signals required for the low pass filter (128kHz) digital to analog converter (1.024MHz) are generated by a phase-lock loop comprised of a VCO, a frequency divider, a loop filter and a lock detector. The loop locks to the externally supplied 8kHz strobe pulses. In the absence of the strobe pulses, the lock detector detects the unlocked condition and forces the device into a power-down mode thereby reducing power dissipation to a minimum. Thus, power-down mode is easily implemented by simply gating the strobe pulses "off" when the channel is idle. During the power-down mode the output amplifier is forced to a high impedance state and the A, B outputs are forced to inactive state. The lock-up time, when strobe pulses are gated "on", is approximately 20ms. During this time the A/B outputs and the analog output stage are held in the idle state.

The control logic implements the loading of the input shift register, signaling logic and other miscellaneous functions. A new data word is shifted into the input register on a positive transition of the strobe signal at the shift clock rate. The received data is decoded by the D/A converter and applied to the sample and hold circuit. The output sample and hold circuit is filtered by a low pass filter. The low pass filter is a sixth order elliptic filter. The combined response of the sample and hold and the low pass filter is shown in Figure 5.

Signaling information is received and latched immediately after the A/B select input makes a positive or negative transition. On the positive transition of the A/B select input information received in the eighth bit of the data word is routed to the A_{OUT} pin and latched until updated again after the next positive transition of the A/B select input. Similarly "B" signaling information is routed and latched at the B_{OUT} pin after each negative transition of the A/B select input. The A and B outputs are designed such that either relay or TTL compatibility can be achieved (see detailed description under Pin/Function descriptions). In the CCIS compatible A/B signaling option. "A" bit is latched during the data bit 1 time and "B" bit is latched during the data bit 8 time.

S3502 Decoder with Filter Pin/Functions Descriptions

Strobe: (Refer to Figure 1 for timing diagram.) This TTL compatible input is typically driven by a pulse stream of 8kHz rate. Its active state is defined as a logic 1 level and is normaly active for a duration of 8 clock cycles of the shift clock. It initiates the following functions: (1) instructs the device to receive a PCM data word serially on PCM IN pin at the shift clock rate; (2) supplies sync information to the phase-lock loop from which all internal timing is generated; (3) conveys power-down mode to the device by its absence. (See functional description of the phase-lock loop for details.)

Shift Clock: This TTL compatible input is typically a square wave signal at 1.544MHz. The device can operate with clock rates from 56kHz (as in the single channel 7-bit PCM system) to 3.152MHz (as in the T1-C carrier system). Data is shifted in the PCM IN buffer on the falling edges of the clock after the strobe signal makes a logic 0 to logic 1 transition.

PCM IN: This is a TTL compatible input on which time multiplexed PCM data is received serially at the shift clock rate during the active state of the strobe signal.

A/B Select: (Refer to Figure 6 for timing diagram.) This TTL compatible input is provided in order to select the path for the signaling information. It is a transition sensitive input. A positive transition on this input routes the received signaling bit to the "A" output and a negative transition routes it to the "B" output.

A Out, B Out: These two open drain outputs are provided to output received signaling information. These outputs are designed in such a way that either LS TTL or relay drive compatibility can be achieved. With a suitable pull-up resistor (47KΩ) connected to the LS TTL logic supply, the output voltage will swing between digital ground and the LS TTL logic supply when the polarity pin is connected to digital ground. (See Figure 6.) The output polarity is the same as the received signaling bit polarity. If the polarity pin is connected to the V_{SS} supply, the output voltage will swing between V_{SS} and V_{DD} supplies with a suitable pull-up resistor. This facilitates driving a relay by a PNP emitter grounded transistor in -48V systems. The output polarities are inverted from the received signaling bit polarity to facilitate relay driving.

Polarity: This pin is provided for testing purposes and for controlling the A/B output polarities and TTL/relay drive

compatibilities. For TTL compatibility this pin is connected to digital ground. The A/B output polarities are then the same as the received signaling bit polarities. For relay drive capability this pin is connected to the V_{SS} supply. The A/B output polarities then are inverted from the received signaling bit polarities. Test mode results when this pin is connected to V_{DD}. In this mode the decoder output (S&H output) is connected to the B-Out pin while the filter input is connected to the A-Out pin.

$-V_{REF}$: The input provides the conversion reference for the digital to analog conversion circuit and the phase-lock loop. The reference must maintain 100ppM/°C regulation over the operating temperature range. A high input impedance buffer is provided on this input which facilitates bussing of the same reference voltage to several devices.

V_{OUTH}: This is the output of the low pass filter which represents the recreated voice signal from the received PCM data words. This is a high impedance output which can be used by itself or connected to the output amplifier stage which has a low output impedance.

V_{OUTL}, IN−: These two pins are the output and input of the uncommitted output amplifier stage. Signal at the V_{OUTH} pin can be connected to this amplifier to realize a low output impedance with the unity gain, increased gain or reduced gain. This allows easier calibration of the receive channel and testing of the decoder in a stand alone situation.

Analog Ground, Digital Ground: Two separate pins are provided for connection of analog signals referenced to analog ground and digital signals referenced to digital ground. This minimizes switching noise associated with the digital signals from affecting the analog signals.

V_{DD}, V_{SS}: These are the positive and negative power supply pins.

Loop Filter: A capacitor C_{LOOP} (nominal .1μF) is required from this pin to digital ground to provide filtering of the phase comparator output.

A/B IN: This optional TTL compatible input is provided to implement CCIS compatible A/B signaling scheme.Time multiplexed A, B signaling information is applied at this input and recovered by the decoder as shown in Figure 2-b.

S3502 Absolute Maximum Ratings

DC Supply Voltage V_{DD}	+6.0V
DC Supply Voltage V_{SS}	−6.0V
Operating Temperature	0°C to +70°C
Storage Temperature	−55°C to +125°C
Power Dissipation at 25°C	250mW
Digital Input	$-0.3 \le V_{IN} \le V_{DD} + 0.3$
Analog Input	$-V_{REF} \le V_{IN} \le V_{REF}$
$-V_{REF}$	$V_{SS} \le V_{REF} \le 0$

S3502 Electrical Operating Characteristics ($T_A = 25°C$)
Power Supply Requirements

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V+	Positive Supply	4.75	5.0	5.25	V	See Figure 11
V−	Negative Supply	−4.75	−5.0	−5.25	V	
$-V_{REF}$	Negative Reference	−2.4	−3	−3.25	V	
P_{OPR}	Power Dissipation (Operating)		60	100	mW	
P_{STBY}	Power Dissipation (Standby)		15		mW	

Figure 5. S3502 Decoder Filter with Sample & Hold Loss Response

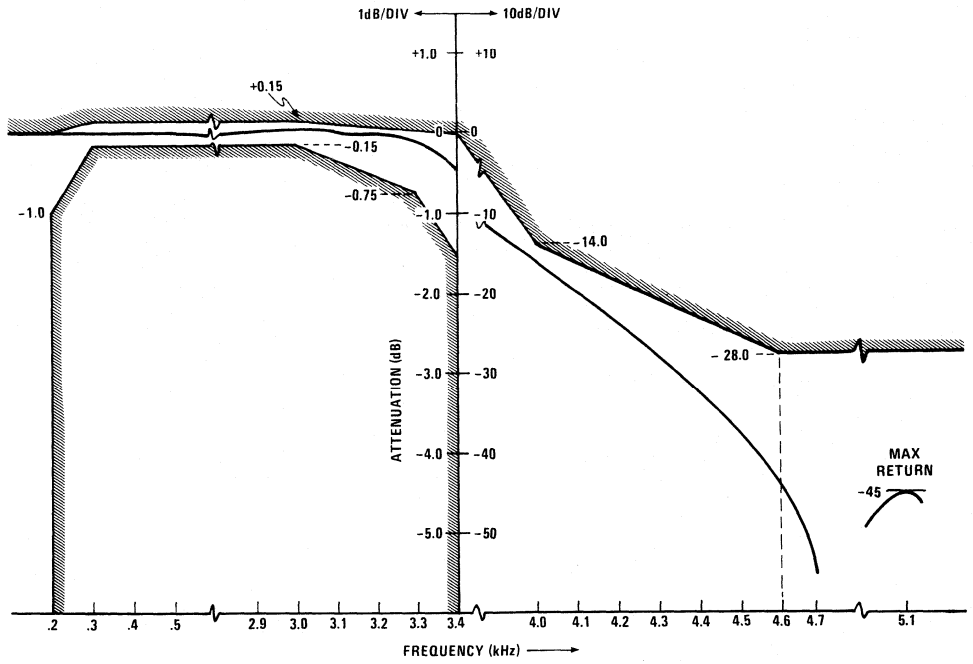
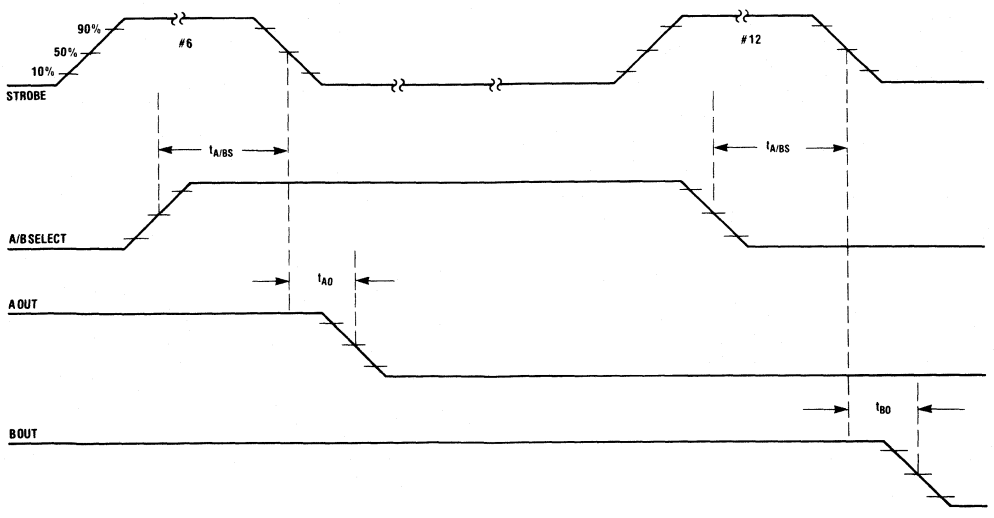


Figure 6. Decoder A/B Output Timing



S3502 AC Characteristics (Refer to Figures 1 and 6)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
f_{SC}	Shift Clock Frequency	0.056	1.544	3.152	MHz	
D_{SC}	Shift Clock Duty Cycle	40	50	60	%	
t_{rc}	Shift Clock Rise Time			100	ns	
t_{fc}	Shift Clock Fall Time			100	ns	
t_{rs}	Strobe Rise Time			100	ns	
t_{fs}	Strobe Fall Time			100	ns	
t_{sc}(On)	Shift Clock to Strobe (On) Delay	0+		(1/2 CP)−	Shift Clock Period	
t_{sc} (Off)	Shift Clock to Strobe (Off) Delay	0+		(1/2 CP)−	Shift Clock Period	
t_{rd}	PCM Input Rise Time			100	ns	
t_{fd}	PCM Input Fall Time			100	ns	
t_L	Phase-Lock Loop Lock Up Time		20	90	ms	
t_j	P—P Jitter of Strobe Rising Edge			5	μs	
t_s	PCM Input Setup Time	100			ns	
$t_{A/BS}$	A/B Select Set Up Time to Strobe Trailing Edge	100			ns	
t_{AO}, t_{BO}	Strobe Falling Edge to A/B Out Delay			200	ns	

S3502 Decoder DC Characteristics 5V Power Supply, $-V_{REF} = -3.0V$ (see Figure 11).

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$R_L(V_{OUTL})$	Output Load Resistance	600			Ω	
R_{INA}(IN−)	Analog Input Resistance	10			MΩ	
C_{INA}(IN−)	Analog Input Capacitance			10	pF	
I_{REF-}	Negative Reference Current		150	300	nA	
R_{REF-}	Negative Reference Input Resistance	10			MΩ	
V_{IL}	Logic Input (Shift Clock, Strobe, PCM In) "Low" Voltage			0.8	V	
V_{IH}	Logic Input "High" Voltage	2.0			V	
I_{INL}	Logic Input "Low" Current			1	μA	V_{IL}=0.8V
I_{INH}	Logic Input "High" Current			1	μA	V_{IH}=2.0V
V_{OL}	A, B Output "Low" Voltage			0.8	V	Polarity=Dig. Gnd, I_{OL}=1mA
V_{OL}	A, B Output "Low" Voltage			V_{SS}+1.0	V	Polarity=V_{SS}, I_{OL}=1mA

S3502 Analog Performance Characteristics

Parameter	Min.	Typ.	Max.	Unit	Condition Analog Input = (dBmO)
Signal to Distortion	35	40		dB	0
	35	40		dB	−20
	35	38.5		dB	−25
	35	39		dB	−30
	32	36.5		dB	−35
	29	33.5		dB	−40
	25	29		dB	−45
Gain Tracking		.02±.02	±0.25	dB	−10
		.04±.02	±0.25	dB	−20
		.04±.03	±0.25	dB	−25
		.03±.03	±0.25	dB	−30
		.04±.04	±0.25	dB	−35
		.04±.05	±0.50	dB	−40
		.1±.05	±0.50	dB	−45
		.15±.07	±0.50	dB	−50
Idle Channel Noise		9	13	dBrncO	PCM Input to Analog GND
0 Transmission Level Point (Digital Milliwatt Response)		5.3		dBm	−3V V_{REF} 600Ω Load

S3501/S3502 System Characteristics
Typical Group Delay Characteristic

Device	Abs. Gr. Delay μs f = 1000Hz	Abs. Gr. Delay μs f = 2600Hz	Relative Gr. Delay Distortion (Over Band of 1000 Hz to 2600Hz wrt 1000Hz) μs
Encoder Low Pass	132	220	88
Encoder High Pass	104	22	−82
Encoder Total	236	242	6
Decoder Low Pass	153	250	97
Encoder + Decoder (Total)	389	492	103
End to End Group Delay (Encoder Analog Input to Decoder Analog Output)	639	742	103

Design Considerations

Because the Codec set is required to handle signals with a very large dynamic range, optimal analog performance requires careful attention to the layout of components:

The analog ground, digital ground, V_{DD} and V_{SS} busses should run independently to the power supply, or at least to the edge connector. They should be separate for each chip and should be kept as wide as possible on the printed circuit.

The connections should be as independent as possible. For example (see Figure 7), the 750Ω pull-up resistor to Pin 6 should join the V_{DD} supply at the edge connector and not at the device pin.

Decoupling capacitors should be as close as possible to the power supply pin and analog ground pin.

Digital signal lines should be kept away from analog signals, and separated by an analog ground line where possible for shielding.

3501/3501A Design Guidelines

A recommended S3501 schematic is shown in Figure 7. Parts of the circuit are discussed in more detail below.

Loop Filter Network—For shift clock rates above 512kHz the network in Figure 8 is recommended. For 512kHz or below a .1μF capacitor between pins 13 and 17 is sufficient.

Supply Decoupling—Figure 9 shows the recommended power supply decoupling circuits. The diodes are essential for ±5V power supplies.

Reference Voltage—pin 18, requires a .1μF capacitor to analog ground. Pin 2, AZ filter, requires a .022μF capacitor to analog ground in parallel with 10MΩ resistor.

Anti-Aliasing

In applications where anti-aliasing pre-filtering is required, an on-chip op-amp may be configured into an active filter (Figure 10). Note that small changes in gain can be made by adjusting the resistor ratio R_1/R_2. Where anti-aliasing is not needed, a 3KΩ-4KΩ resistor can be connected between pins 3 and 5 (inverted gain configuration).

S3502/S3502A Design Guidelines

Figure 11 depicts a recommended S3502 circuit. All of the following comments apply to Figure 11:

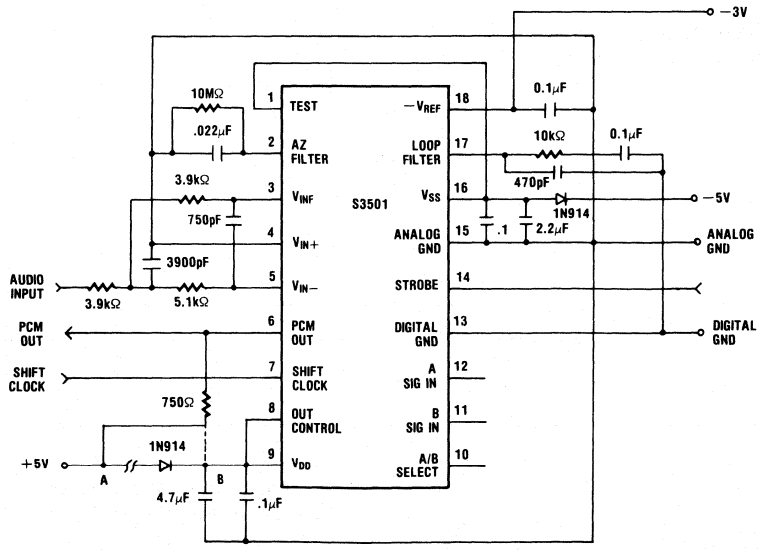
B_{OUT} is connected to V_{DD} at either point X or Y. For ±5V power supplies position Y is recommended. For larger power supplies position X should be used to prevent forward biasing of pins 2 and 16. R should be larger than 10KΩ to reduce noise.

When pin 1 is connected to DGND (non-inverted signalling with T²L output levels; not shown in Figure 11), R> 47KΩ.

Pin 1 should be connected to Pin 10, and not just to −5V, to avoid forward biasing the pin.

The 51KΩ output amplifier resistors should be carefully positioned away from the digital signals.

Figure 7. Hookup Schematic for S3501 Using 1.544mHz Shift Clock Rate



NOTES:
1. FOR ±5V POWER SUPPLIES POSITION A IS RECOMMENDED.
2. FOR LARGER POWER SUPPLIES POSITION B SHOULD BE USED TO PREVENT FORWARD BIASING OF PIN 6.
3. TEST PIN 1 MUST BE CONNECTED TO PIN 16 (NOT −5V) TO PREVENT FORWARD BIASING THE PIN.

Figure 8. Selection of Loop Filter Network

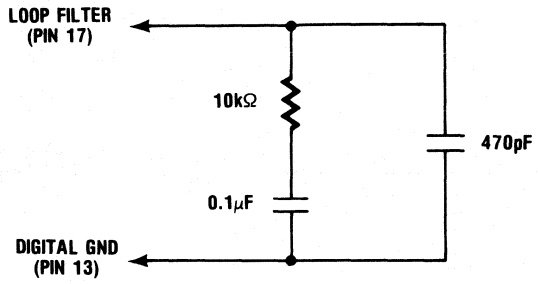


Figure 9-A. Supply Decoupling for the V_{DD} Supply Pin

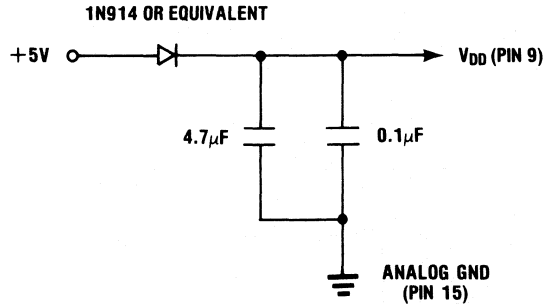


Figure 9-B. Supply Decoupling for the V_{SS} Supply Pin

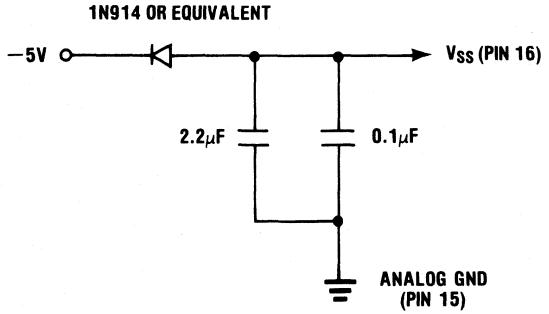


Figure 10. Anti-Aliasing Filter

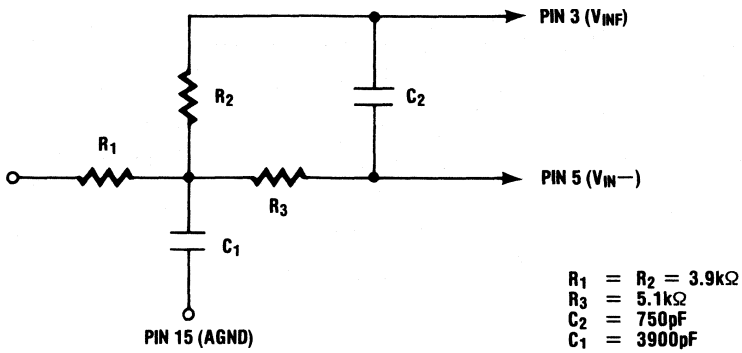
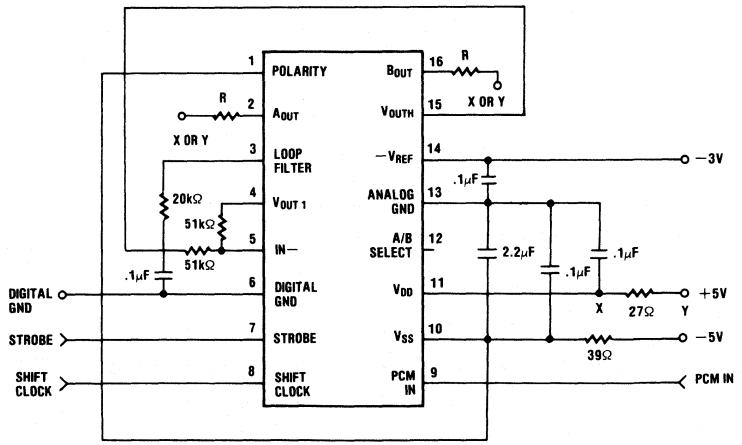


Figure 11. Hookup Schematic for S3502 Using 1.544mHz Shift Clock Rate



AMERICAN MICROSYSTEMS, INC.

ADVANCED PRODUCT DESCRIPTION

S3503/S3504

SINGLE CHANNEL A-LAW PCM CODEC/FILTER SET

COMMUNICATIONS

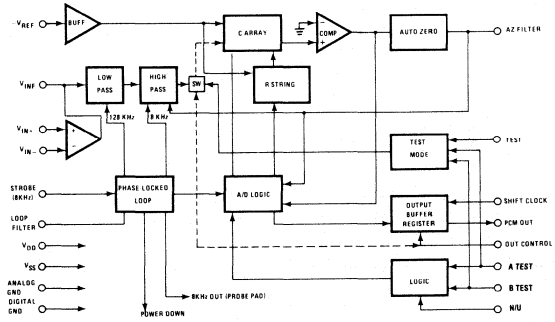
Features

- ☐ CMOS Process, for Low Power Dissipation and Wide Supply Voltage Range
- ☐ Full Independent Encoder with Filter and Decoder with Filter Chip Set
- ☐ Meets or Exceeds CCITT G. 711, G.712 and G. 733 Specifications
- ☐ On-Chip Dual Band Width Phase-Lock Loop Derives All Timing and Provides Automatic Power Down
- ☐ Low Absolute Group and Relative Delay Distortion
- ☐ Single Negative Polarity Voltage Reference Input
- ☐ Encoder with Filter Chip Has Built-In Dual Speed Auto Zero Circuit with Rapid Acquisition During Power Up that Eliminates Long Term Drift Errors and Need for Trimming
- ☐ Serial Data Rates from 56kb/s to 3.152Mb/s at 8kHz Nominal Sampling Rate
- ☐ Programmable Gain Input/Output Amplifier Stage

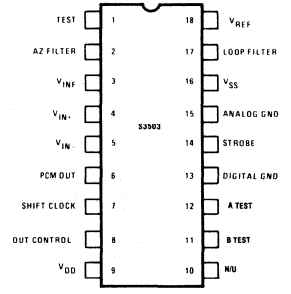
General Description

The S3503 and S3504 form a monolithic CMOS Companding Encoder/Decoder chip set designed to implement the per channel voice frequency CODECS used in PCM systems requiring an A-law transfer characteristic. Each chip contains two sections: (1) a band-limiting filter, and (2) an analog ↔ digital conversion circuit that conforms to the A-law transfer characteristic. Typical transmission and reception of 8-bit data words containing the analog information is performed at 2.048Mb/s rate with analog sampling occurring at 8kHz rate. A strobe input is provided for synchronizing the transmission and reception of time multiplexed PCM information of several channels over a single transmission line. These chips are pin-for-pin replacements for the S3501/S3502 chip set with the exception of the A-law transfer characteristic conforming to CCITT G. 711 and the unused signaling capability which remains available for special applications.

S3503 Block Diagram Encoder With Filter

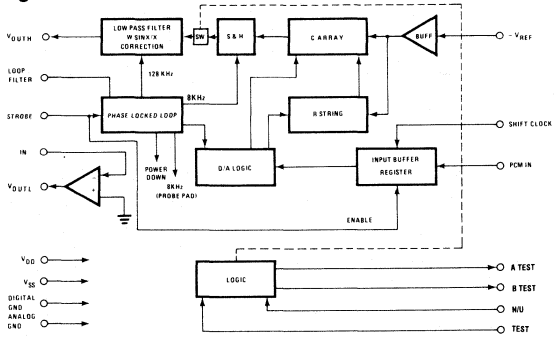


Pin Configuration

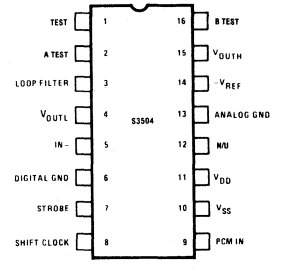


PIN 10, 11, 12 TO V_{DD} FOR NORMAL OPERATION

S3504 Block Diagram Decoder with Filter



Pin Configuration



PIN 1 TO DIGITAL GROUND, PIN 2, 16 OPEN FOR NORMAL OPERATION

AMERICAN MICROSYSTEMS, INC.

ADVANCED PRODUCT DESCRIPTION

S3505/S3505A

SINGLE CHIP μ-LAW PCM CODEC WITH FILTERS

Features

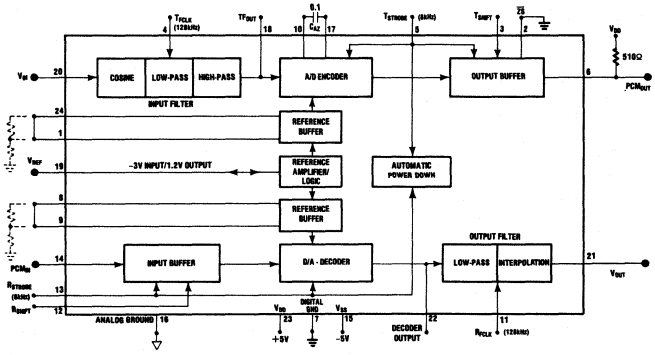
- ☐ Independent Transmit (Coder/Filter) and Receive (Decoder/Filter) Sections
- ☐ Internal Stable Voltage Reference (S3505)
- ☐ Transmit/Receive Isolation of at Least 75dB
- ☐ Meets or Exceeds AT&T D3 Channelbank and CCITT G.711 and G.733 Specifications
- ☐ Input Cosine Filter Eliminates Need for External Anti-Aliasing Prefilter
- ☐ Two Package Configurations:
  S3505, 24 Pin: Int/Ext V_{REF} Operation
  No Signaling
  S3505A, 28 Pin: Ext V_{REF}
  A/B Signaling
- ☐ Minimum Parts Count
  0.1μF Auto Zero Capacitor
  510Ω PCM Out Pullup Resistor

General Description

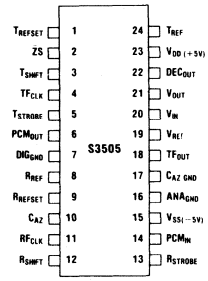
The S3505/S3505A is a single chip μ-law PCM codec with filters designed in a silicon gate CMOS process. It provides the interface between the analog signals of the subscriber loop and digital signals of the PCM highway in a digital telephone switching system. The device operates from dual power supplies of ±5V, ±5% requiring minimum supply decoupling (Typ 2.2μF).

For a sampling rate of 8kHz, PCM input/output data rate can vary from 64Kb/s to 2.1Mb/s. Separate filter clock inputs (nom. 128kHz) control the transmit and

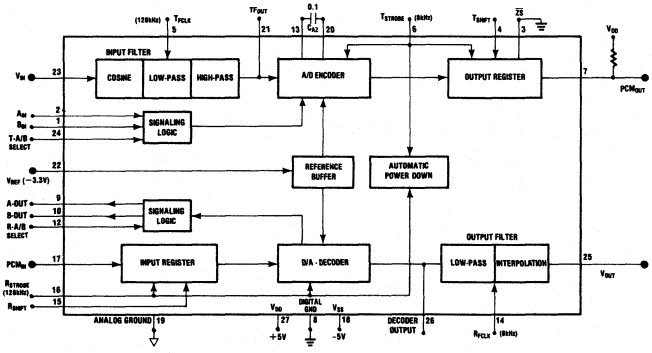
S3505 Block Diagram



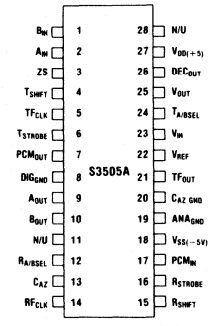
S3505 Pin Configuration



S3505A Block Diagram



S3505A Pin Configuration



receive filter characteristics. Separate transmit/receive timing allows synchronous or asynchronous operation.

The 24-pin S3505 without signaling is intended for PABX and digital telephone applications while the 28-pin S3505A with A/B signaling is more suited for central office/channelbank applications.

Pin Function/Descriptions

PIN	S3505	S3505A	DESCRIPTION
$\overline{ZS}$	2	3	($\overline{\text{Zero Supression}}$): Connection to digital ground enables the zero suppression feature. The all zero code words corresponding to negative signal values exceeding the decision value number 127 are encoded as "00000010".
T_{SHIFT}	3	4	(Transmit Shift Clock): This TTL compatible input shifts PCM data out of the coder on the positive going edges after receiving a positive edge on the T_{STROBE} Input. The clocking rate can vary from 64kHz to 2.1MHz.
R_{SHIFT}	12	15	(Receive Shift Clock): This TTL compatible input shifts PCM data into the decoder on the negative going edges after receiving a positive edge on the R_{STROBE} input. The clocking rate can vary from 64kHz to 2.1MHz.
T_{STROBE}	5	6	(Transmit Strobe): This TTL compatible pulse input (typ. 8kHz) is used for analog sampling and for initiating the PCM output from the coder. It must be synchronized with the T_{SHIFT} clock with its positive going edges occurring after the falling edge of the shift clock. The width of this signal is not critical. An internal bit counter generates the necessary timing for PCM output.
R_{STROBE}	13	16	(Receive Strobe): This TTL compatible pulse input (typ. 8kHz) initiates clocking of PCM Input data into the decoder. It must be synchronized with the R_{SHIFT} clock with its positive going edges occurring after the falling edge of the shift clock. The width of the signal is not critical. An internal bit counter generates necessary timing for PCM input.
TF_{CLK}	4	5	(Transmit Filter Clock): This TTL compatible input is a 128kHz square wave signal for transmit filter operation. It should be synchronized to the T_{SHIFT} clock.
RF_{CLK}	11	14	(Receive Filter Clock): This TTL compatible input is a 128kHz square wave signal for receive filter operation. It should be synchronized to the R_{SHIFT} clock.
PCM OUT	6	7	This is a LS-TTL compatible open-drain output. It is active only during transmission of PCM output for 8-bit periods of T_{SHIFT} clock signal following a positive edge on the T_{STROBE} input.
PCM IN	14	17	This is a TTL compatible input for supplying PCM input data to the decoder.
C_{AZ} C_{AZ} GND	10 17	13 20	(Auto Zero Capacitor): A capacitor of 0.1μF should be connected between these pins for coder auto zero operation. Sign bit of the PCM data is integrated and fed back to the comparator for DC offset cancellation.
V_{IN}	20	23	This is a high impedance input for connecting analog voice signal to the coder.
V_{OUT}	21	25	This is a low impedance analog output of the receive filter capable of driving a 600 ohm load.
TF OUT	18	21	This is a test point for transmit filter output.
DEC OUT	22	26	This is a test point for decoder output.

Pin Function/Descriptions

PIN	S3505	S3505A	DESCRIPTION
T_{REFSET} T_{REF} R_{REFSET} R_{REF} V_{REF}	1 24 9 8 19	 22	These pins provide for adjustment and setting of internal voltage reference for the transmit and receive sections of S3505. Output of the internal band-gap reference voltage generator is brought out to V_{REF} pin (typ. −1.2V). A desired reference value for the transmit section can be generated by connecting a resistor divider between T_{REF}, T_{REFSET} and Analog Ground pins. Similarly, a resistor divider connected between R_{REF}, R_{REFSET} and Analog Ground provides adjustment for reference voltage for receive section. See Figure 8 for details. The S3505 can be operated from an external voltage source also. This is done by forcing a voltage exceeding the internal V_{REF} voltage (−1.2V) into the V_{REF} pin and connecting T_{REFSET} to T_{REF} and R_{REFSET} to R_{REF} (See Figure 8). S3505A can be operated only with an external voltage source (typ. −3.3V) connected to V_{REF} pin.
A IN B IN T-A/B SEL	 	2 1 24	The transmit A/B select input selects the A signal input on a positive transition and the B signal input on the negative transition. These inputs are TTL compatible. The A/B signaling bits are sent in bit 8 of the PCM word in the frame following the frame in which T-A/B SEL input makes a transition. A common A/B select input can be used for all channels in a multiplex operation, since it is synchronized to the T_{STROBE} input in each device.
A OUT B OUT R-A/B SEL	 	9 10 12	In the decoder the A/B signaling bits received in the PCM input word are latched to the respective outputs in the same frame in which the R-A/B SEL input makes a transition. A bit is latched on a positive transition and B bit is latched on a negative transition. A common A/B select input can be used for all channels in a multiplex operation.
V_{DD} V_{SS} ANA GND DIG GND	23 15 16 7	27 18 19 8	These are power supply pins. V_{DD} and V_{SS} are positive and negative supply pins, respectively (typ. +5V, −5V). Analog and digital ground pins are separate for minimizing crosstalk.

Absolute Maximum Ratings

DC Supply Voltage V_{DD}	+6.0V
DC Supply Voltage V_{SS}	−6.0V
Operating Temperature	−20°C to +70°C
Storage Temperature	−55°C to +125°C
Power Dissipation at 25°C	1000mW
Digital Input	$V_{SS}-0.3 \le V_{IN} \le V_{DD}+0.3$
Analog Input	$V_{SS}-0.3 \le V_{IN} \le V_{DD}+0.3$

S3505 Electrical Operating Characteristics ($T_A = 25°C$)

Power Supply Requirements

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{DD}	Positive Supply	4.75	5.0	5.25	V	
V_{SS}	Negative Supply	−4.75	−5.0	−5.25	V	
P_{OPR}	Power Dissipation (Operating)		350	500	mW	$V_{DD}=5.0V$
P_{STBY}	Power Dissipation (Standby)		120		mW	$V_{SS}=-5.0V$

S3505 AC Characteristics (Refer to Figures 3 and 3A)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
f_{SC}	Shift Clock Frequency	0.064	1.544	2.048	MHz	
D_{SC}	Shift Clock Duty Cycle	40	50	60	%	
t_{rc}	Shift Clock Rise Time			100	ns	
t_{fc}	Shift Clock Fall Time			100	ns	
t_{rs}	Strobe Rise Time			100	ns	
t_{fs}	Strobe Fall Time			100	ns	
t_{sc}	Shift Clock Strobe (On) Delay	−100	0	100	ns	
t_{sw}	Strobe Width	200ns		124.8μs		
t_r(128)	128kHz Rise Time			100	ns	
t_f(128)	128kHz Fall Time			100	ns	
D(128)	128kHz Duty Cycle	40	50	60	%	
f (128)	128kHz Clock Frequency		128		kHz	Must be synchronous with 8kHz strobe
t_{cd}	Shift Clock to PCM Out Delay		100	150	ns	
t_{dc}	Shift Clock to PCM in Set-up Time	100			ns	
t_{rd}	PCM Output Rise Time C_L=100pF		30	100	ns	to 3V; 510Ω to V_{DD}
t_{fd}	PCM Output Fall Time C_L=100pF		30	100	ns	to .4V; 510Ω to V_{DD}
t_{dss}	A/B Select to Strobe Trailing Edge Set Up Time	100			ns	

S3505 DC Characteristics (V_{DD} = +5V, V_{SS} = −5V, V_{REF} = −3.1V unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
R_{INA}	Analog Input Resistance	100			KΩ	
C_{IN}	Input Capacitance			40	pF	All Logic and Analog Inputs
I_{INL}	Logic Input Low Current, (Shift Clock, 128kHz)			1	μA	V_{IL}=0.8V

S3505 DC Characteristics (Continued)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_{INH}	Logic Input High Current			1	μA	V_{IH}=2.0V
V_{IL}	Logic Input "Low" Voltage			0.8	V	
V_{IH}	Logic Input "High" Voltage	2.0			V	
V_{OL}	Logic Output "Low" Voltage (PCM Out)			0.4	V	510Ω Pull-up to V_{DD}
V_{OL}	Logic Output "Low" Voltage (A/B Out)			0.4	V	I_{OL}=1.6mA
V_{OH}	Logic Input "High" Voltage	2.6			V	I_{OH}=40μA
R_L	Output Load Resistance V_{OUT}	1200			Ω	

S3505/S3505A Single-Chip μ-Law Filter/Codec System Performance Goals

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
ICN_W	Idle Channel Noise (Weighted Noise)		15	17	dBRNCO	CCITT.G712 5.1
ICN_{SF}	Idle Channel Noise (Single Frequency Noise)			−60	dBMO	CCITT.G712 5.2
ICN_R	Idle Channel Noise (Receive Section)			15	dBRNCO	CCITT.G712 5.3
	Spurious Out-of-Band Signals at the Channel Output			−30	dBMO	CCITT.G712 7.1
IMD_{2F} IMD_{PF}	Inter Modulation (2 Tone Method) Inter Modulation (1 Tone + Power Frequency)			−35 −49	dBMO dBMO	CCITT.G712 8.1 CCITT.G712 8.2
	Spurious-In-Band Signals at the Channel Output Port			−40	dBMO	CCITT.G712 10
	Inter Channel Cross Talk $V_{IN}-V_{OUT}$	75	80		dB	CCITT.G712 12
$V_{IN(Max)}$	Max Coding Analog Input Level		0.628		V_{PK}	
$V_{OUT(Max)}$	Max Coding Analog Output Level		3.0		V_{PK}	R_L=1.2KΩ
ΔG	Gain Variation With Temperature and Power Supply			±0.25	dB	

S3505/S3505A Single-Chip μ-Law Filter/Codec System Performance Goals (Continued)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$0TLP_R$	Zero Transmission Level Point (Decoder) (See Figure 9)		+6.7		dBM	V_{OUT} Digital Milliwatt Response
$0TLP_T$	Zero Transmission Level Point (Encoder)		−6.8		dBM	V_{IN} To Yield Same as Digital Milliwatt Response at Decoder

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
	Transmission Delays					
	Encoder		125		μs	From T_{STROBE} To the Start of Digital Transmitting
	Decoder			8T+25	μs	T= Period in μs of R_{SHIFT} CLOCK
	Transmit Section Filter			271	μs	
	Receive Section Filter			102	μs	

Functional Description

Page 1 shows the simplified block diagrams of the S3505/S3505A respectively. The device contains independent circuitry for processing transmit and receive signals. Switched capacitor filters provide the necessary bandwidth limiting of voice signals in both directions. Circuitry for coding and decoding operates on the principle of successive approximation, using charge redistribution in a binary weighted capacitor array to define segments and a resistor chain to define steps. A band-gap voltage generator supplies the reference level for the conversion process.

Transmit Section

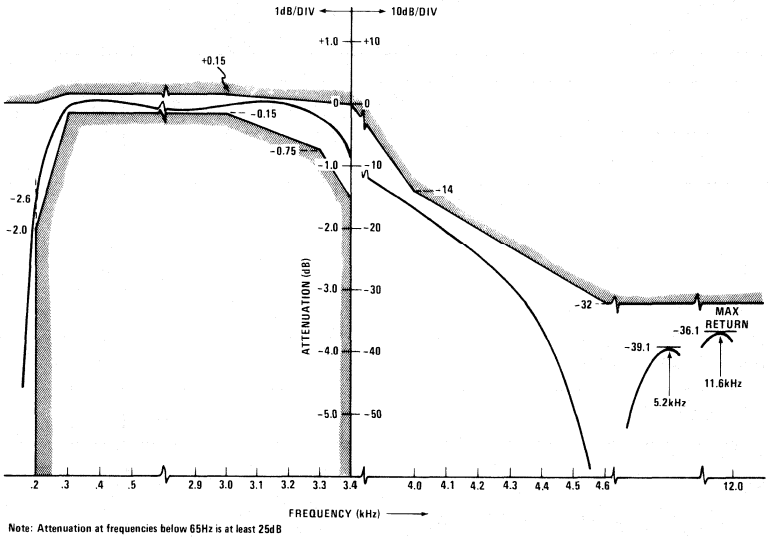
Input analog signals pass through the transmit filter which consists of a series combination of a cosine filter, a low-pass filter and a high-pass filter. The cosine filter, clocked at 128kHz, samples the analog signal at 256kHz and introduces a transmission zero at 128kHz. This technique considerably relaxes the requirements on an external anti-aliasing prefilter. The low-pass filter, clocked at 128kHz, limits the bandwidth of the input signal to about 3.4kHz. The high-pass filter clocked at 8kHz provides an attenuation of at least 25dB for signal frequencies below 65Hz to eliminate effects of power line induced noise. Output of the high-pass filter is sampled by a capacitor array at the sampling rate of 8kHz. Polarity of the incoming signal selects the appropriate polarity of the reference voltage. The successive approximation analog-to-digital conversion process requires three clock cycles to determine segment bits and four clock cycles to determine step bits. The total conversion time is nine clock cycles. For the 128kHz clock rate this corresponds to about 70μs. The 8-bit PCM data is clocked out by the transmit shift clock which can vary from 64kHz to 2.1MHz. A switched capacitor auto zero loop using a small external capacitor (0.1μF) provides DC offset cancellation by integrating the sign bit of the PCM data and feeding it back to the noninverting input of the comparator.

Receive Section

A receive shift clock, variable between the frequencies of 64kHz to 2.1MHz, clocks the PCM data into the input buffer register once every sampling period. A charge proportional to the received PCM data word appears on the decoder capacitor array. A sample and hold initialized to zero by a narrow pulse at the beginning of each sampling period integrates the charge and holds for the rest of the sampling period. A switched capacitor low-pass filter clocked at 128kHz smooths the sampled and held signal. It also performs the loss equalization to compensate for

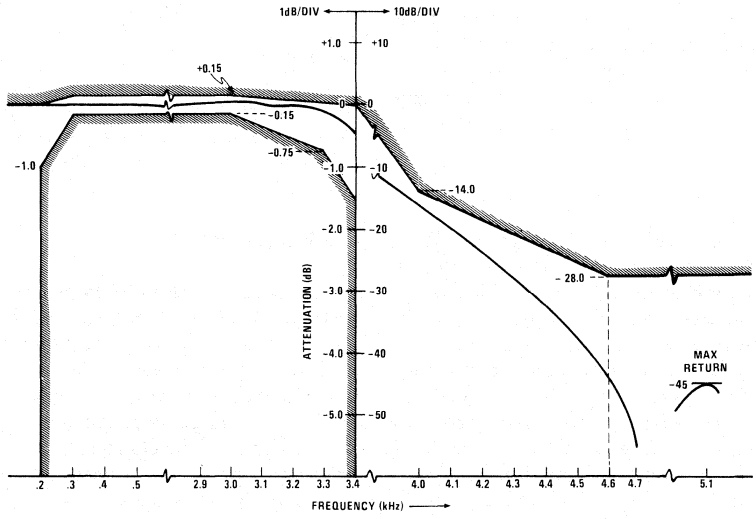
the sin x/x distortion due to the sample and hold operation. A novel switched capacitor interpolation filter further smooths the output of the low-pass filter. It interpolates between two consecutive samples and removes all components around 128kHz. The effect is an increase in the sampling rate to 256kHz. This technique eliminates the need for an external post filter for smoothing the received signal. The interpolation filter uses a low output impedance operational amplifier capable of driving a 600 ohms hybrid transformer.

Figure 1. Encoder Filter Loss Response



Note: Attenuation at frequencies below 65Hz is at least 25dB

Figure 2. Decoder Filter with Sample & Hold Loss Response



Signaling and Power Down Logic

The device contains circuitry to allow multiplexing of signaling information in the least significant bit of the PCM data word. It follows the standard A/B signaling format defined in the AT&T D3 channelbank specifications. Turning off the transmit and receive sampling strobes achieves power down.

Voltage Reference Circuitry

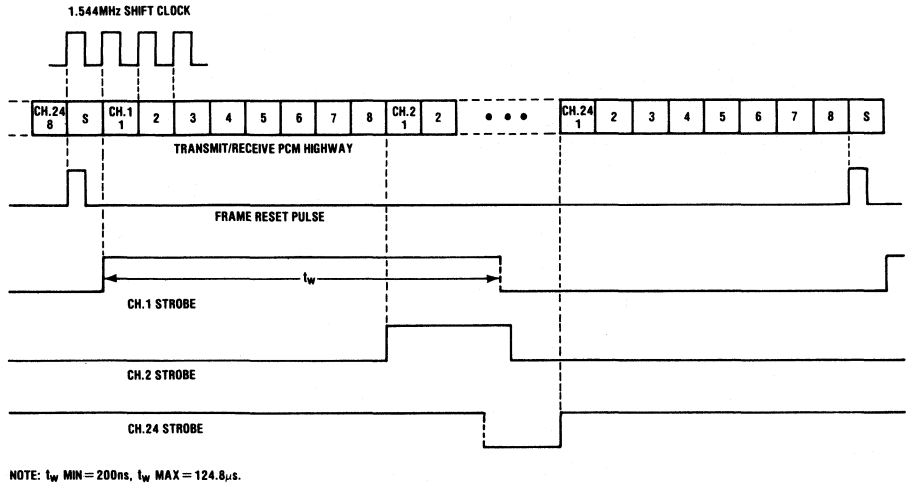
A temperature compensated bank-gap voltage generator (typ. −1.2 volts) provides a stable reference for the coder and decoder. Two amplifiers buffer the reference and supply the coder and decoder independently to minimize crosstalk. These also allow independent external gain adjustments. The device can also operate from an external reference, if the amplifiers are connected in a unity gain configuration and an external voltage exceeding −1.2V (typ −3.3V) is connected to the V_{REF} pin. (See Figure 8.)

Timing Requirements

The internal design of the Single-Chip Codec paid careful attention to the timing requirements of various systems. In North America, central office and channelbank designs follow the AT&T T1 carrier PCM format to multiplex 24 voice channels at a data rate of 1.544Mb/s. PABX designs, on the other hand, may use their own multiplexing formats with different data rates. Yet, in digital telephone designs, Codecs may be used in a non-multiplexed form with a data rate as low as 64Kb/s.

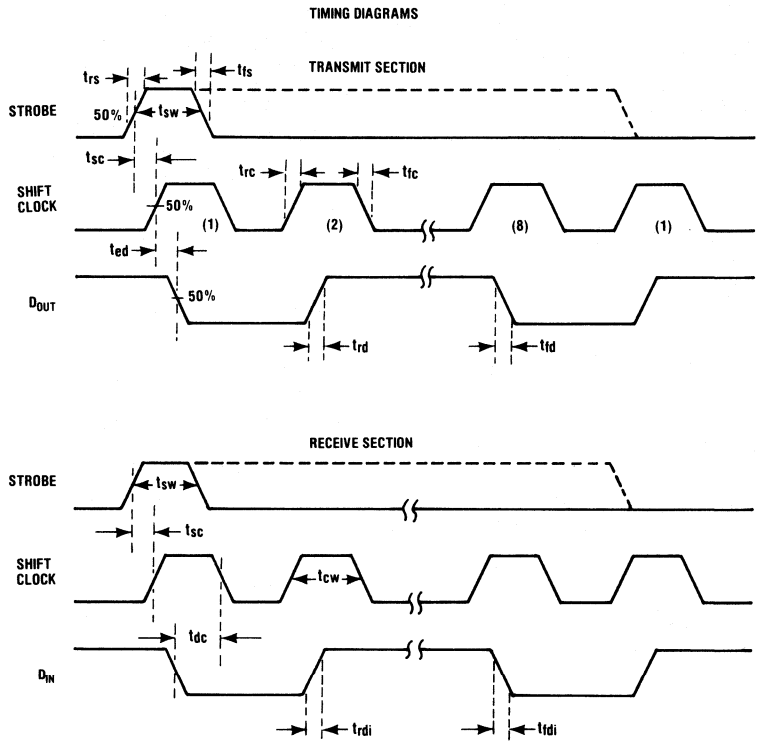
The timing format chosen for the AMI Codec allows operation in both multiplexed or non-multiplexed form with data rates variable from 64Kb/s to 2.1Mb/s. Use of separate clocks for filters and for shifting of PCM input/output data allows the variable data rate capability. Additionally, unlike other Codecs, the S3505 does not require that the 8kHz transmit and receive sampling strobes be exactly 8-bit periods wide. The device has an internal bit counter that counts the number of data bits shifted. It is reset on the leading edges of the strobe. It forces the PCM output in a high impedance state after the 8th bit is shifted out. This allows the strobe signal to have any duty cycle as long as its repetition rate is 8kHz and that the 128kHz filter clock and transmit/receive shift clocks are synchronized to it. Figure 3 shows the waveforms in typical multiplexed uses of the Codec.

Figure 3. Waveforms in a 24 Channel PCM System



NOTE: t_W MIN = 200ns, t_W MAX = 124.8μs.

Figure 3-A. Waveform Details



	MIN	MAX
t_{cw}	195nsec	9.38μsec
t_{rs}		100ns
t_{fs}		100ns
t_{sc}	−100ns	100ns
t_{rc}		100ns
t_{fc}		100ns
t_{sw}	t_{cw}	124.8μs
t_{dc}	100ns	
t_{rdi}		100ns
t_{fdi}		100ns

*SHIFT CLOCK DUTY CYCLE SHOULD BE BETWEEN 40% AND 60% OF 64kHz TO 2.048MHz

(WITH 8kHz FREQUENCY 64kHz CLOCK)

SIGNAL PROCESSING PERIPHERAL

Features

- ☐ High Speed VMOS Technology
- ☐ Programmable for Digital Processing of Signals in Voice-Grade Communications Systems and Other Applications with Signals in the Audio Frequency Range
- ☐ Extremely Fast 12-Bit Parallel Multiplier On-Chip (300ns Max. Multiplication Time)
- ☐ Built-in Program ROM (256x17)*, 3-Port Data Memory (256x16) and Add/Subtract Unit (ASU)
- ☐ Pipeline Structure for High Speed Instruction Execution (300ns Max. Cycle Time)
- ☐ Bus-Oriented Parallel I/O for Easy Microprocessor Interface
- ☐ Additional Double Buffered I/O for Ease of Asynchronous Serial Interface
- ☐ On-Chip Crystal Oscillator (20MHz) Circuit
- ☐ Pre-Programmed Standard Parts to Be Announced Shortly

General Description

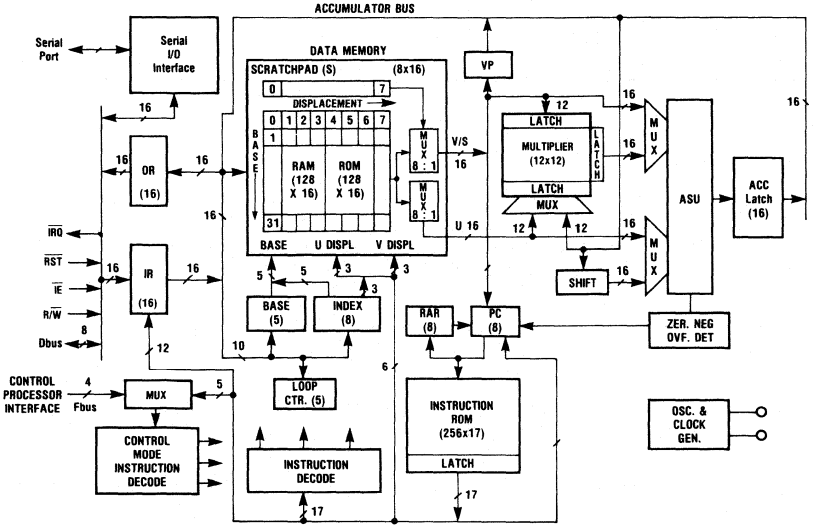
The S2811 Signal Processing Peripheral (SPP) is a high speed special purpose arithmetic processor with on-chip ROM, RAM, multiplier, adder/subtractor, accumulator and I/O organized in a pipeline structure to achieve an effective operation of one multiply, add and store of up to 12-bit numbers in 300 nanoseconds.

User Support

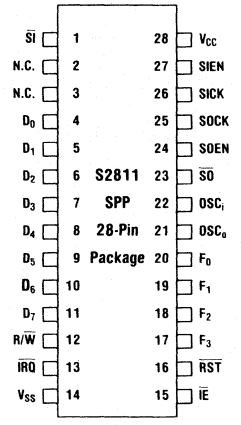
A real time in circuit emulator, the RTDS2811 is under development. This is a fully compatible hardware emulator with software assembler/disassembler and editor for rapid program development and debugging. An S2811 assembler ASMB2811, and a software simulator program package SSPP2811 are also scheduled for 1981.

*Out of the 256 instruction locations of the ROM, 250 are usable by the user program. Six instruction locations are reserved for in-house testing.

Block Diagram



Pin Configuration



Absolute Maximum Ratings

Supply Voltage	7.0VDC
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +125°C
Voltage at any Pin	V_{SS} −0.3 to V_{CC} +0.3V
Lead Temperature (soldering, 10 sec.)	200°C

Electrical Specifications: (V_{CC}=5.0V ±5%, V_{SS}=0V, T_A=0°C to +70°C, unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{IH}	Input HIGH Logic "1" Voltage	2.0		V_{CC}+0.3	V	V_{CC}=5.0V
V_{IL}	Input LOW Logic "0" Voltage	−0.3		0.8	V	V_{CC}=5.0V
I_{IN}	Input Logic Leakage Current		1.0	2.5	μAdc	V_{IN}=0V to 5.25V
C_I	Input Capicitance			7.5	pF	
V_{OH}	Output HIGH Voltage	2.4			V	I_{LOAD}=−100μA, V_{CC}=min, C_L=30pF
V_{OL}	Output LOW Voltage			0.4	V	I_{LOAD}=1.6mA, V_{CC}=min, C_L=30pF
f_{CLK}	Clock Frequency	5.0	20		MHz	V_{CC}=5.0V
P_D	Power Dissipation		1.2	1.8	W	V_{CC}=5.0V
f_{CLK}(max)	Maximum Clock Frequency S2811-6 S2811-5 S2811-4 S2811	 10 12 15 20			MHz	V_{CC}=5.0V

SPP Pin Function/Descriptions

Microprocessor Interface (16 pins)

D_0 through D_7 (Input/Output) Bi-directional 8-bit data bus.

F_0 through F_3 (Input) Control Mode/Operation Decode. Four microprocessor address leads are used for this purpose. See "SPP CONTROL MODES AND OPERATIONS." (Table 1)

$\overline{IE}$ (Input) Interface Enable. A low level on this pin enables the SPP microprocessor interface. Generated by microprocessor address decode logic.

R/$\overline{W}$ (Input) Read/Write Select. When HIGH, output data from the SPP is available on the data bus. When LOW, data can be written into SPP.

$\overline{IRQ}$ (Output) Interrupt Request. This open-drain output will go LOW when the SPP needs service from the microprocessor.

$\overline{RST}$ (Input) When LOW, clears all internal registers and counters, clears all modes and initiates program execution at location 00.

Serial Interface (6 pins)

SICK, SOCK	Serial Input/Output Clocks. Used to shift data into/out of the serial port.
$\overline{SI}$	(Input) Serial Input. Serial data input port. Data is entered MSB first and is inverted.
SIEN	(Input) Serial Input Enable. A HIGH on this input enables the serial input port. The length of the serial input word (16 bits maximum) is determined by the width of this strobe.
$\overline{SO}$	(Output) Serial Output. Three-state serial output port. Data is output MSB first and is inverted.
SOEN	(Input) Serial Output Enable. A HIGH on this input enables the serial output port. The length of the serial output (16 bits maximum) is determined by the width of this strobe.

Miscellaneous

OSC_i, OSC_o	An external 20MHz crystal with suitable capacitors to ground can be connected across these pins to form the time base for the SPP. An external clock can also be applied to OSC_i input if the crystal is not used.
V_{CC}, V_{SS}	Power supply pins $V_{CC}=+5V$, $V_{CC}=0$ volt (ground).

Functional Description

The main functional elements of the SPP (see Block Diagram) are:

1. a 256x17 ROM which contains the user program,
2. a 3-port 256x16 data memory (one input and two output ports) which allows simultaneous readout of two words,
3. a 12-bit high-speed parallel multiplier,
4. an Add/Subtract unit (ASU),
5. an accumulator register, and,
6. I/O and control circuits.

The SPP is implemented in a combination of clocked and static logic which allows complete overlap of the multiply operation with the read, accumulate, and write operations. The basic instruction cycle is "Read, Modify, Write" where the "Read" brings the operands from the RAM to the multiplier and/or the product of the previous operands, and the "Write" stores the result of the "Modify." The cycle time for the instruction is 300 nanoseconds. This results in an arithmetic throughput of about 3.3 multiply and accumulate operations per microsecond. Figure 1 illustrates the SPP Instruction Formats. The OP1 and OP2 instructions are listed in Tables 2 and 3 and Figure 2 illustrates the basic instruction timing.

The SPP is intended to be used as a microprocessor peripheral. The SPP control interface is directly compatible with the 6800 microprocessor bus, but can be adapted to other 8-bit microprocessors with the addition of a few MSI packages.

The high-speed number crunching capability of the SPP gives a standard microprocessor system the necessary computational speed to implement complex digital algorithms in real time.

Operating in a microprocessor system, the SPP can be viewed as a "hardware subroutine" module. The microprocessor can call up a "subroutine" by giving a command to the SPP. A powerful instruction set (including conditional branching and one level of subroutine) permits the SPP to function independently of the microprocessor once the initial command is given. The SPP will interrupt the microprocessor upon completion of its task. The microprocessor is free to perform other operations in the interim.

The SPP contains a high-speed serial port for direct interface to an analog-to-digital (A/D) converter. In many applications, real-time processing of sampled analog data can be performed within the SPP without tying up the main microprocessor. Data transfer to the microprocessor occurs upon completion of the SPP processing. The SPP interface environment is summarized in Figure 3.

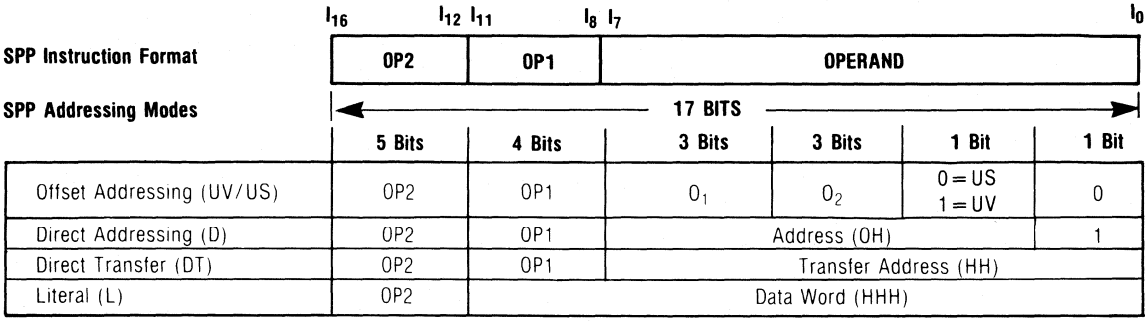
Separate input and output registers exchange data with the SPP data ports. Serial interface logic converts the parallel 2's complement data to serial 2's complement or sign + magnitude format. Data format and source (serial or parallel port) is software selectable.

Table 1 summarizes direct commands given to the SPP from the control processor. These control modes are specified via four address lines brought to the SPP.

The SPP is a memory-mapped peripheral, occupying 16 locations of the microprocessor memory space. Providing the proper SPP address will activate the corresponding control mode.

The control modes and the LIBL command enable real-time modification of the SPP programs. This permits a single SPP program to be used in several different applications. For example, an SPP might be programmed as a "universal" digital filter, with cutoff frequency, filter order, and data source (serial or parallel port) selected at execution time by the control microprocessor.

Figure 1. S2811 Object Code Instruction Formats.



NOTE: O indicates an octal digit (3 bits) and H indicates a hexadecimal digit (4 bits)

Addressing Mode	Effective Address U	Effective Address V/S	Multiplier Operands
UV	(BAS) + O_1	V = (BAS) + O_2	P = U • V
US	(BAS) + O_1	S = O_2	P = U • S
D	—	OH	P = A • V

Table 1. SPP Control Modes and Operations

Input leads F_0-F_3 define several control modes and operations to facilitate the interface between the SPP and a control processor. In general, these inputs are derived from the control processor address leads. The SPP will therefore occupy 16 memory locations, being a memory mapped peripheral.

Control Modes and Operations

F-Bus (F_3-F_0) Hex Value	Mnemonic	Operation/Function
0	CLR (Clear)	Resets control modes to normal operation.
1	RST (Reset)	Software master reset. Clears all SPP registers and starts execution at location 00. Also resets control modes to normal operation.
2	DUH (Data U/H)	Specifies MSByte of data word. DUH terminates data word transfer.
3	DLH (Data L/H)	Specifies LSBs of data word.
4	XEQ (Execute)	Starts execution at location specified on data lines (HH).
5	SRI (Ser. Inp.)	Enables serial input port.
6	SRO (Ser. Out.)	Enables serial output port.
7	SMI (S/M Inp.)	Converts sign-magnitude serial input data to 2's complement form.
8	SMO (S/M Out.)	Converts 2's complement internal data to sign-magnitude serial output.
9	BLK (Block)	Enables block data transfer.
A	XRM (Ext. ROM)	Permits control of SPP using external instruction ROM. A special mode used primarily for testing.
B	SOP	Set Overflow Protect (Normal mode of operation).
C	COP	Clear Overflow Protect.
D,E,F		Not used.

Figure 2. SPP Instruction Timing Diagram

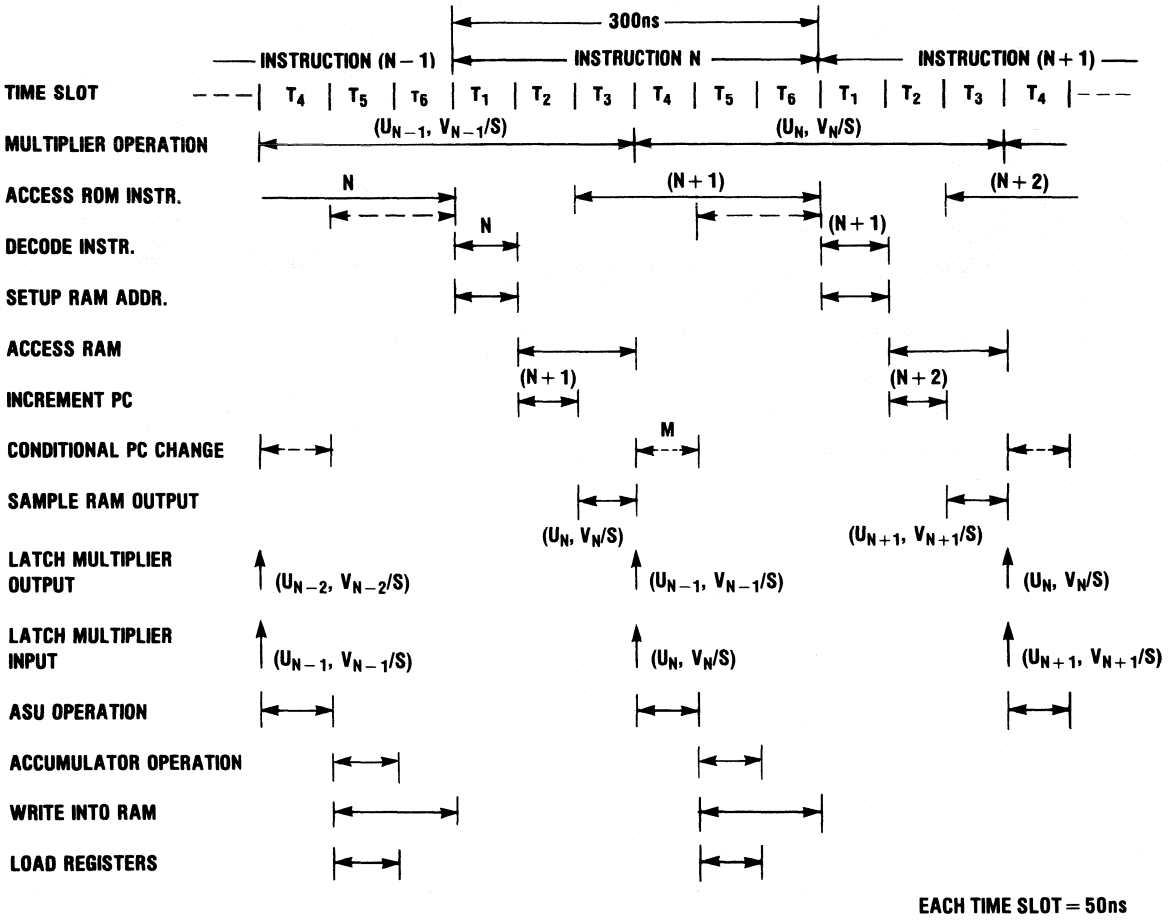


Figure 3. SPP Interface Environment

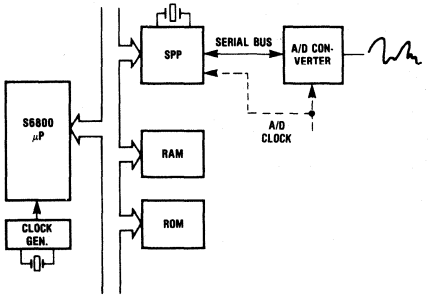


Figure 4. Loading BASE and INDEX registers and LOOP counter

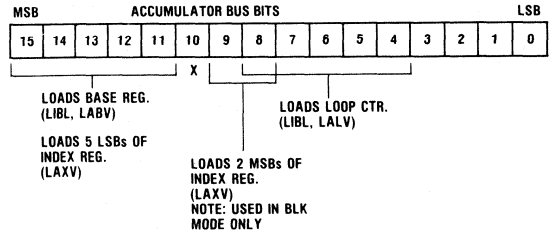


Figure 5A. SPP to 6800 Interface

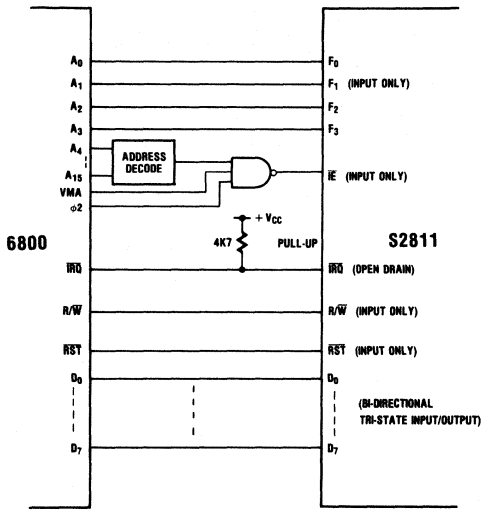
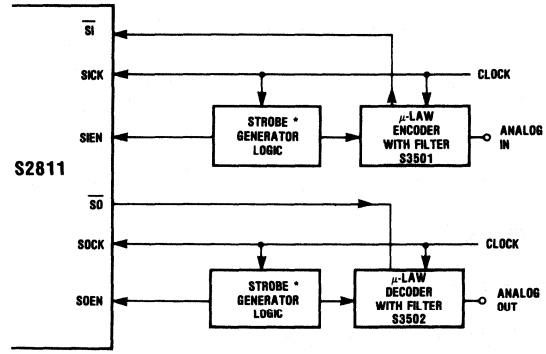


Figure 5B.



Note 1. μlaw↔linear conversion is performed by the SPP software.

*Note 2. The input and output clocks and strobe generators may be realized with two (2) CMOS packages.

Figure 5C. SPP Serial Port to PCM BUS Interface

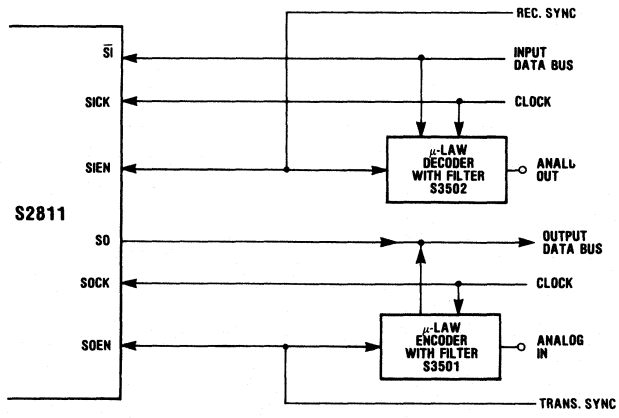
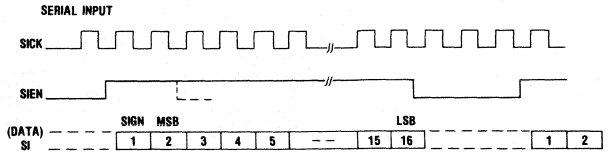
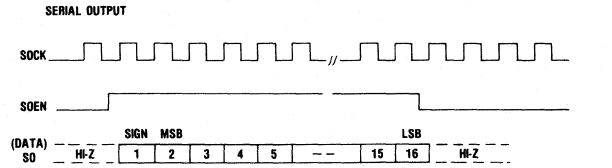


Figure 5D. SPP Serial Interface Timing



1. RISE AND FALL OF SOEN MUST FOLLOW FALLING EDGE OF SOCK.
2. OUTPUT DATA WILL BE 1 TO 16 BITS DEFINED BY WIDTH OF SOEN.
3. DATA ARE VALID FROM RISING EDGE TO RISING EDGE OF SOCK SO THAT THE RECEIVING SYSTEM CAN SAMPLE DATA ON TRAILING EDGE.
4. IF THE SERIAL OUTPUT BUFFER IS EMPTY, ALL ONES WILL BE OUTPUT.
5. SO WILL BE IN A HIGH IMPEDANCE STATE WHEN NOT ENABLED BY SERIAL OUTPUT SEQUENCE.
6. THE SERIAL DATA IS INVERTED AND MAYBE EITHER IN SIGN + MAGNITUDE OR TWO'S COMPLEMENT CODE.
7. THE MAXIMUM FREQUENCY OF SOCK IS 5MHz.



1. SIEN MUST BE SYNCHRONIZED TO THE FALLING EDGE OF SICK SUCH THAT THE RISE AND FALL OF SIEN FOLLOW FALLING EDGE OF SICK.
2. DATA MAY CONTAIN 1 to 16 BITS DEFINED BY WIDTH OF SIEN. SPP WILL LEFT JUSTIFY DATA WORDS 16 BITS.
3. DATA ARE SAMPLED ON THE TRAILING EDGE OF SICK.
4. MINIMUM 16 SICK PULSES + 4_{μ}SEC. ARE REQUIRED BETWEEN SIEN RISING EDGES.
5. IF SERIAL INPUT BUFFER IS FULL, SPP WILL IGNORE NEW INPUT SAMPLES.
6. THE SERIAL DATA IS INVERTED AND MAY BE EITHER IN SIGN + MAGNITUDE OR TWO'S COMPLEMENT CODE.
7. THE MAXIMUM FREQUENCY OF SICK IS 5MHz.

Figure 5E. SPP Parallel Interface Timing

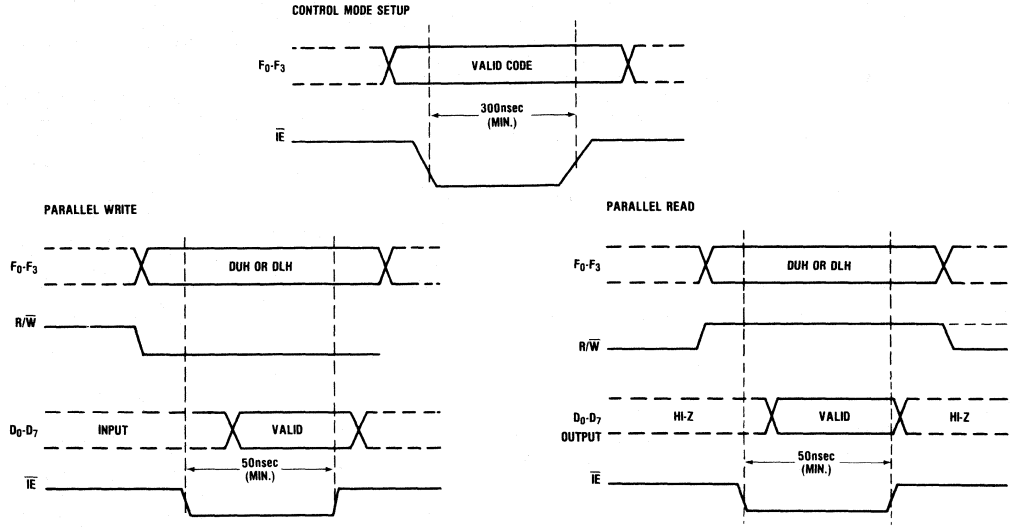


Table 2. SPP Instruction Set

OP1 Instructions

Type	Mnemonic	Hex Code I11-18	Address Modes	Operations	Description
No Operation	**NOP**	0	- - -	None	**No OP**eration
Accumulator Operations	**ASB**	C	- - -	ABS (A)→A	**ASB**olute value of accumulator is placed in accumulator.
	NEG	D	- - -	—(A)→A	**NEG**ate accumulator contents (two's complement) and replace in accumulator.
	SHR	E	- - -	(A)/2→A	**SH**ift **R**ight accumulator contents 1-bit position. Equivalent to dividing contents by two.
	SGV	F	UV/US, D	(A)→A, if sign (A) = sign V/S −(A)→A, if sign (A)≠sign V/S	**Sg**n of RAM output **V** is the sign of accumulator contents. Accumulator contents are negated (two's complement) if different sign from V. Useful in implementing hard limiter function.
Addition Operations	**AUZ**	2	UV/US	(U) + 0→A	**A**dd **U** and **Z**ero. Loads RAM output U into the accumulator.
	AVZ	1	UV/US, D	(V/S) + 0→A	**A**dd **V**/S and **Z**ero. Loads RAM output V/S into the accumulator.
	AVA	8	UV/US, D	(V/S) + (A)→A	**A**dd **V**/S and **A**ccumulator contents. Sum is placed back into accumulator.
	AUV	4	UV/US	(U) + (V/S)→A	**A**dd RAM outputs **U** and **V**/S and place sum in accumulator.
Subtraction	**SVA**	9	UV/US, D	(V/S)—(A)→A	**S**ubtract **V**/S and **A**ccumulator contents. The difference (V—A) is placed in the accumulator.
	SVU	5	UV/US	(V/S)—(U)→A	**S**ubtract RAM outputs **V** and **U** and place difference (V—U) in the accumulator.
Multiply/ Add Operations	**APZ**	3	- - - (current inst.) UV/US, D (prec. instr)	(P) + 0→A	**A**dd **P**roduct and **Z**ero. Loads multiplier product into the accumulator. The multiplier inputs were set up in the preceding instruction by addressing mode.
	APA	A	- - - (current inst.) UV/US, D (prec. instr)	(P) + (A)→A	**A**dd **P**roduct and **A**ccumulator contents. Result is placed in the accumulator. The multiplier inputs were set up in the preceding instructions by addressing mode.
	APU	6	UV (current instr) UV/US, D (prec. instr)	(P) + (U)→A	**A**dd **P**roduct and RAM output **U**. Sum is placed in accumulator. The multiplier inputs were set up in preceding instruction by addressing mode.
Multiply/ Subtract Operations	**SPA**	B	- - - (current instr) UV/US, D (prec. instr)	(P)—(A)→A	**S**ubtract **P**roduct and **A**ccumulator contents. Difference (P—A) is placed in accumulator. The multiplier inputs were set up in preceding instruction by addressing mode.
	SPU	7	UV/US (current instr) UV/US, D (prec. instr)	(P)—(U)→A	**S**ubtract **P**roduct and RAM output **U**. Difference (P—U) is placed in accumulator. The multiplier inputs were set up in preceding instruction by addressing mode.

Table 3. SPP Instruction Set
OP2 Instructions

Type	Mnemonic	Hex Code I16-I12	Address Modes	Operations	Description
Load Instructions	**LLTI**	1E	Literal	HHH→IR	**L**oad **LiT**eral in **I**nput register. A 12-bit (3 hex digits) literal is transferred to the input register. This instruction cannot be used with an OP1 instruction or with a specified addressing mode. Literal is left justified to occupy bits 4-15 in register.
	LIBL	07	- - -	(IR)→BAS (IR)→LC	**L**oad **I**nput contents to **B**ase register and **L**oop counter. See Figure 4. Clears input flag (LOW).
	LACO	02	- - -	(A)→OR	**L**oad **AC**cumulator contents into the **O**utput Register. This is the basic data output instruction. Sets output flag (HIGH). The IRQ line will be set low if the SRO mode is not set.
	LAXV	05	UV/US, D	(A)→IX, V/S (A)→A	**L**oad **A**ccumulator contents into index register and RAM location **V**/S. Accumulator is truncated to 5 most significant bits after the operation. See Figure 4.
	LALV	04	UV/US, D	(A)→LC, V/S	**L**oad **A**ccumulator to **L**oop counter and RAM location **V**/S. See Figure 4.
	LABV	03	UV/US, D	(A)→BAS, V/S (A)→A	**L**oad **A**ccumulator to **B**ase and RAM location **V**/S. Truncate accumulator contents to most significant 5 bits after the operation. See Figure 4.
Data Transfer Instructions	**TACU**	0B	UV/US	(A)→U	**T**ransfer **A**ccumulator **C**ontents into RAM location **U**.
	TACV	0C	UV/US, D	(A)→V/S	**T**ransfer **A**ccumulator **C**ontents into RAM location **V**/S.
	TIRV	08	UV/US, D	(IR)→V/S	**T**ransfer **I**nput **R**egister Contents to RAM location **V**/S. This is the basic data input instruction. Clears input flag (LOW).
	TVPV	09	UV/US, D	VP→V/S	**T**ransfer contents of **VP** register (equals previous value of output V) to RAM location **V**/S.
	TAUI	10	UV/US	(A)→U	**T**ransfer **A**ccumulator contents into RAM location **U** using **I**ndex register as base.
Accumulator Operations	**CLAC**	01	- - -	0→A	**CL**ear the **AC**cumulator. Forces SWAP mode to normal operation and clears overflow flag.
Register Manipulation Instruction	**INIX**	0D	- - -	(IX) + 1→IX	**IN**crement the **I**nde**X** register.
	DECB	0E	- - -	(BAS)—1→BAS	**DEC**rement the **B**ase register.
	INCB	0F	- - -	(BAS) + 1→BAS	**INC**rement the **B**ase register.
	SWAP	06	- - -	BAS↔IX	**SWAP** the roles of Base and Index registers.
Unconditional Branch Instruction	**JMUD**	15	DT	HH→PC	**JuMp** **U**nconditionally **D**irect to location indicated by 8-bit (two hex digits) literal HH. Cannot be used with an OP1 instruction requiring specific addr. mode.
	JMUI	11	UV/US	[(IX)]→PC	**JuMp** **U**nconditionally **I**ndirect to location indicated by contents of RAM address pointed to by index and displacement indicated by V/S. $[V/S)_{0\text{-}7}]$→PC.
Conditional Branch Instructions	**JMCD**	16	DT	HH→PC, if LC≠0 (LC)—→LC	**JuMp** **Conditionally** **D**irect to location indicated by 8-bit (two hex digits) literal HH, if loop counter is not zero. Loop Counter is decremented after the test.
	JMPZ	19	DT	HH→PC if (A) = 0	**JuMP** to location specified if accumulator contents are **Z**ero as a result of previous instruction.
	JMPN	1A	DT	HH→PC if (A) :	**JuMP** to location specified if accumulator contents are **N**egative as a result of previous instruction.
	JMPO	1B	DT	HH→PC if (A) Overflows	**JuMP** to location specified if accumulator **O**verflows as a result of previous instruction. Clears **O**verflow.
	JMIF	1C	DT	HH→PC if IF = 0	**JuMp** if **I**nput **F**lag is low to location specified (Note 4). IRQ line will be set low if the SRI mode is not set.
	JMOF	1D	DT	HH→PC if OF = 1	**JuMp** if **O**utput **F**lag is high to location specified (Note 4).
Subroutine Instruction	**JMSR**	14	DT	(PC) + 1→RAR, HH→PC	**JuMp** to **SubR**outine. Execution jumps unconditionally to location indicated by 8-bit (two hex digits) literal HH. Return address is stored in RAR. Cannot be used with an OP1 instruction requiring specified address mode.
	RETN	13	- - -	(RAR)→PC	**RETurN** from subroutine. Execution continues at instruction following the JMSR instruction.

Table 3. SPP Instruction Set
OP2 Instructions (Continued)

Type	Mnemonic	Hex Code I16-I12	Address Modes	Operations	Description
Complex Instructions	**JCDT**	18	DT	HH→PC if LC≠0, (LC)—1→LC (BAS) + 1 →BAS, (IX) + 1→IX	**J**ump **C**onditionally **D**irect Dual **T**racking. Increment base and Index registers. Loop Counter is decremented after test.
	JCDI	17	DT	HH→PC if LC ≠0, (BAS) + 1→BAS (LC)—1→LC	**J**ump **C**onditionally **D**irect and **I**ncrement base register. Loop Counter is decremented after test.
	TVIB	0A	UV/US	(VP)→V/S, (BAS) + 1→BAS	**T**ransfer contents of VP register to RAM location **V**/S and **I**ncrement **B**ase register.
	MODE	1F	- - -	Control mode replaces OP1	OP1 code in this instruction can select any one of the several control **MODE**s/operations specified in Table 1.
	REPT	12	- - -	PC inhibited if LC≠0 (next instruction) (LC)—1→LC (each iteration of next instruction.)	**REP**eat next instruction until LC = 0. Increment PC to access next instruction, then suppresses increment of PC if LC≠0. Loop Counter is decremented with each iteration of the repeated instruction.

NOTES:
1. Whenever the Index register is selected by an instruction OP2 it controls the entire line of code.
2. Loop Counter cannot underflow.
3. S refers to scratchpad.
4. Input flag is low if SPP has not received a new input word.
5. (A) represents truncation of the accumulator to 5 most significant bits (sign and 4 MSB).
6. Multiplier input latches and the VP register are not updated when either the DT or L addressing modes are used in conjunction with an OP2 instruction.
7. - - - indicates don't care address mode.
8. When D address mode is used, accumulator contents as a result of previous instruction replace U input to multiplier.

SPP Addressing Modes

The SPP provides four methods of data access (see Figure 1). In the direct mode, the full address of the data is specified. Due to limitations in the instruction word size, only one data word at a time may be accessed in this manner, and only even displacement addresses.

In the relative (to base) mode the base register is set up using a LLTI/LIBL sequence, or LABV, and two data words are accessed simultaneously by specifying U and V displacements in the instruction word.

Data may be stored/retrieved from the scratchpad memory by specifying the scratchpad mode and providing scratchpad and U port displacements. The U port data is accessed relative to the base register. The scratchpad data is treated exactly the same as data accessed via the U and V RAM ports, except the 8-word scratchpad block is substituted for the V data block.

The fourth addressing mode is dual-tracking base addressing. This mode greatly increases throughput in matrix operations.

The JMIF and JMOF instructions provide the capability to synchronize the SPP when operating in synchronous sampled data systems. When executed these commands cause the SPP to set the $\overline{IRQ}$ output low, thus requesting service from the microprocessor. The SPP can be put in a wait loop until a new data sample is available at the IR or has been read from the OR, as appropriate. The TIRV and LIBL commands facilitate transfer of input data from the IR to data memory or the base register and loop counter respectively. LACO command provides for data transfer to the OR.

Block Data Transfer (BLK Mode)

The contents of the RAM portion of the data memory may be loaded or dumped via the parallel interface by use of the Block Transfer mode. This mode is ideally suited for transfer using a DMA Controller. The sequence and timing are shown in Figure 6. Eight bit words may be transferred using the DUH mode only. The memory is addressed by the index register in this mode, and the register is automatically incremented after each word transfer. The displacement is addressed by the 2 most significant bits of this register (see Figure 4) so that the addressing is done base-by-base, then next displacement, i.e., columnwise. The starting address is selected by pre-

setting the Index Register (using the LAXV instruction) before setting the SPP into the BLK mode. The last address will depend on the number of word transfers executed. Note that the address following Base 31, Displacement 3 is Base 0, Displacement 0. This allows the continuous transfer of any number of words to be executed, starting at any address. The status of the R/$\overline{W}$ line is latched into the chip when the BLK mode is set up, eliminating the need to control this line when the block transfer is being done under the direct control of the host processor.

Figure 6A. Block Read Sequence/Timing

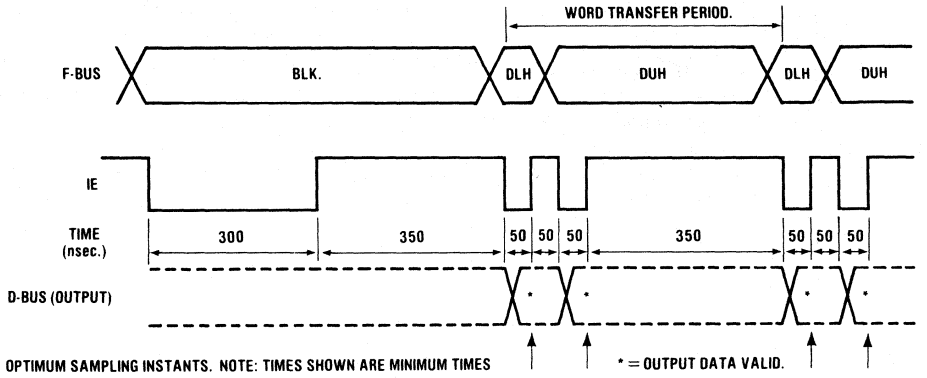
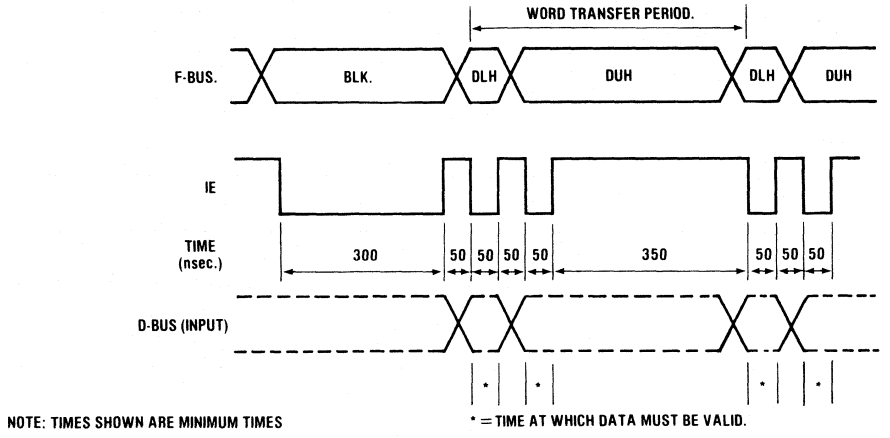


Figure 6B. Block Write Sequence/Timing



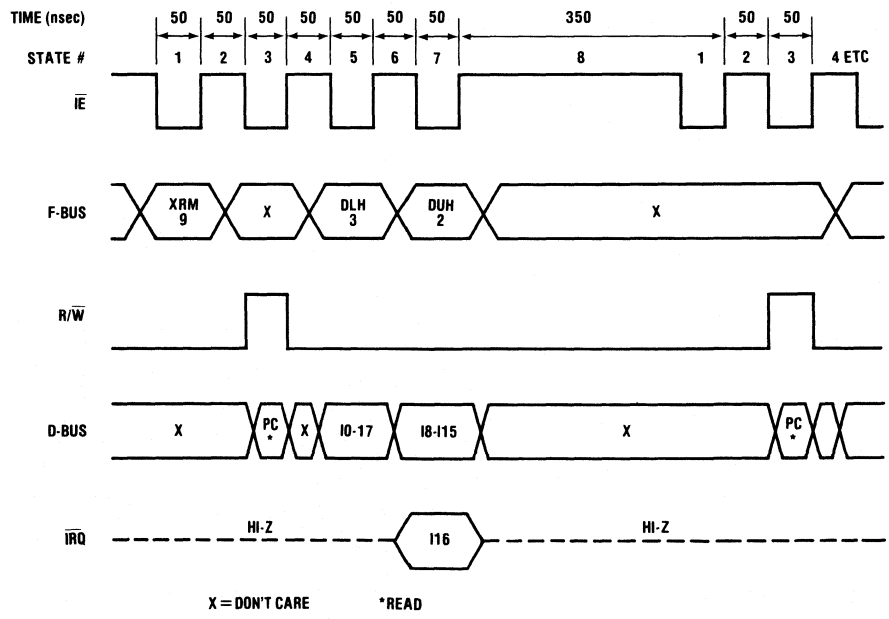
External Instruction Operation (XRM Mode)

The XRM mode is primarily intended for testing the SPP independently of the contents of the Instruction ROM. However, it can be used in program development and certain low speed applications using an external memory to store the program. Note that only the Instruction ROM is substituted in this mode, it is not possible to substitute the contents of the Data ROM (Displacements 4-7).

In this mode the SPP operates as a state machine. Selecting the XRM mode initializes the state machine to the idle state (State 1), as shown in Figure 7-A. When the $\overline{IE}$ line returns high the state machine advances to the ready state (State 2). In State 3 the program counter is output on the Data Bus (D_0-D_7), provided the R/$\overline{W}$ line is high at that time. The next rising edge of $\overline{IE}$ takes the state machine into State 4, and may be used to latch the PC into an external register. By using this to address the external instruction memory it is possible to make full use of the conditional branching instructions without any separate computation. The next cycle of the $\overline{IE}$ line takes the state machine through States 4 and 5 during which time the lower 8 bits of the next instruction to be executed (I0-I7) are read in on the Data Bus, and latched in on the rising edge of $\overline{IE}$ which takes the state machine into State 6. The next cycle takes the state machine through States 6 and 7 when the next 8 bits of the next instruction (I18-I15) are read in on the Data Bus, and the MSB (I16) is read in on the $\overline{IRQ}$ line. The $\overline{IRQ}$ line will always be floating at this time, even if it was previously set low. The next rising edge of the $\overline{IE}$ latches in these instruction bits and advances the state machine into State 8, the execute state. The next low state of the $\overline{IE}$ line advances the state machine into the idle state, State 1, once again. It is important that the SPP be allowed to complete its execution cycle (300nsec) before the next rising edge of $\overline{IE}$, otherwise the cycle may be corrupted.

No restrictions on serial I/O exist in the XRM mode, but there are constraints on the handling of parallel I/O due to the use of the $\overline{IE}$ line, the F-bus and the D-bus for instruction loading. When the SPP is waiting for input data (caused by the execution of a JMIF

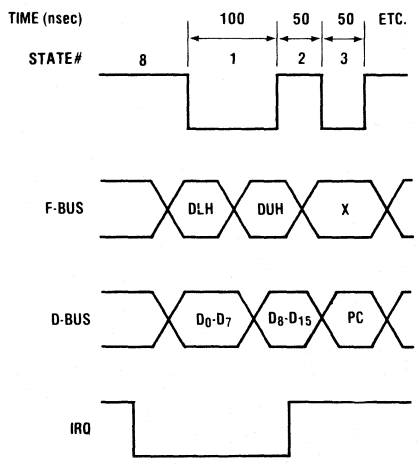
Figure 7A. XRM Timing/Sequence



NOTES: CODE XRM NEED ONLY APPEAR ON THE F-BUS IN THE FIRST CYCLE.
USE CLR OR RST TO STOP XRM OPERATION.
TIMES SHOWN ARE MINIMUM TIMES.

operator) or has output data ready (caused by the execution of a LACO operator) the $\overline{IRQ}$ line will go low during the T5 period (see Figure 2) of the execution cycle. Several methods of dealing with the data transfer exist, but the simplest is to extend the period of State 1 after the detection of the $\overline{IRQ}$ signal as shown in Figure 7-B. If the F-bus is set to code DLH (hex 3) during the first part of this period the LSbyte of the data may be read, (in the case of an output) or written (in the case of an input). If the F-bus is then set to code DUH (hex 2) without taking $\overline{IE}$ high, the data will change to the MSbyte (in the case of an output), and in the case of an input the LSbyte will be latched in at the F-bus transition, allowing the MSbyte to be written and latched in at the rising edge of $\overline{IE}$ taking the state machine into State 2.

Figure 7B. Data Transfer During XRM Operation



NOTE: TIMES SHOWN ARE MINIMUM TIMES

Circuit Description

Instruction ROM—The SPP program is stored in a 256x17 bit ROM. The 17-bit wide instruction word (See Figure 1) facilitates multiple operations per instruction. Addresses 250-255 are reserved for chip testing.

Data Memory—The 256x16 bit data memory is organized to provide two operands (U, V) in a single fetch cycle. The 256 data words are structured in a 32-'base' by 8-'displacement' word matrix. Memory is further partitioned such that each base group contains 4 words of RAM (displacements 0 through 3) and 4 words of ROM (displacements 4 through 7). Only the base information is fed to the RAM/ROM core. All eight displacement words associated with that base are accessed in parallel. Two independent displacement multiplexers select the two operands (U, V) from the eight output words. Within an 8-word base, therefore, the memory appears to have three ports.

Scratchpad Memory—An 8-word scratchpad memory (all RAM) is provided so that common data may be accessed with the full efficiency of data contained within an 8-word base. An additional multiplexer on the "V" memory port accesses the scratchpad data instead of data from the main memory core. Since this is independent of the base group, the scratchpad contents may be considered as a "floating" base group. This feature doubles the efficiency of equalizer tap update and similar programs.

VP Register—The VP register provides a one-instruction delay of data accessed from the memory "V" port. The memory read cycle precedes the write cycle (see Figure 2). The VP register consists of two portions. Data from the n-th read cycle first enters the master portion. During the next cycle, data from instruction n+1 enters the master portion while the instruction n data shifts to the slave portion. The data in the slave portion may be returned to the memory during the instruction n+1 write cycle by use of the commands TVPV or TVIB. Thus digital filter z^{-1} delays are implemented with minimal software overhead.

RAR—A return address register allows one level of subroutine nesting. This facilitates repeated use of universal subroutines such as a second order digital filter routine, SIN/COS routine, etc., thus minimizing the program size.

Loop Counter—A loop counter is provided to handle iteration loops up to 32 iterations. Special jump instructions conditional on this loop counter to be zero, provide the iteration test without adding program steps. The loop counter can be loaded from the Input Register as well as the Accumulator.

Base Register—The base register is 5 bits wide and is used to set up the base in memory in the offset addressing (UV/US) modes. Its function may be taken over by the Index Register by means of the SWAP and TAUI instructions, and also during Block Transfer.

Table 4. OP1, OP2 Code Cross-Compatibility Table

Notes: X indicates the OP1, OP2 combination cannot be used
1. index register provides "base" information
2. CLAC overrides OP2 instruction
3. OP1 bits provide function code—see Table 1
4. address is not used with MODE and is available for setting up multiplier and VP register

	OP1→ / OP2↓	Accumulator Operations					Addition Operations				Subtraction Operations		Multiply/Add Operations			Multiply/Sub. Operations		
		NOP	ABS	NEG	SHR	SGV	AUZ	AVZ	AVA	AUV	S V A	SVU	APZ	APA	APU	SPA	SPU	MULTIPLIER SETUP
No Operation Instruction	NOOP																	
Load Instructions	LLTI	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
	LIBL																	
	LACO																	
	LAXV																	
	LALV																	
	LABV																	
Data Transfer Instructions	TACU																	
	TACV																	
	TIRV																	
	TVPV																	
	TVIB																	
	TAUI						1	1	1	1	1	1			1		1	1
Accumulator Instructions	CLAC	See note 2																
Register Manipulation Instructions	INIX																	
	DECB																	
	INCB																	
	SWAP																	
Unconditional Branch Instructions	JMUD					X	X	X	X	X	X	X			X		X	X
	JMUI					1	1	1	1	1	1	1			1		1	1
Conditional Branch Instructions	JMCD					X	X	X	X	X	X	X			X		X	X
	JMPZ					X	X	X	X	X	X	X			X		X	X
	JMPN					X	X	X	X	X	X	X			X		X	X
	JMPO					X	X	X	X	X	X	X			X		X	X
	JMIF					X	X	X	X	X	X	X			X		X	X
	JMOF					X	X	X	X	X	X	X			X		X	X
Subroutine Instructions	JMSR					X	X	X	X	X	X	X			X		X	X
	RETN																	
Complex Instructions	JCDT					X	X	X	X	X	X	X			X		X	X
	JCDI					X	X	X	X	X	X	X			X		X	X
	MODE	See note 3																4
	REPT																	

Index Register—The index register is 5 bits wide and is used to access lookup tables. This register can be incremented by a software command. Lookup table instructions cause the index contents to be used as the data memory base. Table contents may be used either as data or as jump addresses for computed GO-TO operations. Special instructions allow the base and the index register to work together, providing a dual base addressing scheme. The index is also used to step through the data memory during block transfer operations. In this mode two additional MSBs are added to this register.

ASU—The heart of the SPP is a 16-bit adder/subtractor unit (ASU). The ASU operates with two's complement arithmetic, and is provided with zero, negative and overflow detect circuits. The basic adder cell includes look-ahead carry logic to improve speed. The ASU will deliver a 16-bit sum in 40 nanoseconds. An accumulator latch follows the ASU. A shifter is available to shift the accumulator contents 1 bit to the right, providing a precision divide-by-two.

Multiplier—The SPP incorporates a parallel modified Booth's algorithm multiplier. The multiplier inputs are truncated to 12 bits and the multiplier output is rounded to 16 bits. These truncations produce a product with a resolution of 15 bits. The 16 MSBs of the product are retained. This implies that all numbers in the SPP are represented as fractions less than one in magnitude. The imaginary binary point is to the left of the MSB (B14). This fractional representation and the fixed-point arithmetic requires proper scaling of equations to realize the full accuracy of the SPP. A benefit of fractional representation of numbers is that the multiplier cannot overflow. The propagation delay through the multiplier is 300 nanoseconds. A 300-nanosecond SPP instruction cycle is achieved by pipelining the multiplier. Data entered into the multiplier during instruction n will result in a product available during instruction n+1 (see Figure 2). The one instruction delay removes the multiplier propagation delay from the overall instruction cycle.

Multiplication is automatically set up by the address mode (see Figure 1). The multiplier is always active. Products are utilized by specifying one of the multiplier OP1 operators (APZ, APA, APU, SPA, SPU). The multiplier latches are updated wherever the instruction operand is a D or UV/S address. They are not updated if the operand is a Literal or DT, and the product of the previous set-up is retained until one of the multiplier OP1 operators is used to read it out.

COMMUNICATIONS

Programming Examples

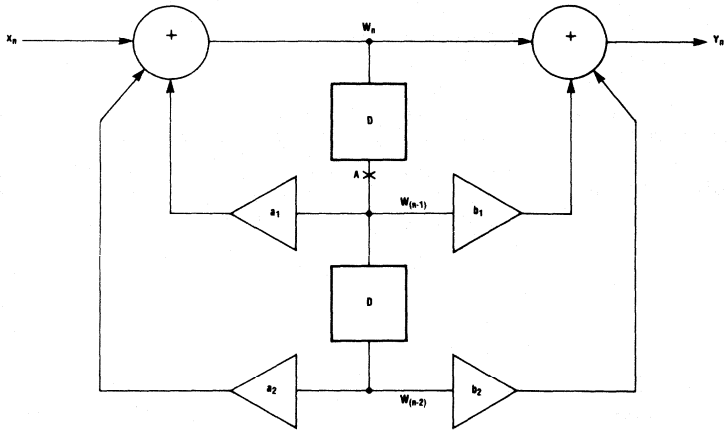
In this section two programming examples are provided to illustrate the use of some of the instructions and the power of the instruction set. The first example is that of a second order digital filter section. This can be implemented as a subroutine in the SPP such that the main program can access it repeatedly to implement higher order filter sections. The second example is that of a SINCOS subroutine that computes the values of sin ω and cos ω using an approximation formula. This routine was chosen as it illustrates the use of some of the complex instructions and because it is useful in applications that require carrier generation.

1. A second Order IIR Digital Filter Section; Figure 8 shows a block diagram, filter equations and the computational process involved in the implementation of this filter. It is clear that storage must be provided for the fixed coefficients a_1, a_2, b_1 and b_2 and previous two intermediate results W_{n-1} and W_{n-2}. Figure 10 illustrates the memory configuration at the beginning of the subrouine. Fixed coefficients are conveniently stored in the ROM portion of the data memory in displacements 4 through 7 while displacements 0 and 1 are used for storage of past values. It is assumed that the present input sample X_n is loaded in the accumulator by the main program prior to accessing the subroutine. At the end of the subroutine output Yn is left in the accummulator while W_{n-1}, and W_{n-2} are replaced by W_n and W_{n-1} so that the next input sample X_{n+1} can be processed. Note that only one base value is used by the filter for the storage and main program must load this value in the base register prior to execution.

Figure 9 illustrates the instruction sequence of the subroutine. Only five instructions are needed to completely process the section. This corresponds to a processing time of 1.5 microseconds. Figure 10 illustrates how the memory map gets modified during the execution. A higher order filter is implemented by cascading of the second order sections. The main program can increment the base register and decrement the loop counter after each iteration until the required number of iterations of this subroutine take place. Since the accumulator holds the output of the filter after each iteration, no storage is required in memory. Figure 11 illustrates the program and memory allotment for implementation of a sixth order filter.

Figure 8. Digital Filter Example

A. Second Order Recursive IIR Digital Filter Section



B. Computation Process

Input Samples $X(n) \cdots, X_{(n-2)}, X_{(n-1)}, X_n, \cdots$

Intermediate Results $W(n) \cdots, W_{(n-2)}, W_{(n-1)}, W_n, \cdots$

Output Samples $Y(n) \cdots, Y_{(n-2)}, Y_{(n-1)}, Y_n, \cdots$

Sampling Instants $\cdots\cdots, t_{(n-2)}, t_{(n-1)}, t_n, \cdots$

C. Digital Filter Equations

$$W_n = X_n + a_1 W_{(n-1)} + a_2 W_{(n-2)}$$

$$Y_n = W_n + b_1 W_{(n-1)} + b_2 W_{(n-2)}$$

Figure 9. Digital Filter Subroutine

LINE#	LABEL	OP1	OP2	OPERAND		COMMENTS
0	DF	NOP	NOOP	UV 4,0	;	a_1, $W_{n-1} \rightarrow$MULT. ACC$=X_n$
1		APA	NOOP	UV 5,1	;	a_2, $W_{n-2} \rightarrow$MULT. $X_n + a_1 \rightarrow$ACC
2		APA	TACV	UV 6,0	;	b_1, $W_{n-1} \rightarrow$MULT. $W_n = X_n + a_1$, $W_{n-1} + a_2 W_{n-2} \rightarrow$ACC ACC$\rightarrow$V 0 replace W_{n-1} $W_{n-1} \rightarrow$VP
3		APA	TVPV	UV 7,1	;	b_2, $W_{n-2} \rightarrow$MULT. $W_n + b\ W_{n-1} \rightarrow$ACC $W_{n-1} \rightarrow$V 1 replaces W_{n-2}
4		APA	RETN	—	;	$Y_n = W_n + b_1\ W_n + b_2\ W_{n-2} \rightarrow$ACC Return to main program

Figure 10. Memory Maps for the Digital Filter

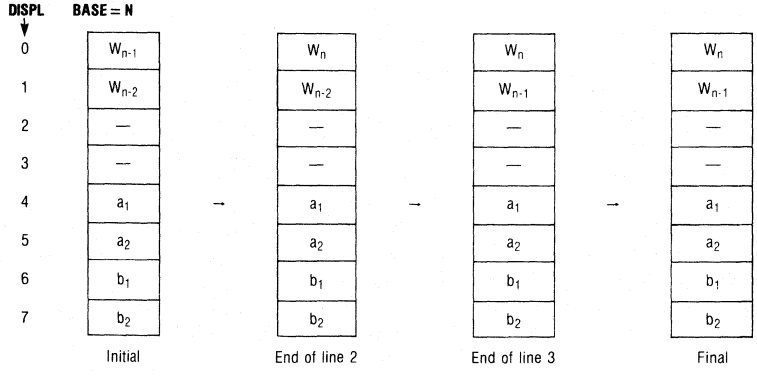


Figure 11A. Main Program Instructions for a Sixth Order Filter

```
LABEL   OP1   OP2    OPERAND   COMMENTS
                 •
                 •
                 •
        NOP   LLTI   L002   ;  (IR) = 002
        NOP   LIBL   —      ;  0→BAS, 2→LC
                            Initialize base register and loop counter
L1      —     JMSR   DF     ;  Jump to DF subroutine
        —     JCDI   L1     ;  Increment base, Test if LC = 0
                 •          If non zero go to L1
                 •          Decrement LC after test
                 •          Output of the filter is in accumulator at
                            the end of iterations.
```

Figure 11B. Memory Map for the Sixth Order Filter

Base → / DISPL ↓	0	1	2	—
0	$W_{0(n-1)}$	$W_{1(n-1)}$	$W_{2(n-1)}$	
1	$W_{0(n-2)}$	$W_{1(n-2)}$	$W_{2(n-2)}$	
2	—			
3	—			
4	a_{01}	a_{11}	a_{21}	
5	a_{02}	a_{12}	a_{22}	
6	b_{01}	b_{11}	b_{21}	
7	b_{02}	b_{12}	b_{22}	

Basic Subroutine (|coefficients|<1)

```
0 NOP   NOOP  UV4,0 ; a1, Wn-1→MULT.
                      ACC=Xn
1 APA   NOOP  UV5,1 ; a2, Wn-2→ACC
2 APA   TACV  UV6,0 ; b1, Wn-1→MULT.
                      Wn=Xn+a1 Wn-1+a2
                      Wn-2→ACC
                      ACC→V0 (replace Wn-1)
                      Wn-1→(VP)
3 APA   TVPV  UV7,1 ; b2, Wn-2→MULT.
                      Wn+b1 Wn-1→ACC
                      Wn-1→V(1) (replaces Wn-2)
4 APA   RETN        ; Yn=Wn+b1 Wn-1+b2
                      Wn-2→ACC
                      Return to main program
```

Modified Subroutine (|coefficients|<2)

```
0 NOP   NOOP  UV4,0 ;
1 APA   NOOP  UV5,1 ; as above
2 APA   TACV  UV6,0 ;
3 APA   TVPV  UV7,1 ;
4 APA   TACV  US−0  ; Yn=Wn+b1 Wn-1+b2
                      Wn-2→ACC→S0
5 AUV   TACV  UV0,0 ; U0+V0→ACC→V0=2Wn-1
6 AVZ   RETN  US−0  ; S0→ACC=Yn
```

Implementation of Second Order Digital Filter with Coefficients >1 in the S2811

In order to be able to implement a digital filter with coefficients in the range of -2 to $+2$ it is necessary to scale the coefficients by a factor of 2 to bring them into the permissible range of -1 and $+1$. However, in order to restore the "loop gain" of the recursive section of the filter it is necessary to correct for this in the signal flow network. The easiest way to do this is to double the signal level at the point A in Figure 8. The modified second order filter subroutine is shown below, together with the basic subroutine. Note that in the modified subroutine all the coefficients must be halved.

2. **SINCOS:** SINCOS is a subroutine that provides the $\sin\omega$ values for values of ω satisfying the condition $-\pi \leqslant \omega < \pi$. Since all numbers in the SPP are represented as fractions less than 1 it is first necessary to scale by a factor π such that $-1 \leqslant \frac{\omega}{\pi} < 1$. The value $\omega' = \frac{\omega}{\pi}$ is assumed to be in the accumulator at the beginning of the subroutine. In a practical application the control processor can enter ω' into the SPP before the computation begins

If the control processor does not have scaled values of ω available, an alternative method can be used. In this method the control processor can enter $\frac{\omega}{4}$ into the SPP. $\frac{\omega}{4}$ can be easily obtained by a 2-bit right shift operation. The SPP can then convert $\frac{\omega}{4}$ to $\frac{\omega}{\pi}$ by first multiplying $\frac{\omega}{4}$ by $\frac{2}{\pi}$ and then adding the result to itself. In any event it is assumed that $\omega' = \frac{\omega}{\pi}$ is available in the accumulator when the subroutine is accessed. When the control is returned to the main program $\sin\omega$ is available in S(0) and $\cos\omega$ is available in S(1) while ω' remains in the accumulator as well as S(2). The subroutine computes the $\sin\omega$ and $\cos\omega$ values by use of the following approximation:

For small values of $\Delta\omega$.

$\sin\Delta\omega \cong \Delta\omega$

$\cos\Delta\omega \cong 1$

$$\sin\omega = \sin(\hat{\omega}+\Delta\omega) = \sin\hat{\omega}\cos\Delta\omega + \cos\hat{\omega}\sin\Delta\omega \cong \sin\omega + \Delta\omega\cos\omega$$

$$\cos\omega = \cos(\hat{\omega}+\Delta\omega) = \cos\hat{\omega}\cos\Delta\omega - \sin\hat{\omega}\sin\Delta\omega \cong \cos\hat{\omega} - \Delta\omega\sin\hat{\omega}$$

ω represents the nearest quantized value to ω. In the subroutine the quantized value is obtained by truncating $2|\omega'| = (\frac{2}{\pi}|\omega|)$. The truncation results in five most significant bits including the sign bit. Since absolute value is truncated, sign bit is zero. The four most significant magnitude bits provide sixteen quantized angles $2|\hat{\omega}'| = \omega_q$. ω_q is loaded in the index register. Use of SWAP command allows the index register to access the appropriate block of data memory corresponding to ω_q. $\sin\hat{\omega}$ and $\cos\hat{\omega}$ values corresponding to ω_q are stored in displacements 4 and 5 (ROM portion) of the appropriate block addressed by ω_q. Figure 13A illustrates the organization of the lookup table.

Figure 12 shows a detailed sequence of instructions for the SINCOS routine. The routine is nineteen instructions long and takes 5.7 microseconds to execute. As seen from Figure 12, the first objective of the program is to transform the input angle to the first quadrant. This transformation process is graphically illustrated in Figure 13B. The input angle ω' is stored in S(0) and a number $[\frac{1}{2} - |\omega'|]$ is stored in S(1). The signs of these numbers are used to assign the sign to the magnitudes of $\sin\omega$ and $\cos\omega$ computed by the approximation formulae. Table 13C illustrates how the sign of $\sin\omega$ can be taken from the sign of the angle ω' and sign of $\cos\omega$ can be taken from the sign of the number $[\frac{1}{2} - |\omega'|]$. The signs are assigned by use of the SGV instruction at the end of the subroutine. The quantized angle ω_q is computed by the truncation of the number $2|\omega'|$. The truncated value (five most significant bits including sign bit) are loaded in the index register by the LAXV instruction and allows direct access of the $\sin\hat{\omega}$ and $\cos\hat{\omega}$ values from the appropriate block. $\Delta\omega$ is computed simply as a difference between the input and the quantized angle. The $\sin\omega$ and $\cos\omega$ values are stored in S(0) and S(1) respectively while the angle ω' is retained in the accumulator as well as S(2) when the program exits.

The SINCOS subroutine illustrates the following operations:

- —Scaling
- —Table Lookup
- —Use of SWAP command
- —Use of SCRATCHPAD
- —All Data Addressing Modes
- —Use of SGV command
- —Use of TVPV command
- —Truncation of the accumulator using LAXV command.

Figure 12. SINCOS Subroutine

SINCOS Routine

LINE#	LABEL	OP1	OP2	OPERAND		COMMENTS
0	SC	NOP	TACV	US−,0	;	$\omega' = \frac{\omega}{\pi} \rightarrow$ S0, ACC
1		ABS	SWAP	- -	;	$\lvert\omega'\rvert \rightarrow$ACC, SWAP roles of base and index
2		SVA	NOOP	D00.6	;	$\frac{1}{2}-\lvert\omega'\rvert \rightarrow$ACC
3		NOP	TACV	US-,1	;	$\frac{1}{2}-\lvert\omega'\rvert \rightarrow$ACC
4		AVA	NOOP	US-,1	;	$S(1) + ACC \rightarrow ACC = (1-2\lvert\omega'\rvert)$
5		ABS	NOOP	- -	;	$\lvert 1-2\lvert\omega'\rvert)\rvert \rightarrow$ACC
6		SVA	NOOP	D01.6	;	$2\lvert\omega'\rvert \rightarrow$ACC
7		NOP	LAXV	US-,2	;	$2\lvert\omega'\rvert \rightarrow S(2)$. $\hat{\omega}' \rightarrow$ACC, IX. $\hat{\omega}'$ = quantized value corresponding to ω
8		SVA	TACV	US-,2	;	$2\lvert\omega'\rvert - \hat{\omega}' = 2\Delta\omega' \rightarrow$ACC, S(2)
9		AVA	NOOP	US-,2	;	$S(2) + ACC = \rightarrow ACC(4\Delta\omega')$
10		NOP	NOOP	D02.6	;	$\frac{\pi}{4}$, $4\Delta\omega' \rightarrow$MULT.
11		APZ	TACV	US-,2	;	$\pi\Delta\omega' \rightarrow$ACC, S(2) ($\pi\Delta\omega' = \Delta\omega$)
12		NOP	NOOP	US(4,2)	;	$\sin\hat{\omega}$, $\Delta\omega \rightarrow$MULT. Index register contents $\hat{\omega}'$ point to $\sin\hat{\omega}$ in displacement 4 of the appropriate block.
13		SPU	TACV	US(5,2)	;	$\Delta\omega\sin\hat{\omega} - \cos\hat{\omega} = \cos\omega \rightarrow$ACC, S(2). $\Delta\omega$, $\cos\hat{\omega} \rightarrow$MULT.
14		APU	SWAP	US(4,2)	;	$\sin\hat{\omega} + \Delta\omega\cos\hat{\omega} = \sin\omega \rightarrow$ACC. Transfer control back to base register
15		SGV	TACV	US-,0	;	Assign the sign of ω' to ($\sin\omega$) and store result in S(0). $\sin\omega \rightarrow S(0)$, $\omega' \rightarrow$(VP)
16		AVZ	TVPV	US-,2	;	$-\cos\omega \rightarrow$ACC. (VP) = ωS(2). Refer to the description of the VP register for explanation of TVPV instruction.
17		SGV	TACV	US-,1	;	Assign the sign of $[\frac{1}{2}-\lvert\omega'\rvert]$ to $\cos\omega$ and store result in S(1). $\cos\omega \rightarrow S(1)$
18		AVZ	RETN	US-,2	;	$\omega' = \frac{\omega}{\pi} \rightarrow$ACC. Return to main program.

Figure 13A. Organization of the Lookup Table for SINCOS Routine

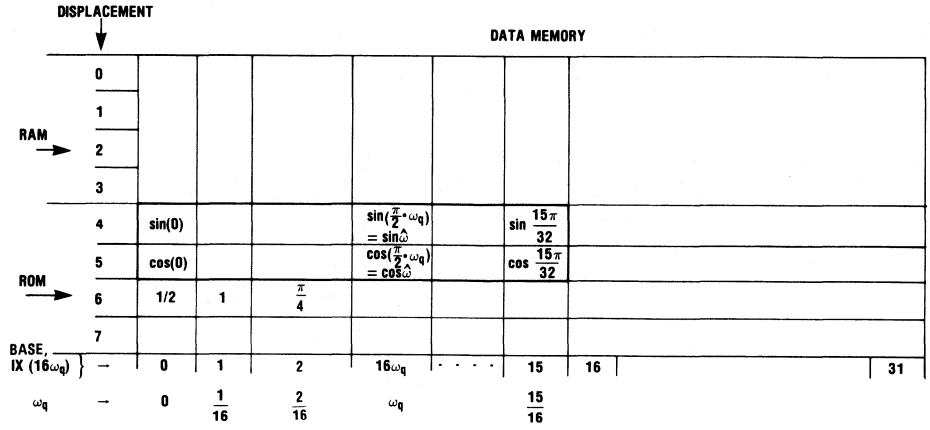


Figure 13B. Graphical Angle Transformation Process

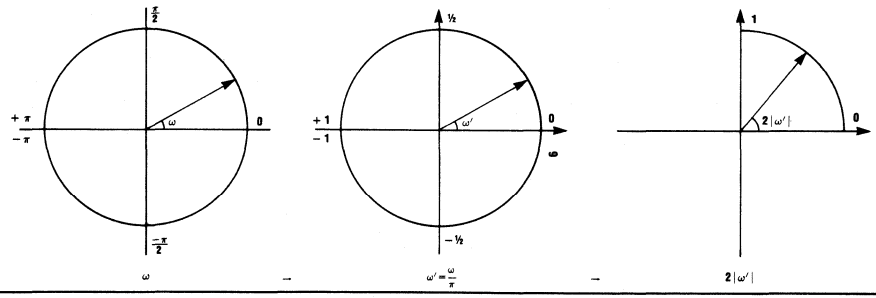


Figure 13C. Table for Computing Sign of sinω, cosω

	QUANDRANTS			
	1	2	3	4
Range of ω	0→π/2	π/2→π	−π→−π/2	-π/2→0
Range of ω′	0→½	½→1	-1→-½	-½→0
Range of [½-|ω′|]	½→0	0→-½	-½→0	0→ ½
Sign of ω′	+	+	−	−
Sign of sinω	+	+	−	−
Sign of [½-|ω′|]	+	−	−	+
Sign of cos ω	+	−	−	+

FAST FOURIER TRANSFORMER

Features

- ☐ **Performs 32 Complex Point Forward or Inverse FFT in 1.3msec, Using Decimation in Frequency (DIF)**
- ☐ **Transform Expandable either by Using Multiple S2814As (for Minimum Processing Time) or by a Single S2814A (for Minimum Hardware)**
- ☐ **Operates with any 8 or 16 Bit Microprocessor, including S6800 and S9900. Optional DMA Controller Increases Speed**
- ☐ **All Data I/O Carried Out on Microprocessor Data Bus**
- ☐ **Basic Resolution of 57dB. Optional Conditional Array Scaling (CAS) Routine Increases Dynamic Range to 70dB**
- ☐ **Optional Windowing Routine Incorporated to Permit Use of Arbitrary Weighting Function**
- ☐ **Coefficient Generation On Chip, with Rotation Algorithm for Transform Expansion up to 512 Points**
- ☐ **Based on AMI's Signal Processing Peripheral Chip (S2811) Using VMOS Technology to Achieve High Speed and Low Power Dissipation**
- ☐ **Optional Power Spectrum Computation**

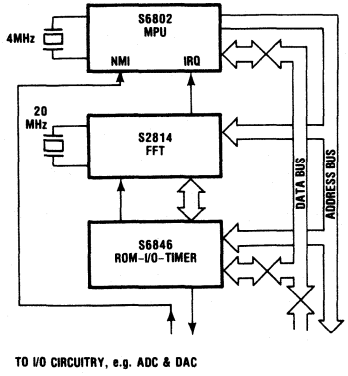
General Description

The AMI S2814A Fast Fourier Transformer is a preprogrammed version of the S2811 Signal Processing Peripheral. For further information on the internal operation of the S2811, please refer to the S2811 Advanced Product Description. It calculates FFTs and IFFTs using a decimation in frequency (DIF) technique for minimum distortion. The S2814A calculates a 32 complex point FFT using internally generated coefficients in a single pass. A coefficient rotation algorithm allows larger FFTs to be implemented (in blocks of 32 points). This implementation may be carried out by successive passes of the data through the two main routines in the S2814A, allowing larger transforms to be carried out with a single S2814A. Alternatively, an array of S2814As may be used to increase the transformation speed by parallel processing.

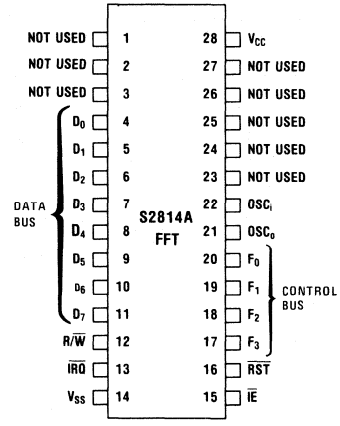
The word length used in the S2814A gives the transformed data a resolution of up to 57dB, but the total dynamic range can be increased up to 70dB by using the Conditional Array Scaling (CAS) routine incorporated.

The S2814A is intended to be used in a microprocessor system (see Block Diagram), using an 8 or 16 bit microprocessor, ROM, RAM and an optional DMA Controller or Address Generator. The S2814A is used as a

Block Diagram: Minimum System Configuration



Pin Configuration



memory mapped peripheral, and should be assigned a block of 16 addresses. It is used as a "hardware subroutine" function. The microprocessor controls the flow of data, including I/O, and calls the routines in the S2814A to cause the FFT to be executed. The S2814A responds to the microprocessor with the $\overline{IRQ}$ line when the processing of each routine is completed. In the case of a 32 point transform this signifies the completion of the transform, and in larger transforms it signifies that the microprocessor should unload the output data, load the next input data and call the next routine to be executed. The data is stored externally in RAM. Input data to be transformed is loaded into displacements 0 and 1 of the S2814A data memory. At the end of the FFT routine output data overwrites the input data. If power spectrum flag (PSF) is set, the S2814A computes the sum of the squares of the real and imaginary components of the output data and places the result in displacement 3 of the data memory. Both complex FFT data and power spectrum data are thus available. Windowing weights may be loaded into the S2814A prior to processing if the windowing routine is to be used. A 6800 compatible source listing of a suitable control program is available to the S2814A user at no charge. This control program will also be made available as a mask programmed ROM.

Absolute Maximum Ratings

Supply Voltage	7.0VDC
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +125°C
Voltage at any Pin	V_{SS} −0.3 to V_{CC} +0.3V
Lead Temperature (soldering, 10sec.)	200°C

Electrical Specifications (V_{CC} = 5.0V ± 5%; V_{SS} = 0V, T_A = 0°C to 70°C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{IH}	Input High Logic "1" Voltage	2.0		V_{CC}+0.3	V	V_{CC} = 5.0V
V_{IL}	Input LOW Logic "0" Voltage	−0.3		0.8	V	V_{CC} = 5.0V
I_{IN}	Input Logic Leakage Current		1.0	2.5	μA	V_{IN} = 0V to 5.25V
C_I	Input Capacitance			7.5	pF	
V_{OH}	Output HIGH Voltage	2.4			V	I_{LOAD} = −100μA, V_{CC} = min, C_L = 30pF
V_{OL}	Output LOW Voltage			0.4	V	I_{LOAD} = 1.6mA, V_{CC} = min, C_L = 30pF
f_{CLK} (max)	Maximum Clock Frequency				MHz	V_{CC} = 5.0V
	S2814A-6	10				
	S2814A-5	12				
	S2814A-4	15				
	S2814A	20				
P_D	Power Dissipation		1.2	1.8	W	V_{CC} = 5.0V

S2814A Pin Functions/Descriptions

Pin	Number	Function
D_0-D_7	4-11	(Input/Output) Bi-directional 8-bit data bus. Data is Two's Complement coded.
F_0-F_3	20-17	(Input) Control Function bus. Four Microprocessor address lines (typically A_0-A_3) are used to control the S2814A.
$\overline{IE}$	15	(Input) Interface Enable. A low level on this line enables data transfer on the data bus and control functions on the F-bus. Usually generated by microprocessor address decode logic.
R/$\overline{W}$	12	(Input) Read/write select. When HIGH, output data from the S2814A may be read, and when LOW data may be written into the S2814.
$\overline{IRQ}$	13	(Output) Interrupt Request. This open drain output goes low when the S2814A has completed the execution of a routine and output data is available.
$\overline{RST}$	16	(Input) When LOW all registers and counters will be cleared, including the program counter, and all control functions cleared.
OSC_i, OSC_0	22,21	Oscillator input and output. For normal operation a 20MHz crystal is connected between these pins to generate the internal clock signals. Alternatively, an external 20MHz (or lower frequency) square wave signal may be connected to OSC_o pin with OSC_i pin left open.
V_{CC}	28	Positive power supply connection.
V_{SS}	14	Negative power supply connection. Normally connected to ground.

In addition to the above, pins 23-27 and 1 are connected internally. They should all be tied to V_{SS} during normal operation.

Functional Description

The S2814A is a pre-programmed version of AMI's S2811 Signal Processing Peripheral. This is a high speed microcomputer organized for efficient signal processing and contains a data memory, instruction memory, an arithmetic unit incorporating a 12-bit parallel multiplier, as well as control registers and counters. For more detailed information about the chip, please refer to the S2811 Advanced Product Description.

The S2814A Instruction ROM contains the various routines which make up the FFT package. The routines together with their starting addresses in the Instruction ROM, are shown in Table 1A.

The Data ROM contains the coefficients required to execute the functions. 128 words of Data RAM are provided to hold the 32 point complex signal data during processing as well as the power spectrum of the output and various other parameters, including the total number of points in the desired transform. The memory is organized as a 32x4 matrix, with the data arranged in columns, as shown in Table 1B.

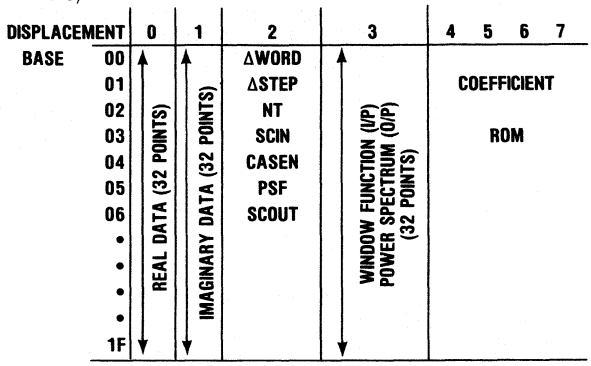
Table 1: Software Model of S2814A

A. Routine Locations in Instruction Memory

LOC (HEX)	FUNCTION
00	IDLE STATE
01	ENTRY PT. "INIT" ROUTINE
04	ENTRY PT. "FFT32" ROUTINE
D3	ENTRY PT. "COMPAS" ROUTINE
EA	ENTRY PT. "SCALE" ROUTINE
DC	ENTRY PT. "WINDOW" ROUTINE
E4	ENTRY PT. "CONJUG" ROUTINE

B. Data Memory Map

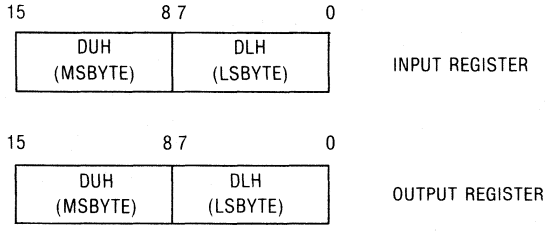
(Note: Address [Base AB, Displacement C] is written as AB·C)



C. Control Functions

F-BUS (HEX)	MNEMONIC	FUNCTION
1	RST	RESETS CHIP
2	DUH	SELECTS MSBYTE
3	DLH	SELECTS LSBYTE
4	XEQ	STARTS EXECUTION
9	BLK	SELECTS BLOCK MODE

D. Input and Output Registers



CODE IS TWO'S COMPLEMENT.

Initial Set-Up Procedure

After power up, the $\overline{RST}$ line should be held low for a minimum of 300nsec. If this line is connected to the reset line of the microprocessor this condition will be met easily. This will clear the Base and Index Registers, which are used for memory addressing, the Loop Counter and the Program Counter. Address zero in the Instruction ROM contains a Jump to Zero instruction, and thus the S2814A will remain in an idle state after being reset. Every routine in the memory is also terminated with a Jump to Zero instruction, and thus the S2814A will also remain in this same idle state after the execution of each routine. The $\overline{IRQ}$ line will signal this condition each time (except after the initial reset).

The Control Functions

The S2814A is controlled by the host microprocessor by means of the F-bus, Interface Enable ($\overline{IE}$) and the Read-Write (R/$\overline{W}$) lines. It should be connected to the host processor as a memory mapped peripheral as shown in Figure 1.

The 12 most significant address lines decode a group of 16 addresses to activate the $\overline{IE}$ line each time an address in the group is called, and the S2814A is controlled by reading to or writing from those addresses. Only 5 of these addresses are used as described in Table 2. Throughout this Product Description these addresses will be referred to as NNNX (X=0-F).

Figure 1. Connection of S2814A as a Memory Mapped Peripheral

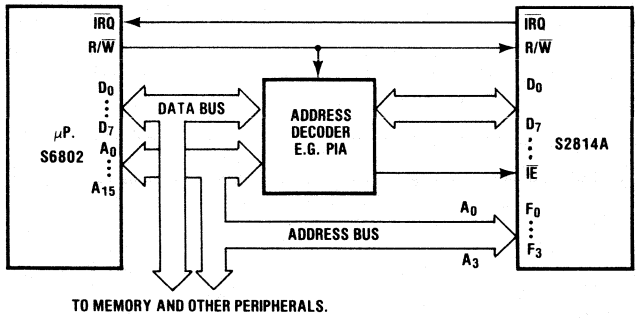


Table 2: S2814A Control Functions

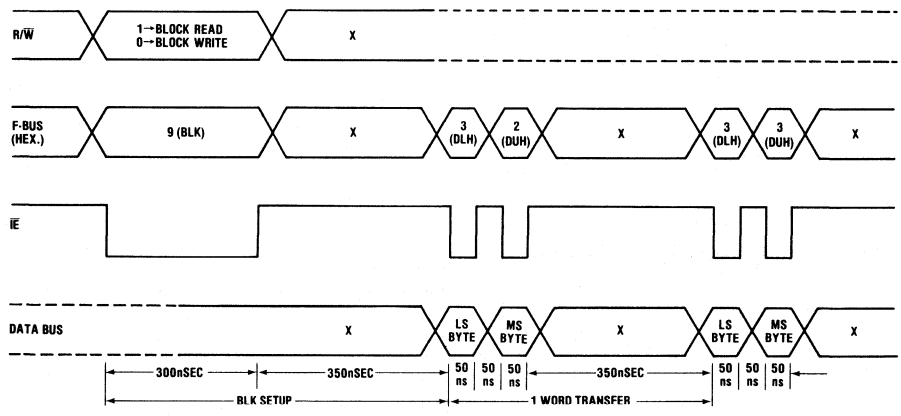
MNEMONIC	F-BUS HEX	DATA	TYPE OF OPERATION	FUNCTION
RST	1	XX	READ/ WRITE	CLEARS ALL REGISTERS. STARTS PROGRAM EXECUTION AT LOCATION 00. THIS IS THE IDLE STATE. THIS INSTRUCTION SHOULD PRECEDE BLOCK READ, BLOCK WRITE AND EXECUTE COMMANDS.
DUH	2	HH	READ/ WRITE	READS FROM OR WRITES INTO S2814A THE UPPER HALF OF THE DATA WORD. (SEE TABLE 1.D.)
DLH	3	HH	READ/ WRITE	READS FROM OR WRITES INTO S2814A THE LOWER HALF OF THE DATA WORD. (SEE TABLE 1.D)
XEQ	4	HH	WRITE	STARTS EXECUTION AT LOCATION HH
BLK	9	XX	READ/ WRITE	INITIATES A BLOCK READ OR BLOCK WRITE OPERATION. THE ENTIRE DATA RAM CAN BE ACCESSED SEQUENTIALLY BEGINNING WITH VALUES OF BASE AND DISPLACEMENT INITIALIZED USING "BLOCK TRANSFER SET UP" ROUTINE. IF A RESET OPERATION IS PERFORMED PRIOR TO BLOCK COMMAND THE DATA MEMORY ADDRESS IS INITIALIZED TO BASE 0, DISPLACEMENT 0. BLOCK READ OR WRITE OPERATION CAN BE TERMINATED ANY TIME BY PERFORMING A RESET OPERATION. THE INDEX REGISTER IS USED TO ADDRESS THE MEMORY DURING BLOCK TRANSFER AND INTERNAL ADDRESSING IS SEQUENCED AUTOMATICALLY.

NOTE: XX = Don't care
HH = 2 Hex characters (8-bit data)

The Block Transfer Operation

Block transfer is the mode used to load and unload the main data blocks into the S2814A at up to 4Mbytes/sec. In this mode the data memory is addressed by the Index Register, and after initialization the internal addressing is sequential and automatic. The sequence generated is that after each word transfer (16-bit words as 2 bytes, or 8-bit words as MSbyte (DUH) only) the base is incremented. After base 1F (31) has been reached, the base resets to 00 and the displacement increments. After base 1F displacement 3 has been reached (i.e., the highest address in the RAM, 1F.3), both base and displacement reset to zero. Note that when the BLK command is given the Read/Write line is latched internally, and remains latched until the RST command is given. The block transfer sequence and timing are shown in Figure 2.

Figure 2. Block Transfer Sequence and Timing



NOTE 1: X=DON'T CARE, OR NOT VALID.
NOTE 2: TIMES SHOWN ARE MINIMUM.

In 6800 Assembly Language a Block Write would be executed with the following code:

```
LDX     OFFST   ;LOAD MEMORY START ADDRESS INTO INDEX REG.
STA  A  BLK     ;WRITE DUMMY DATA TO ADDRESS $NNN9,BLOCK MODE.
LDA  A  0,X     ;READ FIRST BYTE FROM MEMORY.
STA  A  DLH     ;WRITE INTO S2814A AS LSBYTE. ADDRESS $NNN3
LDA  A  1,X     ;READ SECOND BYTE FROM MEMORY.
STA  A  DUH     ;WRITE INTO S2814A AS MSBYTE.ADDRESS $NNN2
LDA  A  2,X     ;SECOND WORD.
  .       .       .
  .       .       .
  .       .       .
LDA  A  62,X    ;32ND. WORD,LSBYTE.
STA  A  DLH     ;
LDA  A  63,X    ;32ND. WORD,MSBYTE.
STA  A  DUH     ;END OF TRANSFER.
STA  A  RST     ;WRITE DUMMY DATA TO ADDRESS $NNN1.RESET.
```

Block Read would be executed by substituting LDA A for STA A, and vice versa.

where:

```
RST   EQU $NNN1
DLH   EQU $NNN3
DUH   EQU $NNN2
BLK   EQU $NNN9
```

The above code assumes that the block transfer is controlled by the host processor, not using DMA. Note that DLH must always precede DUH. 8-bit data may be transferred using DUH only, assuming that the significance of the data is correct.

The FFT Routines

Six individual routines are stored in the S2814A Instruction memory. Two or more of these are used in the computation of an FFT, depending on the transform size and the options selected. The starting addresses of the routines are shown in Table 3.

Table 3. FFT Routines and Their Starting Addresses

LOCATION (HEX)	FUNCTION
00	IDLE STATE
01	ENTRY POINT FOR "INIT" ROUTINE
	(IR) = BASE, DISPLACEMENT
	$(BASE)_{4-0} \leftarrow (IR)_{15-11}, (DISP)_{1,0} \leftarrow (IR)_{9,8}$
	Sets IRQ, Returns to Idle state Exec. Time = 0.9μs
04	ENTRY POINT FOR "FFT32" ROUTINE
	(DISP0) = Input Data (Real), (DISP1) = Input Data (Imag.) (DISP2) = SCIN, CASEN, PSF
	Perform 32 point FFT. Sets IRQ, Returns to Idle state. Exec. Time = 1.2 ms to 1.8ms.
	(OR) = SCOUT (DISP0) = Transformed Data (Real), (DISP1) = Transformed Data (Imag.) (DISP2) = SCOUT, (DISP3) = Power Spectrum Data if PSF = 1
D3	ENTRY POINT FOR "COMPAS" ROUTINE
	(DISP0) = Input Data (Real), (DISP1) = Input Data (Imag.) (DISP2) = WORD, STEP, NT, SCIN, CASEN
	Perform COMPAS, Sets IRQ, Returns to Idle State Exec. Time = 233 to 374μsec.
	(DISP0) = Output Data (Real), (DISP1) = Output Data (Imag.) (DISP2) = SCOUT, (OR) = SCOUT
EA	ENTRY POINT FOR "SCALE" ROUTINE
	(IR) = SCIN, (DISP0) = Data, (DISP1) = Data
	Performs scaling, Sets IRQ. Returns to Idle State Exec. Time = 51 to 250μsec.
	(DISP0) = Scaled Data, (DISP1) = Scaled Data
DC	ENTRY POINT FOR "WINDOW" ROUTINE
	(DISP0) = Input Data, (DISP1) = Input Data (DISP3) = Multiplying factors
	Performs multiplication, Sets IRQ, Returns to Idle State Exec. Time = 49μsec.
	(DISP0) = Output Data (DISP1) = Output Data
E4	ENTRY POINT FOR "CONJUG" ROUTINE
	No set-up required. Conjugates input data (negates imaginary components). Sets IRQ. Returns to Idle State. Exec. time = 30μsec.

1. Block Transfer Set-Up (INIT). Entry Address 01.

This routine presets the Index Register to allow block transfer to commence at any location other than 00.0 in the S2814A data RAM. An eight-bit word is loaded into the upper half of the input register and the routine executed as shown:

Figure 3A. Flowchart for Subroutine FT32IN

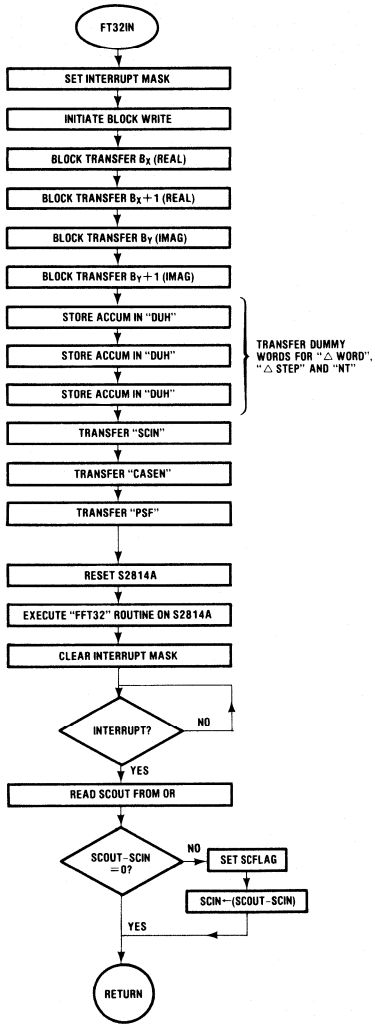
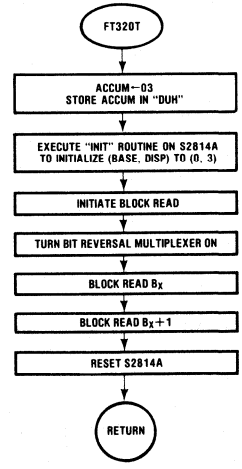


Figure 3B. Flowchart for Subroutine FT320T




```
DUH   EQU $NNN2
XEQ   EQU $NNN4


LDA   A #$XX
STA   A DUH
LDA   A #1
STA   A XEQ
```

where XX represents the start address for block transfer. (0.9μsec.) and the S2814A will return to the idle state. The routine will be executed in 3 instruction cycles Block transfer may then commence immediately.

2. FFT32. Entry Address = 04.

This is the basic 32 complex point FFT routine. For a 32 point FFT this routine is called once only and the output of the routine is the FFT. Larger FFTs are computed by decomposing them into 32 point arrays before final processing of these arrays using FFT32 to obtain the final outputs. The following data is loaded into the S2814A, using block write starting at address 00.0, i.e., INIT is not used.

32 words of real input data (addresses 00.0 - 1F.0)

32 words of imaginary input data (addresses 00.1 -1F.1)

3 dummy words (to skip addresses) (addresses 00.2 -02.2)

SCIN (input scaling parameter) (address 03.2)

CASEN (CAS Enable) (address 04.2)

PSF (Power spectrum flag) (address 05.2)

Note that CASEN (Conditional array scaling enable) and PSF are not modified during processing, and need only be loaded once. CASEN should be positive to inhibit CAS (e.g. 0000) and negative to enable CAS (e.g. 8000). Note that SCIN is not needed if CAS is not enabled. PSF should be zero if the power spectrum output is not needed, any non-zero value (e.g. 0100) will cause the power spectrum to be computed. The block transfer should be terminated with the RST command, and the FFT32 routine called. Flow charts for loading and dumping the data are shown in Figure 3. The following sequence will cause the execution of the entire function:

```
CLR   B          ;CLEAR B ACC.
STA   A  RST     ;RESET S2814A REGISTERS.
SEI              ;SET INT. MASK.
STA   A  BLK     ;SET UP BLOCK WRITE.
JSR      BLKWT   ;WRITE 64 WORDS OF DATA.
STA   A  DUH     ;WRITE DUMMY DATA TO 00.0
STA   A  DUH     ;.....TO 00.1
STA   A  DUH     ;.....TO 00.2
LDA   A  SCIN    ;FETCH SCIN.
STA   A  DLH     ;WRITE TO ADDRESS 00.3
STA   B  DUH     ;COMPLETE WORD XFER.
LDA   A  CASEN   ;FETCH CAS ENABLE.
STA   A  DUH     ;WRITE TO ADDRESS 00.4
LDA   A  PSF     ;FETCH PS FLAG.
STA   A  DUH     ;WRITE TO ADDRESS 00.5
STA   A  RST     ;RESET S2814A.
LDA   A  #4      ;FFT32 START ADDRESS.
STA   A  XEQ     ;START EXECUTING.
CLI              ;CLEAR INT. MASK.
WAI              ;WAIT FOR ROUTINE END.
LDA   A  DLH     ;START OF INT. ROUTINE.
LDA   B  DUH     ;(DUMMY).READ SCOUT.
LDA   B  SCIN    ;FETCH SCIN.
SBA              ;COMP.SCOUT WITH SCIN.
BEQ      READ    ;JUMP IF NO CHANGE.
STA   A  SCIN    ;SCOUT →SCIN
LDA   A  PASSN   ;FETCH PASS #
CMP   A  #1      ;IS THIS 1ST.PASS?
BEQ      READ    ;JUMP IF SO.
JSR      SKOUT   ;SCALE PREVIOUS ARRAYS
LDA   A  #3      ;(ASSUME PSF SET.)
STA   A  DUH     ;PRESET TO ADDRESS 00.3
LDA   A  #1      ;
STA   A  XEQ     ;EXECUTE INIT.
STA   A  BRV     ;TURN ON BIT REV.MUX.
LDA   A  BLK     ;SET UP BLOCK READ.
JSR      BLKRD   ;READ DATA.
STA   A  RST     ;END
```

The routine execution time is variable, depending on whether CASEN and PSF are set. The times are:

1. CAS - OFF. PSF - OFF 3730 instruction cycles (1.119msec.)
2. CAS - OFF. PSF - ON 3862 instruction cycles (1.159msec.)
3. CAS - ON . PSF - OFF 5867max. instruction cycles (1.760msec.)
4. CAS - ON . PSF - ON 5999max. instruction cycles (1.800msec.)

When CAS is enabled, the time depends on the number of times overflow is corrected. At the end of the routine the complex output data will have overwritten the input data in the memory (addresses 00.0 to 1F.1) and the power spectrum data will be in displacement 3 (addresses 00.3 -1F.3). The output scaling factor (SCOUT) will be loaded in the output register, generating the $\overline{IRQ}$ to signify to the host processor that the routine has completed processing.

3. Combination Pass Routine, COMPAS. Entry Address = D3.

This is the decomposition routine that breaks up larger transforms into a number of 32 point transforms to be executed by FFT32. The N data points are split into N/16 blocks of 16 points, and pairs of blocks are passed through COMPAS. The procedure is repeated one or more times if N is greater than 64, but for a 64 point FFT the resulting data is ready for processing using FFT32. The procedure is explained in greater detail in the section "Executing Larger Transforms". The following data is loaded into the S2814A before execution:

Figure 4A. Flowchart for Subroutine CSIN

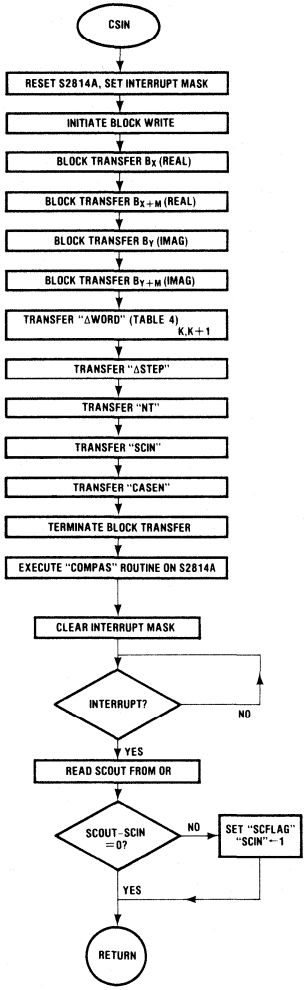
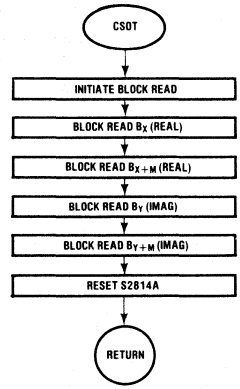


Figure 4B. Flowchart for Subroutine CSOT



32 words of real input data (addresses 00.0 - 1F.0)

32 words of imaginary input data (addresses 00.1 -1F.1)

Δ WORD (address 00.2)

Δ STEP Set up parameters (address 01.2)

NT (address 02.2)

SCIN (address 03.2)

CASEN (address 04.2)

PSF (address 05.2)

The new parameters required, Δ WORD, Δ STEP and NT are dependent on the size of the transform and with the exception of NT, change with each pass through the COMPAS routine. The values required are shown in the tables in sections "Executing 64 Point Transforms" and "Executing Larger Transforms". Flow charts for loading and dumping the data are shown in Figure 4. The routine execution time varies with transform size and depends on whether CAS is enabled or not, as shown:

TRANSFORM SIZE	64 POINT	128 POINT	256 POINT	512 POINT
Without CAS, Inst. cycles, (μsec.)	776 (233)	828 (248)	842 (253)	949 (255)
With CAS. (Max.) Inst. cycles (μsec.)	1172(352)	1224(367)	1238(371)	1245(374)

4. Data Point Scaling Routine, SCALE. Entry location = EA.

If CAS is enabled, then routines COMPAS, and FFT32 will scale all 32 data points being processed if an overflow occurs during that pass. The value of SCOUT allows the data during subsequent passes to be scaled automatically during the pass. However, data points which have already been processed must also be scaled, so that all the data is scaled by the same factor during each processing step. SCALE is a routine that allows this to be done at high speed. Each block to be scaled is block loaded into the S2814A, the routine SCALE executed, and the block dumped back into the original locations in memory.

Care must be taken to keep track of which blocks have already been processed during each step, so that blocks do not get missed or scaled twice. The execution time depends on the scaling factor (SCOUT), as shown below:

Scaling Factor (SCOUT)	1	2	3	4	5
Execution time. Inst. Cycles, (μsec.)	170(51)	336(101)	502(151)	668(200)	834(250)

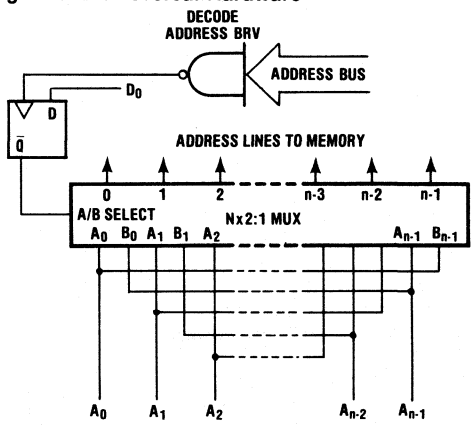
Windowing Routine, WINDOW. Entry Address = DC.

In order to allow the input data points to be windowed, a routine is provided to multiply the 32 real or complex points loaded in the S2814A by 32 window points. This is done on each block of 32 points prior to commencing the actual FFT processing. The input data required, in addition to the normal input data, are the 32 points of the window. They should be loaded into displacement 3 of the S2814A RAM and the routine WINDOW executed. The windowed data points will be returned to their original positions in the memory, so that COMPAS or FFT32 may then be executed immediately without further processing. The entire data can be loaded in a single block transfer operation by using INIT to preset the start address to 00.3. The 32 point window data is then loaded, followed by the signal data. This is possible because after loading the window the memory address will automatically reset to 00.0, the start address for the real data. The parameters are then loaded into displacement 2 addresses in the usual way. They will not be affected by the windowing operation. The total execution time is 163 instruction cycles, 49μsec.

Executing FFTs

Executing the FFTs consists of loading data blocks, executing routines in the S2814A and dumping the data. However, the sequence of the FFT output data is scrambled, and in order to use the results meaningfully, it must be unscrambled. This is done by reversing the order of the bits of the address lines for the final output data. Thus, for a 2^N point FFT the N address lines A_0, A_1, A_2 ..... A_{N-1} must be reversed to the sequence A_{N-1}, A_{N-2} ..... A_1, A_0 to address the output buffer memory. This is most conveniently done as the data points are being dumped out of the S2814A after the processing of the FFT32 routine(s). The bit reversal can be done either by software or hardware. The hardware realization is shown in Figure 5, and an example of software bit reversal is given in the section "Executing 32 Point FFTs."

Figure 5. Bit Reversal Hardware



Executing 32 Point Transforms

The basic 32 point transform is easily implemented with the S2814A since it simply requires the loading of the 32 real or complex data points and the 3 parameters SCIN, CASEN and PSF, executing FFT32 once only and dumping the data using bit reversal. The flowchart for this sequence is shown in Figure 6. It is assumed that the loading of data from the source into the input buffer and dumping of data from the output buffer to destination is carried out by the NMI (non-maskable interrupt) routine. The parameter SCIN should be set to zero, and the output data should be scaled (multiplied) by 2 (SCOUT) if absolute levels are wanted.

Figure 6. Flowchart for 32 Point FFT

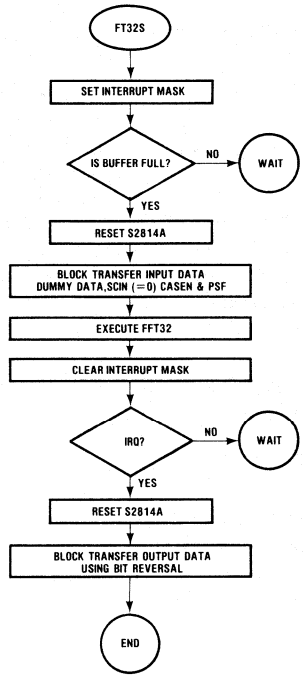
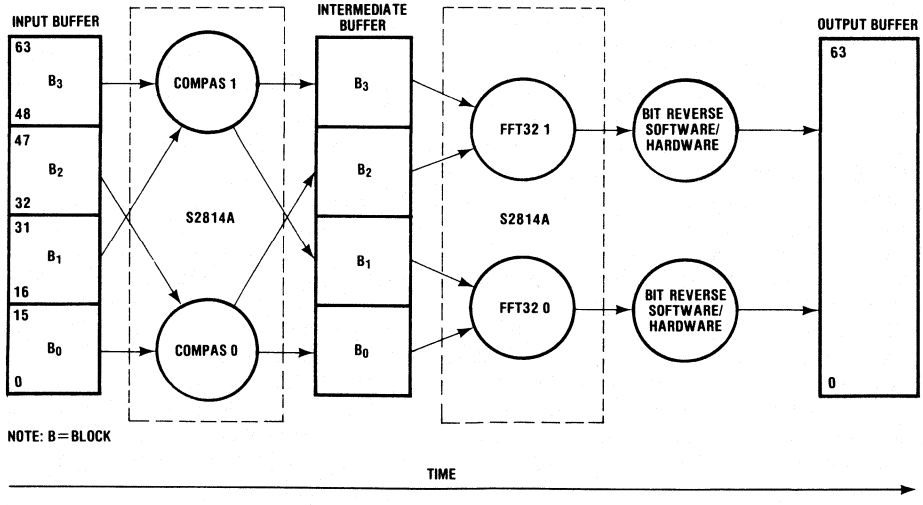


Figure 7. 64 Point FFT Flowgraph



Executing 64 Point Transforms

This is the simplest expansion of the FFT. The first step is to use COMPAS (twice) to decimate the data into two 32 point transforms, and then use FFT32 (twice) to produce the transforms. This is shown in the signal flow graph in Figure 7. The flow graph is independent of whether one or two S2814As are used, since the two passes through each of the 2 routines (COMPAS and FFT32) can be carried out sequentially or in parallel. The set up parameters for the 64 point FFT are:

For COMPAS 0: ΔWORD=8070
For COMPAS 1: ΔWORD=C070 ΔSTEP=4000 NT=1

The treatment of SCIN and SCOUT is dealt with in the next section.

Executing Larger Transforms

The execution of larger transforms follows the same sequence as the 64 point transforms; namely the decimation of the data into a series of 32 point blocks that can be processed using FFT32. For a 2^N point FFT this involves N-5 steps of processing using COMPAS, and each step requires $2^{(N-5)}$ passes through the COMPAS routine. This is followed by $2^{(N-5)}$ passes through the FFT32 routine. Within each step, each pass may be carried out sequentially using a single S2814A, or in parallel using $2^{(N-5)}$ chips. There are also intermediate sequential + parallel combinations possible, of course, using fewer chips. A signal flow graph for 1 step is shown in Figure 8.

At the start of each step, SCIN should be set to zero. For the remaining passes in that step the value of SCOUT for the current pass should be used for SCIN for the next pass. The outputs of previously computed passes must be scaled using routine SCALE each time SCOUT increases during a pass. The maximum value of SCOUT after executing COMPAS is 1, and after executing FFT32 it is 5.

A flow chart for an N point transform control program is shown in Figure 9. The routine is called NFFT and uses the following subroutines.:

CSIN — procedure for loading S2814A with COMPAS input data (Figure 4A)
CSOT — procedure for dumping COMPAS output data (Figure 4B)
SCLPRV — procedure for scaling previously computed blocks of data in each step. See Figure 10.
FT32IN — procedure for loading S2814A with FFT32 input data (Figure 3a)
FT32OT — procedure for dumping FFT32 output data. (Figure 3b)

The values of ΔWORD, ΔSTEP and NT are shown in Tables 4 and 5.

Figure 8. N Point FFT Flowgraph

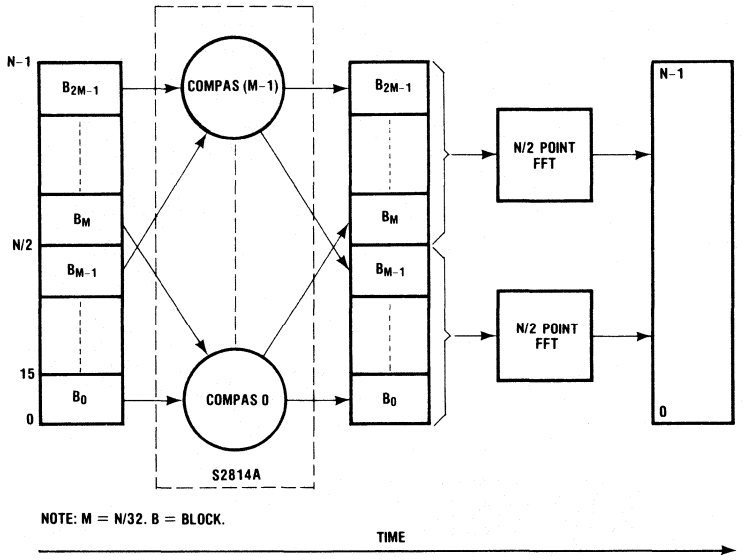
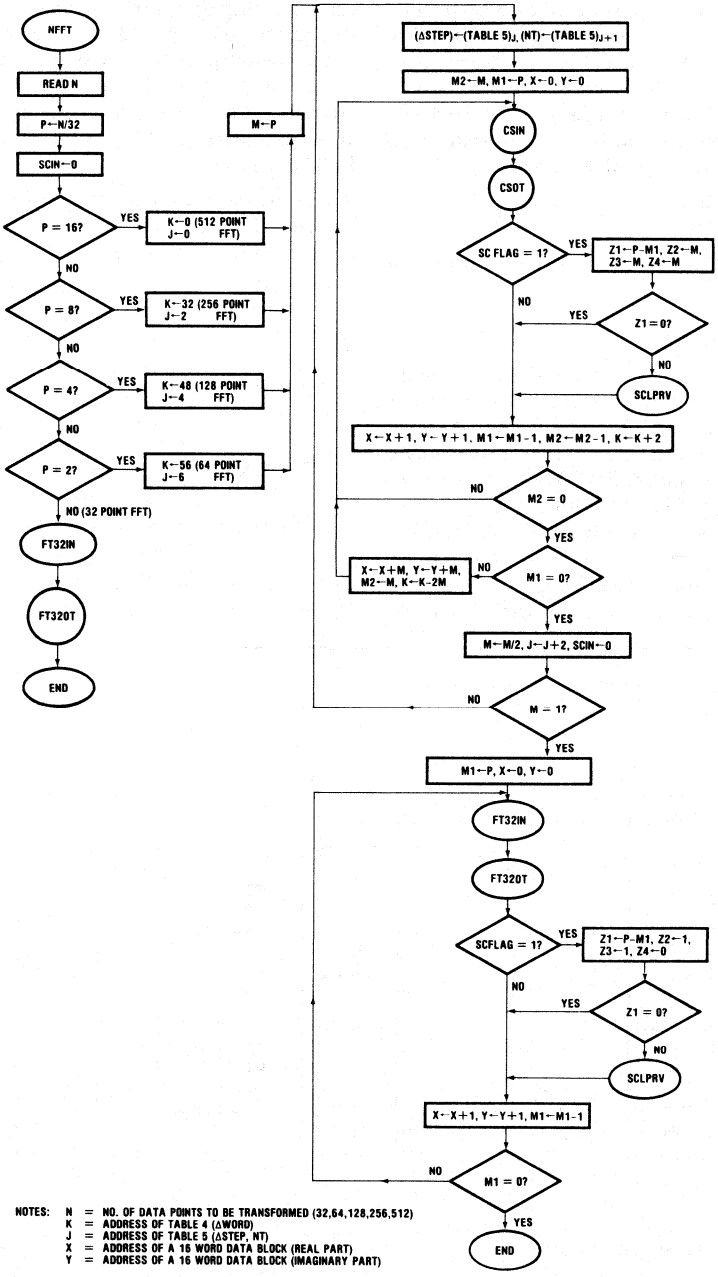


Figure 9. Flow Chart for N Point FFT, Routine "NFFT"



NOTES: N = NO. OF DATA POINTS TO BE TRANSFORMED (32,64,128,256,512)
K = ADDRESS OF TABLE 4 (ΔWORD)
J = ADDRESS OF TABLE 5 (ΔSTEP, NT)
X = ADDRESS OF A 16 WORD DATA BLOCK (REAL PART)
Y = ADDRESS OF A 16 WORD DATA BLOCK (IMAGINARY PART)

Figure 10. Flowchart for Subroutine "SCLPRV"

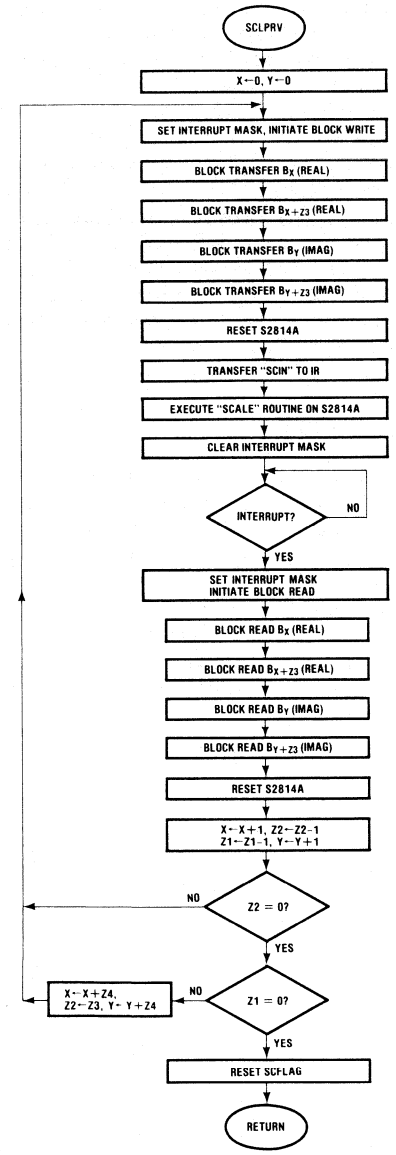


Table 4. (ΔWORD)

ENTRY PT for	K	VALUE	COMMENTS
512→	0	80	(ΔWORD H)
point	1	00	(ΔWORD L)
x'form	2	88	
	3	00	
	4	90	
	5	00	
	6	98	
	7	00	
	8	A0	
	9	00	
	10	A8	
	11	00	
	12	B0	
	13	00	
	14	B8	
	15	00	
	16	C0	
	17	00	
	18	C8	
	19	00	
	20	D0	
	21	00	
	22	D8	
	23	00	
	24	E0	
	25	00	
	26	E8	
	27	00	
	28	F0	
	29	00	
	30	F8	
	31	00	
256→	32	80	
point	33	10	
x'form	34	90	
	35	10	
	36	A0	

Table 4 (continued)

ENTRY PT for	K	VALUE
	37	10
	38	B0
	39	10
	40	C0
	41	10
	42	D0
	43	10
	44	E0
	45	10
	46	F0
	47	10
128 → point x'form	48	80
	49	30
	50	A0
	51	30
	52	C0
	53	B3
	54	E0
	55	30
64 → point x form	56	80
	57	70
	58	C0
	59	70

Table 5. (ΔSTEP, NT)

ENTRY PT for	J	VALUE	COMMENTS
512 point	0	08	(ΔSTEPH)
x'form	1	0F	NT
256	2	10	"
	3	07	"
128	4	20	"
	5	03	"
64	6	40	"
	7	01	"

Hardware.

The minimum hardware for a 32 point FFT is shown in Figure 11. All data transfer and control is handled by the S6802. The availability of the next input sample is signalled with the NMI line. A suitable analog interface is shown in Figure 12. The sampling clock is derived from the microprocessor clock, and the NMI signal is generated by the EOC (end of conversion) output of the A/D converter. This system may be expanded simply by adding more memory. The memory requirements are shown in Table 6. A word may be up to 16 bits long. In order to speed up the complete procedure it is necessary to use DMA for block transfer of data. The S2814A will transfer data at up to 4Mbytes/sec. A suitable DMA Address Generator is the Advanced Micro Devices AM 2940, but a 6844 will accomplish the function more conveniently at a slightly lower speed (1Mbyte/sec).

Data Bus Interface.

Figure 13 shows how to interface the S2814A with a typical 6800 family microprocessor data bus. Note that the S2814A data bus must be isolated from the microprocessor system data bus by use of a PIA as in Figure 11 or a 74LS245 or 74LS645 type data transceiver as shown in Figure 13. The S2814A data bus does not go into a high impedance state when the device is in the read mode ($R/\overline{W}=1$) even if the interface is not enabled ($\overline{IE}=1$). For this reason data bus isolation is necessary to avoid bus conflict.

Figure 11. 32/64 Joint FFT Hardware

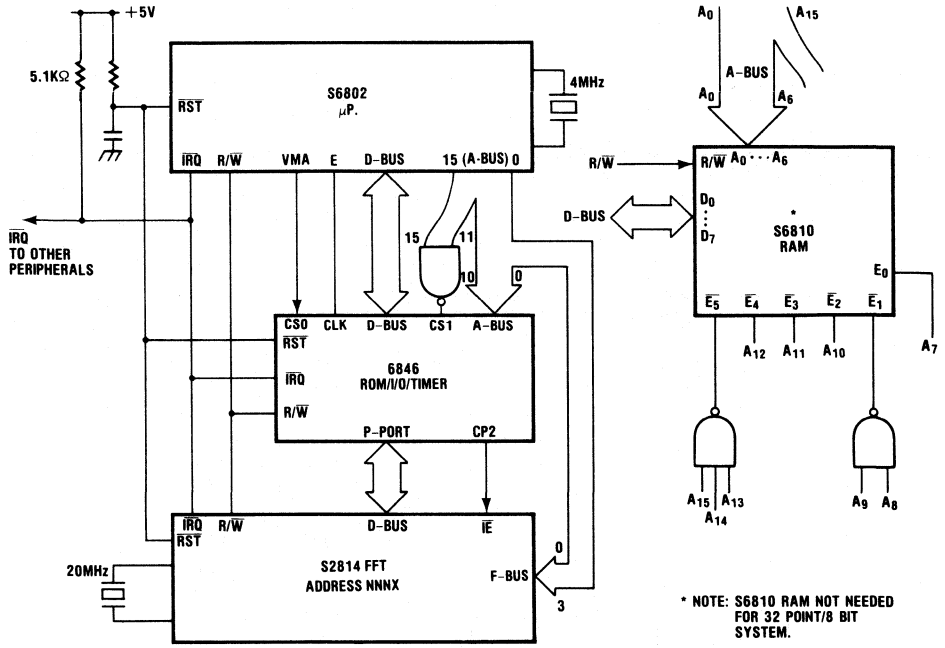


Figure 12. Analog Interface

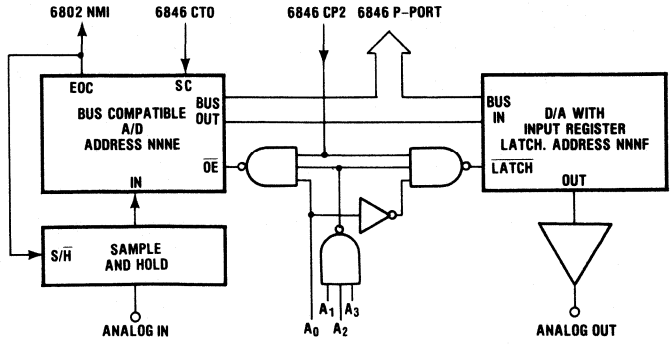


Figure 13. Interfacing the S2814A with a Microprocessor

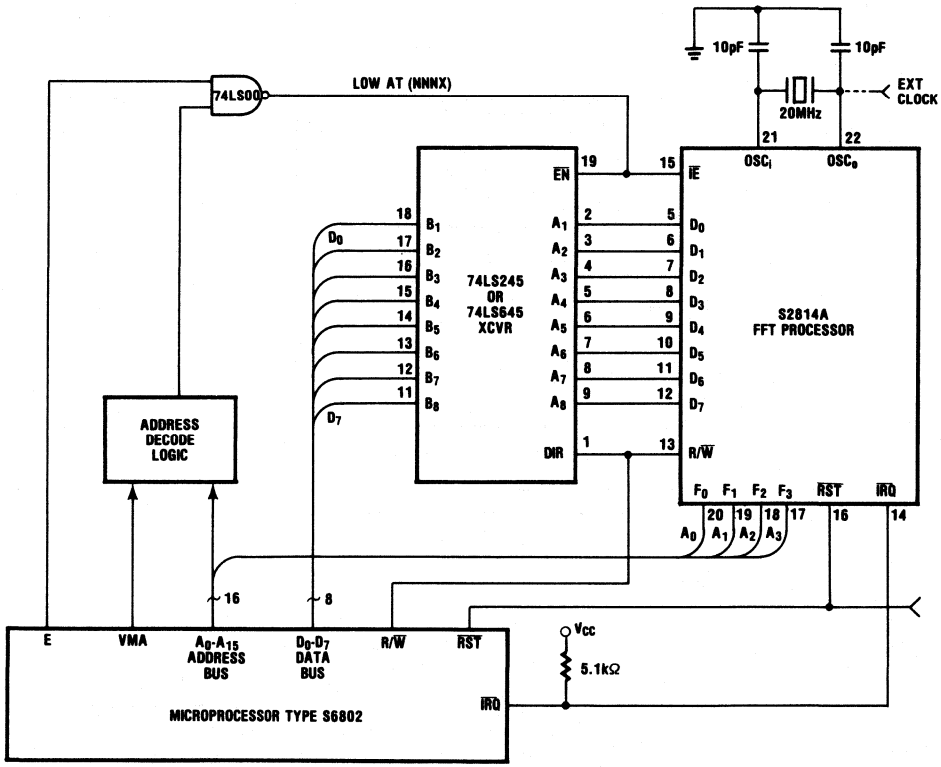


Table 6. Memory requirements for data point storage.

TRANSFORM SIZE (POINTS)	WORD LENGTH (BITS)	MEMORY REQUIREMENTS
32	8	64 bytes
	10/12	See Note 1
	16	128 bytes
64	8	128 bytes
	10/12	See Note 1
	16	256 bytes
128	8	256 bytes
	10/12	768 nibbles
	16	1024 bytes
256	8	512 bytes
	10/12	1536 nibbles
	16	1024 bytes
512	8	1024 bytes
	10/12	3072 nibbles
	16	2048 bytes

Note 1: In practice the memory realization for these cases will be the same as for 16-bit systems.

Transform Execution Times.

The maximum execution times of transforms is shown in Table 7. The actual execution time when CAS is enabled will be between the times shown for CAS off and the maximum with CAS on. It will depend on the number of times that scaling has to be done.

FFT Resolution and Dynamic Range

The use of the Decimation in Frequency (DIF) algorithm in the S2814A ensures optimum signal to noise ratio, (SNR) for the architecture used. The use of the Conditional Array Scaling (CAS) gives a total dynamic range of approximately 70dB on all sizes of Transforms. The maximum resolution obtainable is approximately 57dB. CAS operates by detecting overflow in the butterfly computation routine. As soon as an overflow is detected the two points being combined in that butterfly are halved in magnitude (both the real and imaginary portions) and the butterfly recomputed. A flag is set, all previously computed butterfly outputs are then scaled, and all the inputs to subsequent butterflies are scaled before computation begins, so that at the end of the pass all points have been scaled equally. A scale factor is made available (SCOUT) so that the remaining data points in larger transforms, i.e., those other than the 32 in the S2814A when the overflow occurred, may also be scaled to keep them all in line. Thus, CAS operates as a discrete AGC, halving the signal levels each time an overflow is detected. By using SCOUT after executing the FFT the output may be expanded, so that the levels displayed in the spectrum will increase monotonically as the input increases.

Table 4. Total FFT execution times including block transfers. (msec.)

TRANSFORM SIZE	USING SINGLE S2814A BLOCK TRANSFER USING:				USING MULTIPLE S2814A ARRAY		
	S6802 (22μsec/word)		DMA 2MW/sec		# OF S2814As	(USING DMA AT 2MW/sec)	
	MIN	MAX	MIN	MAX		MIN	MAX
32 pt.	4.0	4.6	1.3	1.9	1	1.3	1.9
64	14.2	15.7	3.2	4.6	2	1.6	2.3
128	40.7	44.0	7.6	11.0	4	1.9	2.8
256	106	114	17.8	25.4	8	2.3	3.2
512	262	280	40.7	57.9	16	2.6	3.7

Note: Minimum times assume that CAS and PSF are off. Maximum times assume that CAS and PSF are on, and that maximum overflow occurs during 1st pass.

AMERICAN MICROSYSTEMS, INC.

ADVANCED PRODUCT DESCRIPTION

S2815

DIGITAL FILTER/UTILITY PERIPHERAL

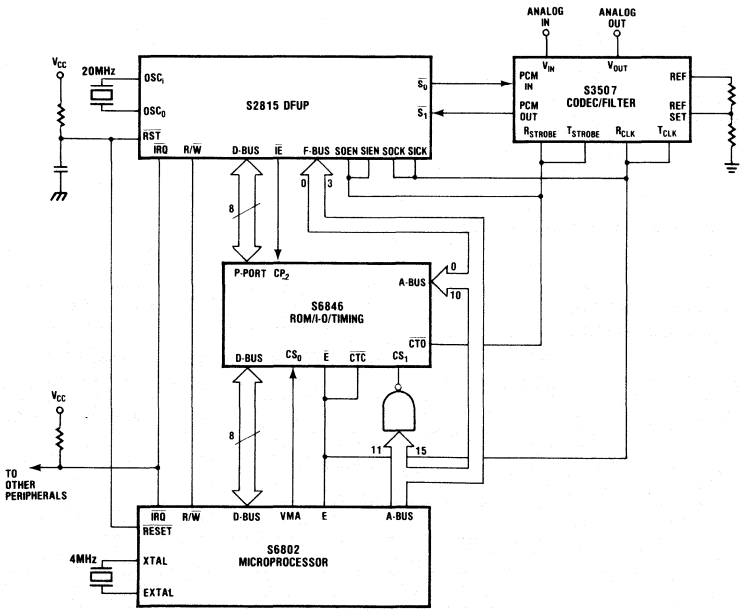
Features

- ☐ **S2811 Signal Processing Peripheral Programmed With Filter and Utility Routines**
- ☐ **Microprocessor Compatible I/O Interface**
- ☐ **Two Independent 32 Tap Transversal Filter Routines, Cascadable into a Single 64 Tap Filter**
- ☐ **Two Recursive (biquadratic) Filters Providing a Total of 16 Filter Sections**
- ☐ **Computation Functions: Two Integrating, Two Rectifying, Squaring, and Block Multiply Routines**
- ☐ **Conversion Functions: μ255 Law-to-Linear, Linear-to-μ255 Law, and Linear-to-dB Transformations**
- ☐ **Generator Functions: Sine and Pseudo-Random Noise Patterns**

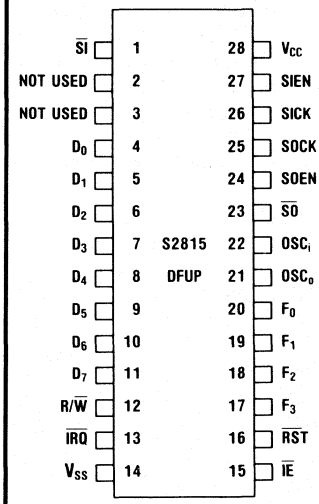
General Description

The AMI S2815 Digital Filter/Utility (DFUP) is a programmed version of the S2811. Architectural and internal operating details of the S2811 may be found in the S2811 Advanced Product Description. The S2815 has been programmed with a collection of filter, computational, conversion, and generator routines which may be selected individually, or cascaded under control of the host processor. This arrangement allows a wide range of

Typical System Configuration



Pin Configuration



General Description (Continued)

signal processing functions frequently required in application areas such as telecommunications, test and instrumentation, industrial automation, process control, etc., to be satisfied by a single S2815 DFUP.

The I/O structure of the S2815 provides flexibility and easy interfacing in microprocessor based systems. Input and output data transfers may be accomplished serially, as shown in the block diagram, using a μ255-law Codec such as the S3507, or using linear A/D and D/A converters. Data may also be transferred in parallel under control of a host processor, such as the S6802. Routines may be executed individually, completely under control of the host processor, or flags may be set up by the host, allowing routines to be cascaded internally. The ability to cascade routines allows complicated functions to be completed without intervention by the host processor.

DTMF BANDSPLIT FILTER

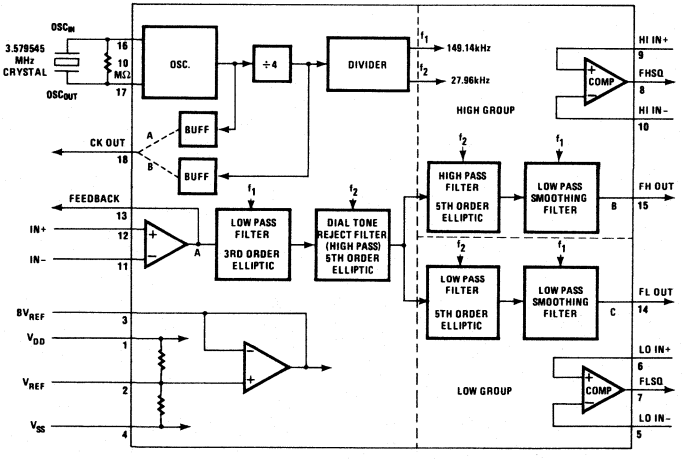
Features

- ☐ **CMOS Technology for Wide Operating Single Supply Voltage Range (7.0V to 13.5V). Dual Supplies (±3.5V to ±6.75V) Can Also Be Used.**
- ☐ **Uses Standard 3.58MHz Crystal as Time Base. Provides Buffered Clock to External Decoder Circuit.**
- ☐ **Ground Reference Internally Derived and Brought Out.**
- ☐ **Programmable Gain Differential Input Amplifier Stage.**
- ☐ **Filter and Limiter Outputs Separately Available Providing Analog or Digital Outputs of Adjustable Sensitivity.**
- ☐ **Can be Used with Variety of Available Decoders to Build 2-Chip DTMF Receivers.**

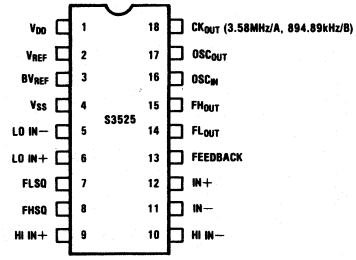
General Description

The S3525 DTMF Bandsplit Filter is a 18-pin monolithic CMOS integrated circuit designed to implement a high quality DTMF tone receiver system in conjunction with a suitable decoder circuit. The device includes a dial tone filter, high group and low group separation filters and limiters for squaring of the filtered signals. An uncommitted input amplifier allows a programmable gain stage or anti-aliasing filter. An overall signal gain of 6dB is provided for the low group and high group signals in the circuit. The dial tone filter is designed to provide a rejection of at least 52dB in the frequency band of 300Hz to 500Hz. The difference between the S3525A and the S3525B is the frequency of output clock signal at the CKOUT pin. In the S3525B, it is a 894.89kHz square wave while in the S3525A, it is a 3.58MHz buffered oscillator signal. The S3525A can be used with digital DTMF decoder chips that need the TV crystal time base allowing use of only one crystal between the filter and decoder chips.

Block Diagram



Pin Configuration



Absolute Maximum Ratings:

DC Supply Voltage (V_{DD} - V_{SS}) ..... +15.0V
Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −55°C to +125°C
Analog Input ..... V_{SS} −0.3V V_{IN} V_{DD} +0.3V

DC Electrical Operating Characteristics: T_A = 0°C to +70°C

Symbol	Parameter/Conditions		Min.	Typ.	Max.	Units
V_{DD}	Positive Supply (Ref to V_{SS})		9.6	12.0	13.5	V
$V_{OL(CKOUT)}$	Logic Output "Low" Voltage I_{OL} = 160μA			V_{SS} + 0.4		V
$V_{OH(CKOUT)}$	Logic Output "High" Voltage I_{OH} = 4μA			V_{DD} − 1.0		V
$V_{OL(FH, FL)}$	Comparator Output Voltage Low	500pF Load			V_{SS} + 0.5	V
		10kΩ Load			V_{SS} + 2.0	V
$V_{OH(FH, FL)}$	Comparator Output Voltage High	500pF Load	V_{DD} − 0.5			V
		10kΩ Load	V_{DD} − 2.0			V
$R_{INA\ (IN-,IN+)}$	Analog Input Resistance		8			MΩ
$C_{INA\ (INA-,\ IN+)}$	Analog Input Capacitance				15	pF
V_{REF}	Reference Voltage Out		0.49 (V_{DD} − V_{SS})	0.50 (V_{DD} − V_{SS})	0.51 (V_{DD} − V_{SS})	V
V_{OR} = [BV_{REF}-V_{REF}]	Offset Reference Voltage				50	mV
P_D	Power Dissipation	V_{DD} = 10V		170		mW
		V_{DD} = 12.5V		400		mW
		V_{DD} = 13.5V and 0°C			650	mW

AC System Specifications:

Symbol	Parameter/Conditions		Min.	Typ.	Max.	Units
A_F	Pass Band Gain		5.5	6	6.5	dB
	Dial Tone Rejection					
	Dial Tone Rejection is measured at the output of each filter with respect to the passband					
DTR_L	Low Group Rejection	350Hz	55	59		dB wrt 700Hz
		440Hz	50	53		dB wrt 700Hz
DTR_H	High Group Rejection	Either Tone	55	68		dB wrt 1200Hz

AC System Specifications (Continued)

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
	Attenuation Between Groups				
	Attenuation of the nearest frequency of the opposite group is measured at the output of each filter with respect to the passband				
GA_L	Attenuation of 1209Hz	50	>60		dB wrt 700Hz
GA_H	Attenuation of 941Hz	40	42		dB wrt 1200Hz
	Total Harmonic Distortion				
THD	Total Harmonic Distortion (dB). Dual tone of 770Hz and 1336 Hz sinewave applied at the input of the filter at a level of 3dBm each. Distortion measured at the output of each filter over the band of 300 Hz to 10kHz ($V_{DD}=12V$)			−40	dB
	Idle Channel Noise				
ICN	Idle Channel Noise measured at the output of each filter with C-message weighting. Input of the filter terminated to BV_{REF}			1	mV_{rms}
	Group Delay (Absolute)				
GD_L	Low Group Filter Delay over the band of 50Hz to 3kHz		4.5	6.0	ms
GD_H	High Group Filter Delay over the band of 50Hz to 3kHz		4.5	6.0	ms

Pin/Function Descriptions

OSC_{IN}, OSC_{OUT} — These pins are for connection of a standard 3.579545MHz TV crystal and a 10MΩ ±10% resistor for the oscillator from which all clocking is derived. Necessary capacitances are on-chip, eliminating the need for external capacitors.

CKOUT (S3525A) — Oscillator output of 3.58MHz is buffered and brought out at this pin. This output drives the oscillator input of a decoder chip that uses the TV crystal as time base. (Only one crystal between the filter and decoder chips is required.)

CKOUT (S3525B) — This is a divide by 4 output from the oscillator and is provided to supply a clock to decoder chips that use 895kHz as time base.

IN−, IN+, Feedback — These three pins provide access to the differential input operational amplifier on chip. The feedback pin in conjunction with the IN− and IN+ pins allows a programmable gain stage and implementation of an anti-aliasing filter if required.

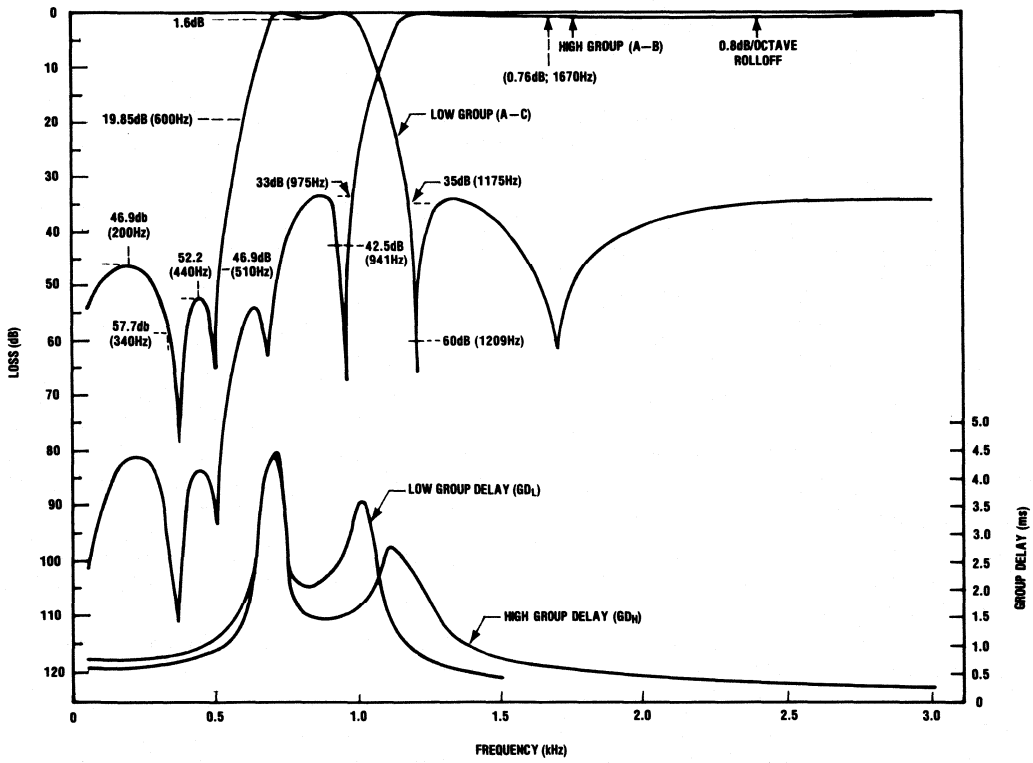
FH OUT, FL OUT — These are outputs from the high group and low group filters. These can be used as inputs to analog receiver circuits or to the on-chip limiters.

HI IN−, HI IN+
LO IN−, LO IN+ — These are inputs of the high group and low group limiters. These are used for squaring of the respective filter outputs. (See Figure 2.)

Pin/Function Descriptions (Continued)

FHSQ, FLSQ	These are respectively the high group and low group square wave outputs from the limiters. These are connected to the respective inputs of digital decoder circuits.
V_{DD}, V_{SS}	These are the power supply voltage pins. The device can operate over a range of $7V \leq (V_{DD} - V_{SS}) \leq 13.5V$.
V_{REF}	An internal ground reference is derived from the V_{DD} and V_{SS} supply pins and brought out to this pin. V_{REF} is $1/2(V_{DD} - V_{SS})$ above V_{SS}.
BV_{REF}	Buffered V_{REF} is brought out to this pin for use with the input and limiter stages.

Figure 1. Typical S3525 DTMF Bandsplit Filter Loss/Delay Characteristics



Input Configurations

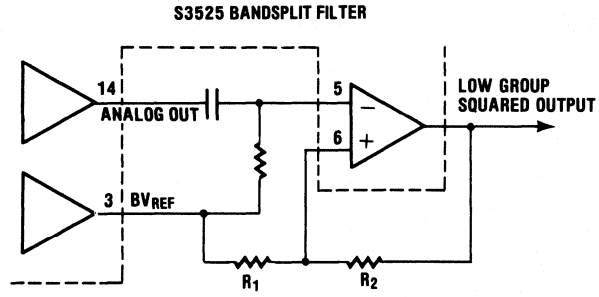
The applications circuits show some of the possible input configurations, including balanced differential and single ended inputs. Transformer coupling can be used if desired. The basic input circuit is a CMOS op amp which can be used for impedance matching, gain adjustment, and even filtering if desired. In the differential mode, the common mode rejection is used to reject power line-induced noise, but layout care must be taken to minimize capacitive feedback from pin 13 to pin 12 to maintain stability.

An important fact to remember is that the filters have approximately 6dB gain and the inputs must be kept low enough that the analog outputs (FL_{OUT} and FH_{OUT}) are not clipping.

Output Considerations

The S3525 has both analog and digital outputs available. Most integrated decoder circuits require digital inputs so the on-chip comparators with hysteresis are used to square the analog outputs. The sensitivity of the receiver system can be set by the ratio of R1 and R2, shown in Figure 2. The amount of hysteresis will eliminate noise response as well as set the basic sensitivity.

Figure 2. Typical Squaring Circuit



ASSUMING $BV_{REF} = 0$ OR $\frac{1}{2}(V_{DD}-V_{SS})$ then

$UTP = E_{O(SAT)} \frac{R_1}{R_1 + R_2}$

$LTP = -E_{O(SAT)} \frac{R_1}{R_1 + R_2}$

Clock Considerations

The clock is provided by a standard 3.58MHz TV crystal in parallel with a 10MΩ resistor across pins 16 and 17. A buffered output at pin 18 is provided to drive the companion decoder at 3.58MHz (S3525A) or 895kHz (S3525B). It can be directly coupled or capacitively coupled depending on the decoder.

The circuits shown are not necessarily optimal but are intended to be good starting points from which an optimal design can be developed for each individual application.

Applications

Companion decoders to be used with the S3525 vary in performance and features. Teltone Corporation's TT6174, Rockwell Microelectronic's CRC8030 and MOSTEK's MK5102/03 are available units that can be used with the S3525.

Figure 3. AMI/Teltone 2 Chip DTMF Receiver

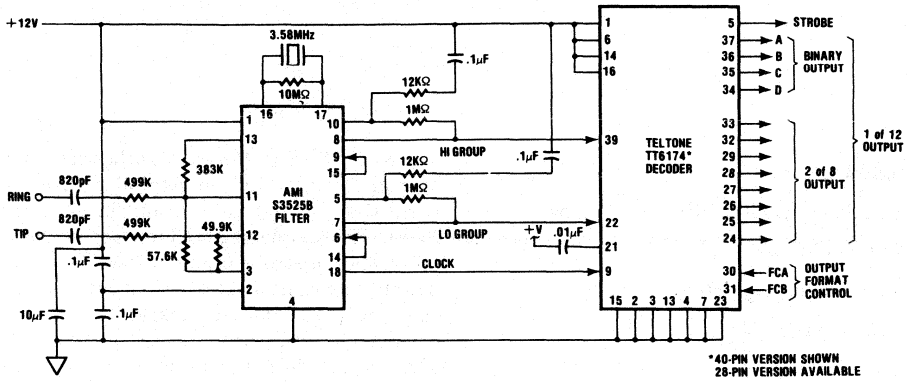


Figure 4. AMI/Rockwell 2 Chip DTMF Receiver

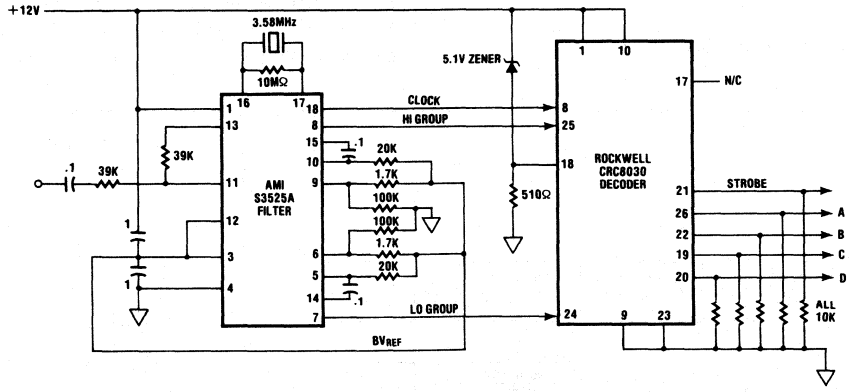
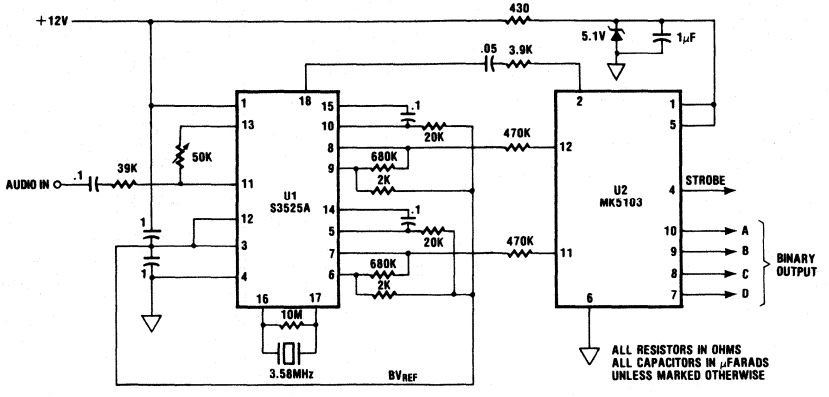


Figure 5. AMI/MOSTEK 2 Chip DTMF Receiver



Additional information can be obtained from the S3525 Applications Note available on request from AMI, and from the suppliers of the decoder circuits.

AMERICAN MICROSYSTEMS, INC.

ADVANCED PRODUCT DESCRIPTION

S3610

LPC-10 SPEECH SYNTHESIZER WITH ON-CHIP 20K SPEECH DATA ROM

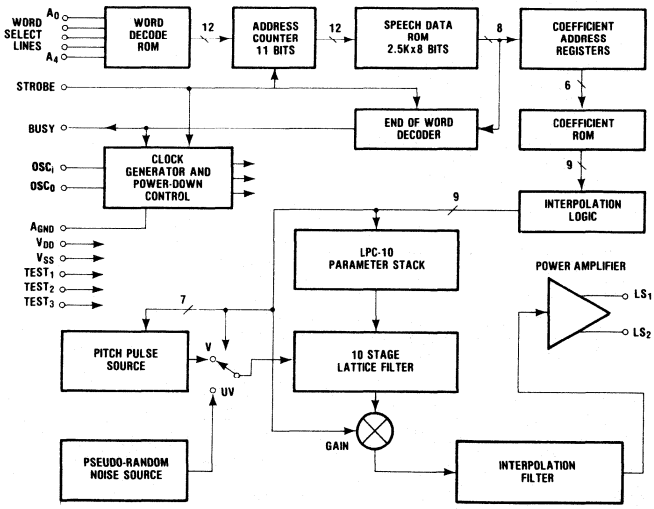
Features

- ☐ Simple Digital Interface
- ☐ CMOS Switched-Capacitor Filter Technology
- ☐ Automatic Powerdown
- ☐ Single Power Supply Operation
- ☐ Direct Loudspeaker Drive
- ☐ 30mW Audio Output
- ☐ 20K Bits Speech ROM
- ☐ Low Data Rate
- ☐ Up to 32 Word Vocabulary

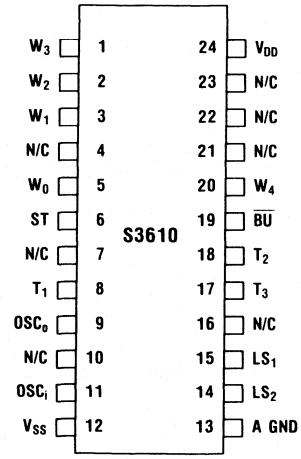
General Description

The S3610 LPC-10 Speech Synthesizer generates speech of high quality and intelligibility from LPC (Linear Predictive Coding) data stored in an internal 20K bit ROM. The simple digital interface consists of 5 word-select lines, a strobe input to load the address data and initiate operation, and a busy output signal. At the end of enunciation the chip automatically goes into the power-down mode until a new word select address is strobed in. The data rate from the speech ROM into the synthesizer is 2.0K bits/sec max. Typically the average data rate will be reduced to about 1.2K bits/sec. by means of the data rate reduction techniques used internally, giving about 17 seconds of speech from the ROM data. The 5 word-select lines allow a maximum vocabulary of 32 words.

Block Diagram



Pin Configuration



N/C = NO CONNECTION

LPC-10 SPEECH SYNTHESIZER

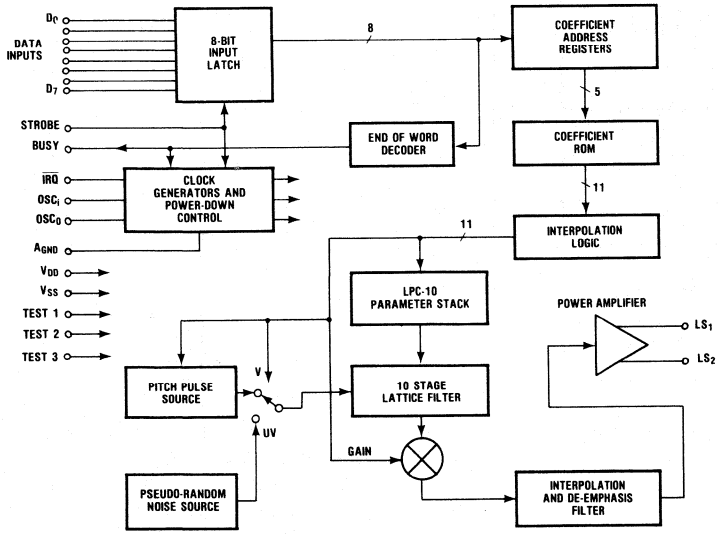
Features

- ☐ Simple Microprocessor Interface
- ☐ CMOS Switched-Capacitor Filter Technology
- ☐ Automatic Powerdown
- ☐ Single Supply Operation
- ☐ Direct Loudspeaker Drive
- ☐ 30mW Audio Output
- ☐ Low Data Rate

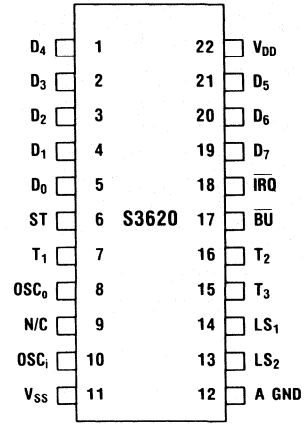
General Description

The S3620 LPC-10 Speech Synthesizer generates speech of high quality and intelligibility from LPC (Linear Predictive Coding) data stored in an external memory. The digital interface circuitry is fully microprocessor compatible and allows the processor to load the data with or without a DMA controller. The loading takes place on a handshake basis, and in the absence of a response from the processor the synthesizer automatically shuts down and goes into the powerdown mode. A busy signal allows the processor to sense the status of the synthesizer. The input data rate is 2.0K bits/sec. max., but typically the average data rate will be reduced to about 1.4K bits/sec. by means of the data rate reduction techniques used internally.

Block Diagram



Pin Configuration



N/C = NO CONNECTION

AMERICAN MICROSYSTEMS, INC.

ADVANCED PRODUCT DESCRIPTION

S3630A/B

128K (16K×8) BIT NMOS ROM

Features

- ☐ Single +5V Power Supply
- ☐ Directly TTL Compatible Inputs
- ☐ Directly TTL Compatible Outputs, Three State on S3630A
- ☐ Low Power: Supply Current-20mA Max.
- ☐ Power Down Capability (S3630A)

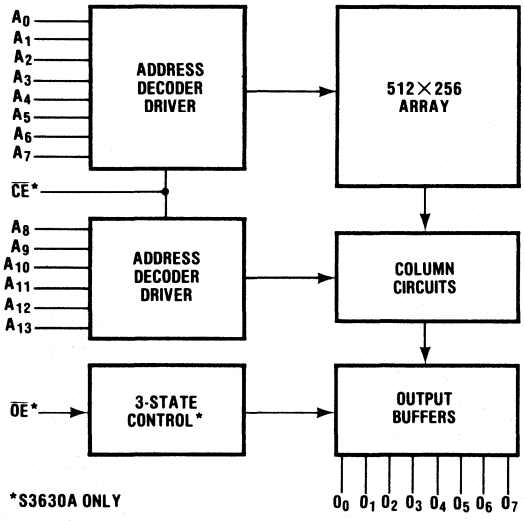
General Description

The S3630A/B is a high density 131072 bit NMOS mask programmable Read Only Memory. The device is fully TTL compatible and the organization as 16K×8 bits makes it very suitable for use in microprocessor systems. It is available in both 6μsec and 10μsec versions.

The S3630 is available in two pin configurations. The S3630A has the industry standard pinout (28-pin package). The S3630B has a minimum pin configuration, allowing it to be packaged in a 24-pin DIL pack, saving valuable board space where this configuration is usable, as well as reducing costs.

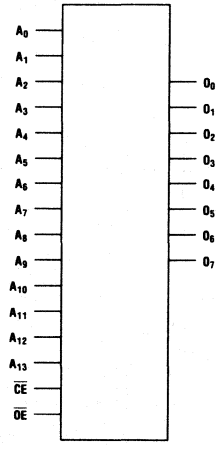
The S3630 is manufactured in a high density silicon gate, depletion load, N-channel process. Its high data capacity makes it extremely suitable for use in speech synthesis systems.

Block Diagram



*S3630A ONLY

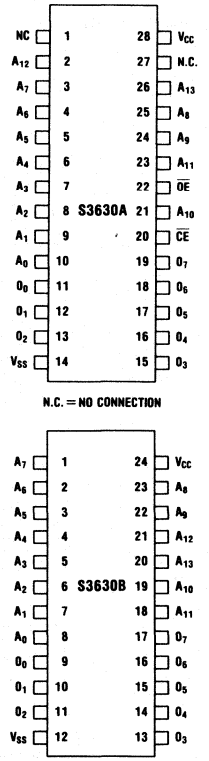
Logic Symbol



Pin Names

A_0-A_{13}	Address Inputs
O_0-O_7	Data Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable

Pin Configuration



N.C. = NO CONNECTION

Contact factory for complete data sheet

REMOTE CONTROL CIRCUITS

Part No.	Description	Process	Power Supply	Packages
S2600	Remote Control Encoder	CMOS	+7V to 10V	16 Pin
S2601	Remote Control Decoder	P-I^2	+10V to 18V	22 Pin
S2602	Remote Control Encoder	CMOS	+9V	16 Pin
S2603	Remote Control Decoder	PMOS	+9V	22 Pin
S2742	Remote Control Decoder	PMOS	+9V	18 Pin
S2743	Remote Control Encoder	PMOS	+9V	16 Pin

CLOCK CIRCUITS

Part No.	Description	Process	Power Supply	Digits	Packages
S2709	Fluorescent Automotive Digital Clock (12 Hour)	P-I^2	+12V	4	22 Pin
S4003	Fluorescent Automotive Digital Clock (12 Hour + Date + Rally Timer)	P-I^2	+12V	4	40 Pin

DISPLAY DRIVER

Part No.	Description	Process	Power Supply	Outputs	Packages
S2809	Universal Display Driver	P-I^2	+8V to +22V	32	40 Pin

ORGAN CIRCUITS

Part No.	Description	Process	Power Supply	Power Dissipation	Packages
S10110	Analog Shift Register	P-I^2	−24V		8 Pin
S10129	Six-Stage Frequency Divider	P-I^2	−14V to −27V	350mW	14 Pin
S10130	Six-Stage Frequency Divider	P-I^2	−14V to −27V	350mW	14 Pin
S10131	Six-Stage Frequency Divider	P-I^2	−14V to −27V	350mW	14 Pin
S10430	Divider-Keyer	P-I^2 MOS	−14V to −27V	350mW	40 Pin
S2567	Rhythm Counter	HI V_T	−15V to −27V	400mW	14 Pin
S2688	Noise Generator	P-I^2	−14V to −27V	350mW	8 Pin
S8890	Rhythm Generator	P-I^2	−12V	400mW	40 Pin
S9660	Rhythm Generator	P-I^2	−12V	400mW	28 Pin
S50240	Top Octave Synthesizer	P-I^2	−11V to −16V	360mW	16 Pin
S50241	Top Octave Synthesizer	P-I^2	−11V to −16V	360mW	16 Pin
S50242	Top Octave Synthesizer	P-I^2	−11V to −16V	360mW	16 Pin
S50243	Top Octave Synthesizer	P-I^2	−11V to −16V	360mW	16 Pin
S50244	Top Octave Synthesizer	P-I^2	−11V to −16V	360mW	16 Pin
S50245	Top Octave Synthesizer	P-I^2	−11V to −16V	360mW	16 Pin

AMERICAN MICROSYSTEMS, INC.

ADVANCED PRODUCT DESCRIPTION

S2600/S2601

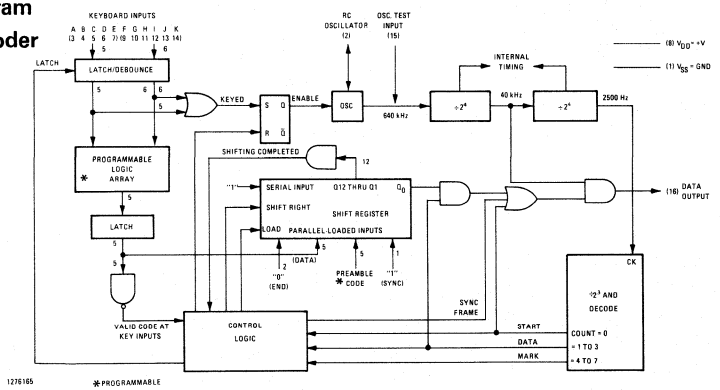
ENCODER/DECODER REMOTE-CONTROL 2-CHIP SET

CONSUMER

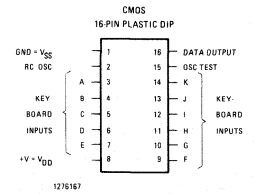
Features

- ☐ Small Parts Count — No Crystals Required
- ☐ Easily Used in LED, Ultrasonic, RF, or Hard-wire Transmission Schemes
- ☐ Very Low Reception Error
- ☐ Low Power Drain CMOS Transmitter for Portable and Battery Operation
- ☐ 31 Commands — 5-bit Output Bus with Data Valid
- ☐ 3 Analog (LP Filterable PWM) Outputs
- ☐ Muting (Analog Output Kill/Restore)
- ☐ Indexing Output — 2½ Hz Pulse Train
- ☐ Toggle Output (On/Off)
- ☐ Mask-Programmable Codes

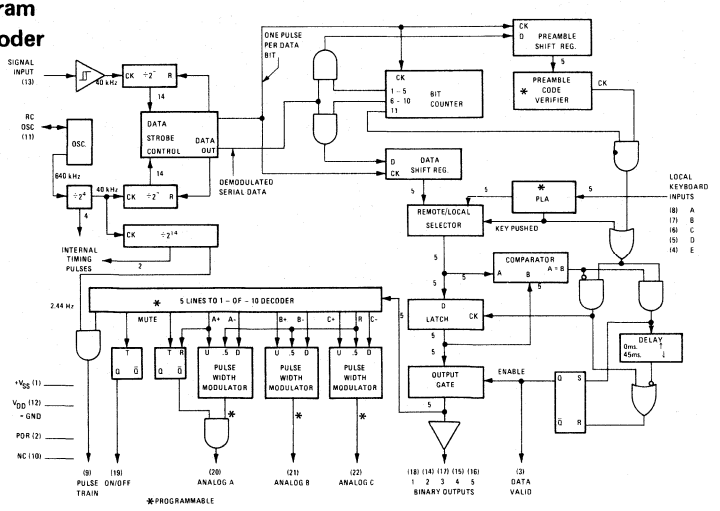
Block Diagram S2600 Encoder



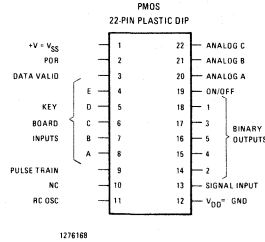
Pin Configuration S2600



Block Diagram S2601 Decoder



Pin Configuration S2601



Functional Description

The S2600/S2601 is a set of two LSI circuits which allows a complete system to be implemented for remote control of televisions, toys, security systems, industrial controls, etc. The choice of transmission medium is up to the user and can be ultrasonic, infrared radio frequency, or hardwire such as twisted pair or telephone.

The use of a synchronizing marker technique has eliminated the need for highly accurate frequencies generated by crystals. The S2600 Encoder typically generates a 40kHz carrier which it amplitude-modulates with a base-band message of 12 bits, each bit preceded by a synchronizing marker pulse.

Bits 1 and 12 denote sync and end-of-message, respectively, bits 2 thru 6 constitute a fixed preamble which must be received correctly for the command bits to be received, and bits 7 through 11 contain the command data. The S2601 Decoder produces an output only after two complete, consecutive, identical, 12-bit transmissions. Marker pulses, preamble bits, and redundant transmissions, have given the S2600/S2601 system a very high immunity to noise, without a large number of discrete components.

S2600 Encoder

The S2600 is a CMOS device with an on-chip oscillator, 11 keyboard inputs, a keyboard encoder, a shift register, and some control logic. The oscillator requires only an external resistor and capacitor, and to conserve power, runs only during transmission. Keyboard inputs are active-low, and have internal pull-up resistors to V_{DD}. When one keyboard input from the group A through E is activated with one from the group F through K, the keyboard encoder generates a 5-bit code, as given in the table entitled "S2600/S2601 CODING," below. This code is loaded into a shift register in parallel with the sync, preamble, and end bits, to form the 12-bit message.

The transmitter output is a 40 kHz square wave of 50% duty factor which has been pulse-code-modulated by (i.e., ANDed with) a signal having a recurring pattern, a bit frame of 3.2 millisecond duration. This bit frame is comprised of three signals: the Start signal which is 0.4 milliseconds of logic "1"; followed by the Data signal which is 1.2 milliseconds of the lowest-order shift register bit; followed by the Mark signal which is 1.6 milliseconds of logic "0" (except in the first bit frame where Mark = 1 to facilitate receiver synchronization).

The shift register is clocked once per bit frame, so that its 12-bit message is transmitted once in a 38.4 milliseconds. The minimum number of transmissions that can occur is two, but if the keyboard inputs are active after the first 3.6 milliseconds of any 12-bit transmission, one more 12-bit transmission will result. Transmissions are always complete, never truncated, regardless of the keyboard inputs.

The Test Input is used for functional testing of the device. A low level input will cause the oscillator frequency to be gated to the Data Output pin. This input has an internal pull-up resistor to V_{DD}.

S2601 Decoder

The S2601 is a PMOS LSI device with an on-chip oscillator, five keyboard inputs, a 40kHz signal input, and 11 outputs. The oscillator requires only an external R and C. The five keyboard inputs are active-low with internal pull-up resistors to V_{SS}; activation of any two causes one of 10 possible 5-bit codes to be generated and fed to the outputs of the S2601, overriding any 40kHz signal input.

Two counters, the signal counter and the local counter, are clocked respectively by the signal input and a 40kHz signal from the local RC oscillator timing chain. A 40kHz input lasting 3.2 milliseconds (i.e., an initial bit frame) causes the signal counter to overrun and reset both itself and the local counter. At specific intervals thereafter, the local counter generates pulses used to interrogate the contents of the signal counter. Resynchronization of the counters occurs every bit frame so that the interrogation yields valid data bits even if the transmitter oscillator frequency has deviated up to ±24% with respect to the receiver oscillator frequency.

Decoded data bits from the next five bit frames following the initial synchronizing frame are compared with the fixed preamble code. The next five decoded bits, the command bits, are converted to a parallel format and are compared against the command bits saved from the prior transmission. If they match, and if the preamble bits are correct, the command bits are gated to the receiver outputs. However, a mismatch causes the receiver outputs to be immediately disabled, and the new command bits are saved for comparison against the command bits from the next 12-bit transmission. In the case where 2 identical, proper, 12-bit transmissions are immediately followed either by transmissions with erroneous pream-

ble codes or by nothing, the receiver outputs will be activated during the end-frame of the second transmission, and will be disabled 45 milliseconds thereafter. In the rest (disabled) state the five Binary Outputs are at a "1" logic level; when not in the rest state, one or more of the open-sourced output transistors will conduct to V_{DD}. The Data Valid output is low during the rest state, and high whenever data is present at the Binary Outputs.

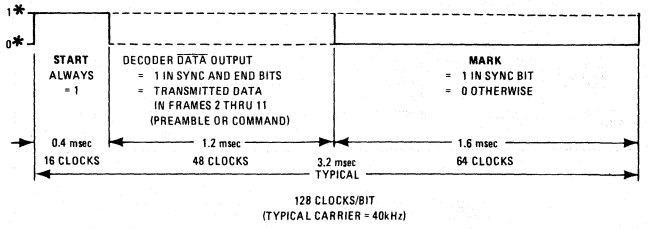
The S2601 has five other outputs: Pulse Train, On/Off, Analog A, Analog B, and Analog C. The states of these outputs are controlled by the 10 particular Binary Output codes which the receiver Keyboard Inputs can cause to be generated. The Pulse Train output provides a 2.44Hz square wave (50% duty factor) whenever 11011 appears at the Binary Outputs, but otherwise it remains at a logic "0". This pulse train can be used for indexing, e.g., for stepping a TV channel selector.

The On/Off ("mains") output changes state each time 01111 appears at the Binary Outputs. In TV applications the On/Off output is most often used to kill and restore the main power supply.

Analog Outputs A, B and C are 10kHz pulse trains whose duty factors are independently controllable. With a simple low-pass filter each of these outputs can provide 64 distinct DC levels suitable for control of volume, color saturation, brightness, motor speed, etc. Each Analog Output increases its duty factor in response to a particular Binary Output code and decreases its duty factor in response to another code—6 codes in all. The entire range of 0% to 100% duty factor can be traversed in 6.5 seconds or at a rate of the oscillator frequency divided by 65,536. All three Analog Outputs are set to 50% duty factor whenever 01011 appears at the Binary Outputs. Analog A is mutable; 01100 sets it to 0% duty factor. If 01100 then disappears and reappears, the original duty factor is restored. This of course implements the TV "sound killer" feature.

The S2601 has an on-chip power-on reset (POR) circuit which sets the Pulse Train and On/Off Outputs to "0", sets the Analog Outputs at 50% duty factor, and insures that Analog A is muted. No external components are required to implement POR, but a POR input has been provided for applications where externally controlled reset is desirable, e.g., where the power supply voltage rise time is extremely slow. The POR input has an internal resistor pull-up to V_{SS}; pulling it low causes a reset.

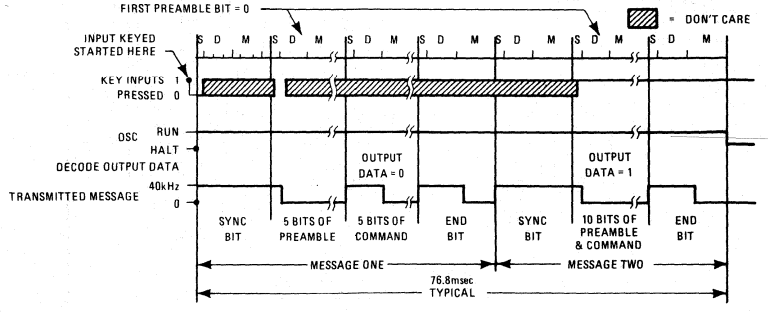
Message Bit Format



* "1" MEANS PRESENCE OF A 40kHz CARRIER (SQUARE WAVE); "0" MEANS ABSENCE OF A 40kHz CARRIER (SQUARE WAVE).

** IF MESSAGE BIT = "1" THEN DECODER DATA OUTPUT = ENCODER DATA INPUT = "0";
IF MESSAGE BIT = "0" THEN DECODER DATA OUTPUT = ENCODER DATA INPUT = "1".

Message Format



AN MICROSYSTEMS, INC.

ADVANCED PRODUCT DESCRIPTION

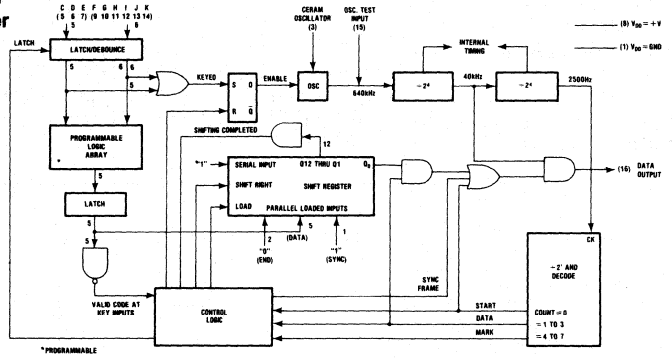
S2602/S2603

ENCODER/DECODER REMOTE-CONTROL 2-CHIP SET

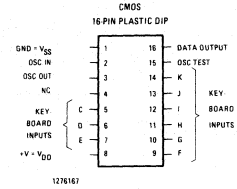
atures

- ☐ Accurate Data Transmission - No Frequency Trimming Required
- ☐ Easily Used in LED, Ultrasonic, RF, or Hardwire Transmission Schemes
- ☐ Very Low Reception Error
- ☐ Low Power Drain CMOS Transmitter for Portable and Battery Operation
- ☐ 18 Commands—5-bit Output Bus with Data Valid
- ☐ Analog (LP Filterable PWM) Output
- ☐ Muting (Analog Output Kill/Restore)
- ☐ Toggle Output (On/Off)
- ☐ Mask-Programmable Codes

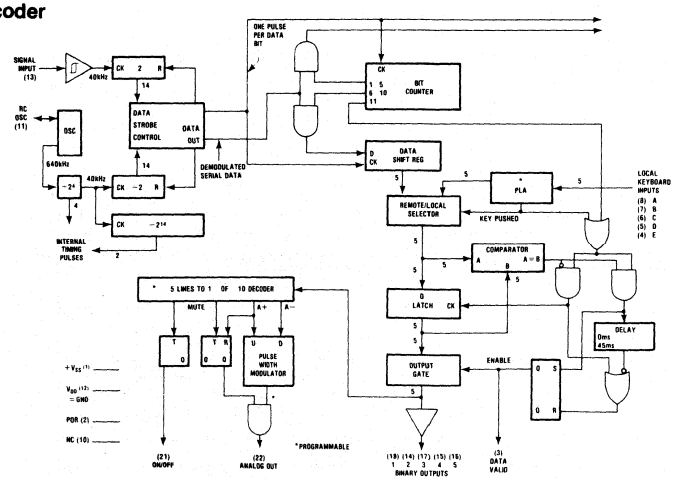
Block Diagram S2602 Encoder



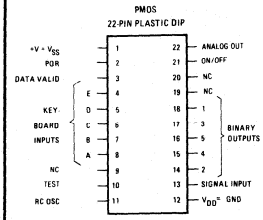
Pin Configuration S2602



Block Diagram S2603 Decoder



Pin Configuration S2603



Functional Description

The S2602/S2603 is a set of two LSI circuits which allows a complete system to be implemented for remote control of televisions, toys, security systems, industrial controls, etc. The choice of transmission medium is up to the user and can be ultrasonic, infrared radio frequency, or hardwire such as twisted pair or telephone.

The use of a ceramic resonator with the S2602 Encoder eliminates the need to trim the S2603 decoder oscillator.

The S2602 Encoder typically generates a 40kHz carrier which it amplitude-modulates with a base-band message of 12 bits, each bit preceded by a synchronizing marker pulse.

Bits 1 and 12 denote sync and end-of-message, respectively, bits 2 through 6 are place-holder bits, and bits 7 through 11 contain the command data. The S2603 Decoder produces an output only after two complete, consecutive, identical transmissions. Marker pulses and redundant transmissions have given the S2602/S2603 system a very high immunity to noise, without a large number of discrete components.

S2602 Encoder

The S2602 is a CMOS device with an on-chip oscillator, 3 keyboard inputs, a keyboard encoder, a shift register, and some control logic. The oscillator uses an external ceramic resonator, and to conserve power, runs only during transmission. Keyboard inputs are active-low, and have internal pull-up resistors to V_{DD}. When one keyboard input from the group C through E is activated with one from the group F through K, the keyboard encoder generates a 5-bit code, as given in the table entitled "S2602/S2603 CODING," below. This code is loaded into a shift register in parallel with the sync and end bits to form the message.

The transmitter output is a 40kHz square wave of 50% duty factor which has been pulse-code-modulated by (i.e., ANDed with) a signal having a recurring pattern, a bit frame of 3.2 millisecond duration. This bit frame is comprised of three signals: the Start signal which is 0.4 milliseconds of logic "1"; followed by the Data signal which is 1.2 milliseconds of the lowest-order shift register bit; followed by the Mark signal which is 1.6 milliseconds of logic "0" (except in the first bit frame where Mark = 1 to facilitate receiver synchronization).

The shift register is clocked once per bit frame, so that its 12-bit message is transmitted once in 38.4 milliseconds. The minimum number of transmissions that can occur is two, but if the keyboard inputs are active after the first 3.6 milliseconds of any 12-bit transmission, one more 12-bit transmission will result. Transmissions are always complete, never truncated, regardless of the keyboard inputs.

The S2602 Encoder is silenced automatically by an on-chip duration limiter if a transmission releases for 6½ seconds (FOSC = 320kHz). The absence of a keyboard closure will reset the duration limiter so that a new 6½ second internal starts with the next key closure.

S2603 Decoder

The S2603 is a PMOS LSI device with an on-chip oscillator, five keyboard inputs, a 40kHz signal input, and 8 outputs. The oscillator requires only an external R and C. The five keyboard inputs are active-low with internal pull-up resistors to V_{SS}; activation of any two causes one of 10 possible 5-bit codes to be generated and fed to the outputs of the S2603, overriding any 40kHz signal input.

Two counters, the signal counter and the local counter, are clocked respectively by the signal input and a 40kHz signal from the local RC oscillator timing chain. A 40kHz input lasting 3.2 milliseconds (i.e., an initial bit frame) causes the signal counter to overrun and reset both itself and the local counter. At specific intervals thereafter, the local counter generates pulses used to interrogate the contents of the signal counter. Resynchronization of the counters occurs every bit frame so that the interrogation yields valid data bits even if the transmitter oscillator frequency has deviated up to ±24% with respect to the receiver oscillator frequency.

The decoded place-holder bits from the next five-bit frames following the initial synchronizing frame are not used. However, the next five decoded bits, the command bits, are converted to a parallel format and are compared against the command bits saved from the prior transmission. If they match, the command bits are gated to the receiver outputs. However, a mismatch causes the receiver outputs to be immediately disabled, and the new command bits are saved for comparison against the command bits from the next transmission. In the case where 2 identical, proper transmissions are immediately followed by nothing, the receiver outputs will be activated during the end-frame of the second transmission, and will be disabled 45 milliseconds thereafter. In the rest (disabled) state the five Binary Outputs are at a "1" logic level; when not in the rest state, one or more of the open-sourced output transistors will conduct to V_{DD}. The Data Valid output is low during the rest state, and high whenever data is present at the Binary Outputs.

The S2603 has two other outputs: On/Off and Analog. The states of these outputs are controlled by the 10 particular Binary Output codes which the receiver Keyboard

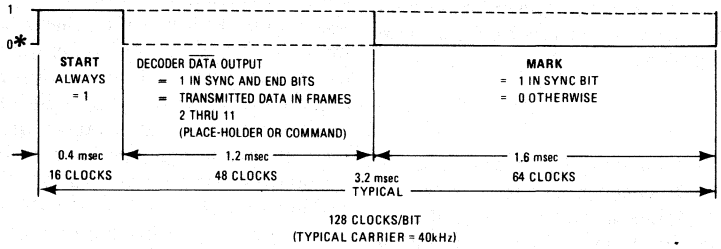
Inputs can cause to be generated.

The On/Off ("mains") output changes state each time 01100 appears at the Binary Outputs. In TV applications the On/Off output is most often used to kill and restore the main power supply.

The Analog Output is a 10kHz pulse train whose duty factor is digitally controllable. With a simple low-pass filter, this output can provide 64 distinct DC levels suitable for control of volume, color saturation, brightness, motor speed, etc. The Analog Output increases its duty factor in response to a particular Binary Output code and decreases its duty factor in response to another code. The Analog Output is set to 50% duty factor whenever 01111 appears at the Binary Outputs. The Analog Output is mutable; 00001 sets it to 0% duty factor. If 00001 then disappears and reappears, the original duty factor is restored. This of course implements the TV "sound killer" feature.

The S2603 has an on-chip power-on reset (POR) circuit which sets the Pulse Train and On/Off Output to "0", sets the Analog Output at 50% duty factor, and insures that the Analog Output is muted. No external components are required to implement POR, but a POR input has been provided for applications where externally controlled reset is desirable, e.g., where the power supply voltage rise time is extremely slow. The POR input has an internal resistor pull-up to V_{SS}; pulling it low causes a reset.

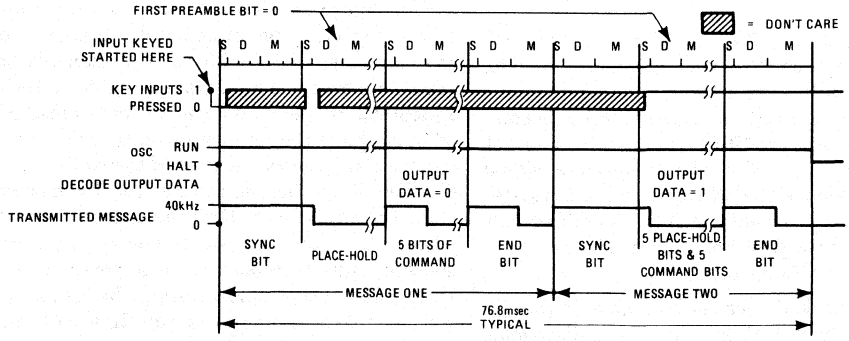
Message Bit Format



* "1" MEANS PRESENCE OF A 40kHz CARRIER (SQUARE WAVE); "0" MEANS ABSENCE OF A 40kHz CARRIER (SQUARE WAVE).

IF MESSAGE BIT = "1" THEN DECODER DATA OUTPUT = ENCODER DATA INPUT = "0";
IF MESSAGE BIT = "0" THEN DECODER DATA OUTPUT = ENCODER DATA INPUT = "1".

Message Format



ENCODER/DECODER REMOTE CONTROL 2-CHIP SET

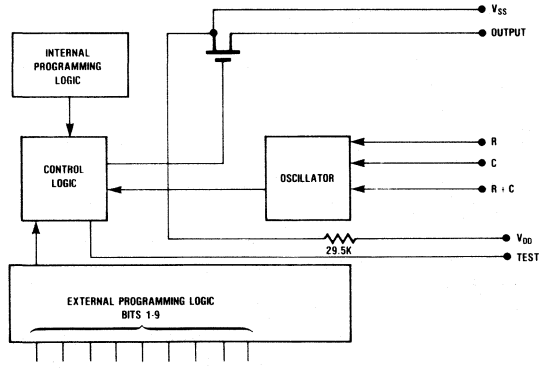
Features

- ☐ **RC Oscillator Used — No Crystal Required**
- ☐ **Phase Locked Loop on Decoder for Reliable Operation**
- ☐ **512 User Selectable Address Codes**
- ☐ **Encoder Operates on a Single Rail 9 Volt Supply — Suitable for Inexpensive and Convenient Battery Operation**
- ☐ **User Can Determine the Type of Transmission Medium to Use**

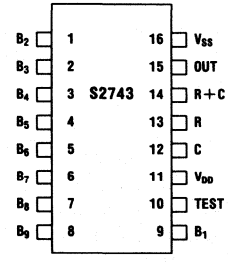
Applications

- ☐ **Entry Access Systems**
- ☐ **Remote Engine Starting for Vehicles and Standby Generators**
- ☐ **Security Systems**
- ☐ **Traffic Control**
- ☐ **Paging Systems**
- ☐ **Remote Control of Domestic Appliances**

Block Diagram 2743 Encoder

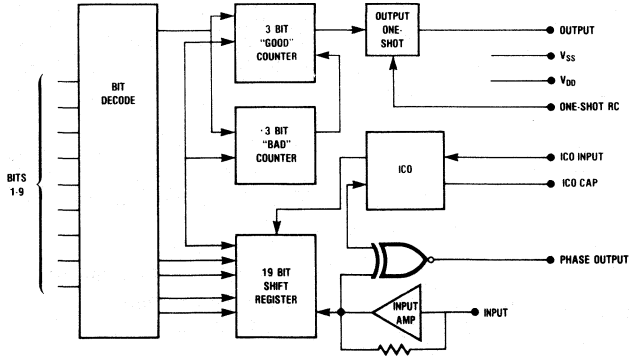


Pin Configuration 2743

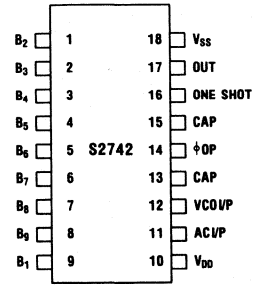


TOP VIEW

Block Diagram of 2742 Decoder



Pin Configuration 2742



TOP VIEW

General Description — Encoder/Decoder

This two-chip PMOS set includes a user-programmable serial data encoder for use in a simple low-power transmitter and a serial data decoder for use in a user addressable receiver. The user can select the transmission medium (RF, infrared ultrasonic, or hardwire). The externally selectable message allows up to 512 codes or addresses; this is done with the nine binary inputs on each device. An additional 3 bits of address can be programmed on chip as a fixed preamble.

The serial data encoder encodes by means of a frequency-shift-keyed trinary data pattern composed of 16 data bits. Each data bit will have a length equivalent to 32 cycles of high frequency clock (20kHz typical). Each trinary data pattern will be 512 cycles of 1/2 the oscillator frequency length. The encoder frequency oscillator reference is controlled with an external RC network. The encoder transmitter can be powered by a single 9 volt battery so that a single momentary push button will activate the encoder and transmitter. In the off position there is no current flow.

The serial data decoder in conjunction with a receiver amplifier decodes the transmitted 16-bit coded signal. The on-chip phase-locked-loop locks in on the 20kHz signal even if the transmitted frequency differs from the receiver by up to ± 15%. The coded signal input is compared with the externally selected code. The serial decoder looks at the transmitted signal a minimum of three times before validating a good message. A 3-bit "good" code counter or a 3-bit "bad" code counter accumulates the number of successive good and bad codes being received.

The decoder has an on-chip one-shot which is user programmed by an external RC combination. Whenever three complete good codes are received in the "good" counter a signal enables the one-shot which controls the signal valid output. If a series of three sequencial bad codes enter the "bad" code counter the "bad" counter resets the "good" code counter and one-shot period and will not allow an active output until the end of the one-shot period. Any "good" code resets the "bad" code counter. If the "good" counter has accumulated three good codes and activated the output one-shot, any occasional "good" code (occurring within the one-shot period) will maintain the output by retriggering the one-shot. The output appears like a single switch, on when "good" codes are received, off when not, with the minimum total period being determined by twice the one-shot period. The one-shot can be used to prevent the output from switching on and off too rapidly due to system noise. The typical RC components shown in the block diagram give a period of about one second.

Functional Description — Serial Data Encoder

The AMI serial data encoder is comprised of three sections: Oscillator, Programming Logic, and Control Logic. Specifically it will provide logical ones "1", logical zeroes "0", and synchronization pulses "S" and arrange them into a trinary data pattern composed of 16 data bits. Each data bit will be 32 cycles of the high frequency (HF-1/2 Oscillator Frequency) in length. Each trinary data pattern will be 512 cycles of 1/2 the Oscillator Frequency length.

A logical "1" is represented by 32 cycles of the high frequency.

A logical "0" is represented by 16 cycles of the high frequency followed directly by 8 cycles of the low frequency (LF = 1/2 HF).

A synchronization pulse "S" is represented by 16 cycles of the low frequency.

A 16-bit data pattern will be encoded in the device in such a manner as to have three (3) bits programmed internally and nine (9) bits programmed externally.

The Oscillator Frequency equals twice that of the High Frequency, and the High Frequency equals twice that of the Low Frequency.

The Oscillator circuit will require a maximum of three (3) external components (refer to Figure 2).

External programming inputs connected to the device $-V_{DD}$ supply will be considered as a logical "1." The bit programming current will not exceed 50μA. The programming resistance should not exceed 1kΩ. Unconnected external bit programming inputs will be considered at a logical "0."

A "1" ($-5V \leq$ "1" $\leq V_{DD}$) presented to the "Test" input sets the Internal counter and maintains the output of the device "On." The input impedance of the test input is greater than 5MΩ.

For portable operation a 9V transistor battery can be used for the DC voltage supply. Proper circuit polarity must be observed ($-V_{DD}$, $+V_{SS}$).

S2743 Absolute Maximum Ratings

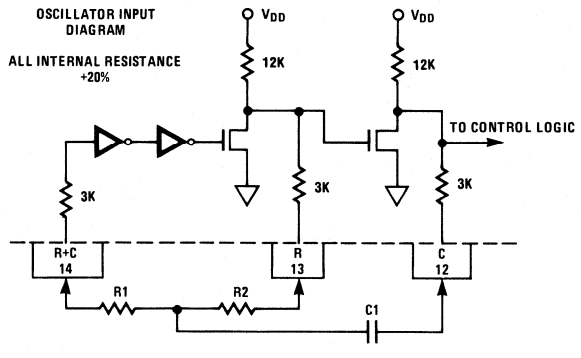
DC Supply Voltage	−15V
Input Voltage	V_{SS}+.3V to V_{SS} −15V
Operating Temperature Range	−40°C to +100°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (During Soldering)	300°C for Max. 10 sec.

S2743 Electrical Characteristics (25°C Air Temperature Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
	Operating Supply Voltage	−6.65	−9.5	−15	V	V_{DD}; V_{SS}=0V
	Operating Power Dissipation		27	40	MW	−8V, −5mA, Max
	Operating Frequency	2	40	60	kHz	Oscillator
	Programming Bits 1-9, Current			50	μA	Programming Input, R 1kΩ
	External Programming Resistance			1	kΩ	Bits 1-9
	(DC Bits 1-9) Program Logical "1"	V_{SS}−5V		V_{DD}	V	
	Input Levels Logical "0"	V_{SS}−1V		V_{SS}	V	
	Bits 1-9 Current		55		μA	Input R 9V>1.5M @ 5V
	Test and R+C Input Impedance	5		75	MΩ	
	(DC) Test Input Levels Test ON	V_{SS}−5V		V_{DD}	V	Maintains Output Device ON
	Test OFF (See Note 1)	V_{SS}−1V		V_{SS}	V	Permits Normal Operation
	R, C Resistance Logical "1"		12		kΩ	Resistance to V_{DD}, ±20%
	R,C Resistance Logical "0" (See Figure 1)		3		kΩ	Resistance to V_{SS} +20%−30%
	Output Current (See Note 2)	5			mA	Output Voltage=.8V W/V_{DD}=−7V

Notes: 1. Effect noted at Pin 15 to V_{SS}. 2. Output Voltage Pin 15 to V_{SS}. 3. All Voltages measured with respect to V_{SS}.

Figure 1. Serial Data Encoder



AMERICAN MICROSYSTEMS, INC.

S2709

VACUUM FLUORESCENT DIGITAL CLOCK FOR AUTOMOTIVE APPLICATIONS

Features

- ☐ Uses Inxpensive 4MHz Crystal
- ☐ Direct Drive to Green or Blue Vacuum Fluorescent Display
- ☐ Low Standby Power Dissipation When Display is Switched Off With Ignition
- ☐ Variable Brightness Tracks Other Dash Lights

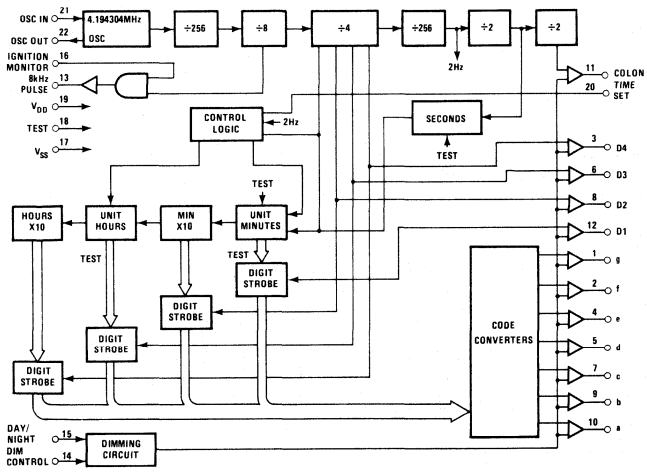
Applications

- ☐ In Dash Automobile Clocks
- ☐ Tape Players, CB Radio Units
- ☐ Automotive After Market Clocks
- ☐ Aircraft, Marine Panel Clocks
- ☐ Portable Instrumentation Clocks

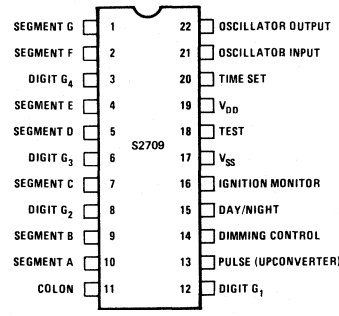
Functional Description

The S2709 vacuum fluorescent clock is a monolithic MOS integrated circuit utilizing P-Channel low threshold, enhancement mode and ion-implanted depletion mode devices. The circuit interfaces directly with 4 digit multiplexed vacuum fluorescent displays and requires only a single nominal 12V power supply. The timekeeping function operates from a 4MHz crystal controlled input. The display format is 12 hours with colon and leading zero blanking. An up-converter output is provided by the circuit to generate increased display driving voltage. A brightness control input allows variation of the display intensity. An ignition monitor input controls the upconverter operation and inhibits time setting. The S2709 is normally supplied in a 22-lead plastic dual-in-line package.

Block Diagram



Pin Configuration



Operational Description

Refer to the block diagram and Figure 1, Typical Application.

Oscillator Input (Pin 21) and Output (Pin 22)—The crystal controlled oscillator operates at a frequency of 4.194304 MHz to increase accuracy and reduce external component costs due to the less expensive quartz crystal. The frequency is controlled by a quartz crystal and fixed capacitor upconverter output (pin 13). This method allows accurate frequency tuning of the crystal oscillator without loading down the oscillator circuit. The feedback and phase shift resistors are integrated to further reduce external component costs. The internal oscillator inverter drives a counter chain that performs the timekeeping function.

Time Setting Input (Pin 20)—To prevent tampering, time setting is inhibited until the ignition monitor (pin 16) is held at a logic high level (V_{SS}).

Normal timekeeping is provided by allowing the time set pin to float externally. (Unloaded, this pin will alternate between V_{DD} and V_{SS} in phase with the unit minutes digit strobe [pin 12] during normal timekeeping.) If the time set pin is held at a logic high level (V_{SS}) the minutes counter advances at a 2Hz rate without carry to hours. If the time set pin is held at a logic low level (V_{DD}) the hours counter advances at a 2Hz rate.

It is possible to reset the hours, minutes and internal seconds counter by applying a logic low level (V_{DD}) to the test input (pin 18) during the time that the ignition monitor input is at a logic low level (V_{SS}). This reset state (time 1:00) is used for testing purposes.

Upconverter Pulse Output (Pin 13)—The clock circuit and vacuum fluorescent display drive normally operate at 25V when the ignition monitor pin is held at a logic high level (V_{SS}). The automobile battery voltage (12V) is doubled by an external upconverter circuit triggered by an 8kHz output pulse having a 28% duty cycle. The voltage, whether 12V or 25V, is applied to the circuit via the V_{SS} input (pin 17).

When the ignition monitor pin is held at a logic low level (V_{DD}) the upconverter is disabled. This drops the V_{SS} supply to 12V allowing the clock to operate while the display drive is decreased, lowering power dissipation. At the battery voltage drops (due to engine starting, cold temperature, or aging) timekeeping is maintained down to approximately 7V with no loss of the memory down to 5V. However, below 9V the upconverter will not be inhibited by the ignition monitor input.

Note that low standby power dissipation (60mW typical @V_{SS}=12V, and no output loads) is accomplished by turning off the filament voltage to the display when the auto ignition switch is off.

Ignition Monitor (Pin 16)—Along with preventing the already mentioned time setting function, the ignition monitor when held at a logic low level (V_{DD}) inhibits the 8kHz upconverter output pulse (pin 13) as long as the supply (V_{SS}) is above 9V. This pin is normally connected to the auto accessory switch.

The ignition monitor input can be protected against power supply transients by using 47KΩ external series resistance (see Figure 1).

Day/Night Display Control Input (Pin 15)—As seen in Figure 2, the display brightness is controlled via both pin 15 and the dimming control input (pin 14). The day/night input is connected to the automobile parking or headlights switch such that when these lights are off (V_{IN} low) the decoded segment and the digit outputs are from V_{SS} to $V_{SS}-2.0$ volts. When the parking or headlights are switched on (V_{IN} high) the internal day/night logic enables the dimming input to control the segment and digit output voltage and brightness by allowing adjustable current to flow as controlled by the dash lights rheostat.

The day/night input can be protected from power supply transients by using 47KΩ external series resistance (See Figure 1).

Display Dimming Control Input (Pin 14)—The display dimming input is connected to the automobile dashboard light dimming rheostat through a series resistor. This allows the fluorescent display to track the dimming characteristics of the incandescent dashboard light (see Figure 2). The display dimming control is inhibited unless the day/night input (pin 15) is held at a logic high level (V_{SS}).

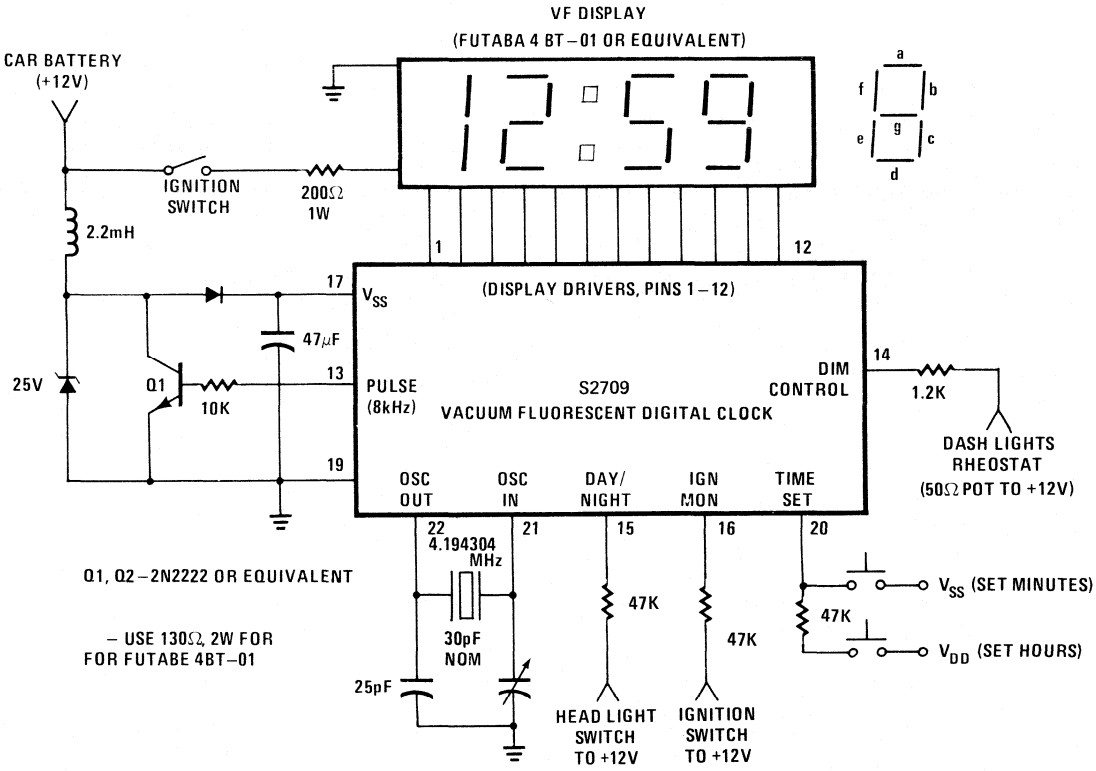
Display Drivers (Pins 1 through 12)—The 12 hour display format is comprised of four digits with leading zero blanking and a flashing colon. Each digit contains 7 segments with individual segments coded in the conventional manner (see Figure 1). The display is multiplexed with each digit output (G1, G2, G3 and G4) being strobed for a time period of approximately 0.5mS. Figure 3 shows the minimum output current as a function of output voltage for the digit (grid) and segment outputs.

The colon output (pin 11) is designed to have an unobtrusive flash while still indicating that the clock is functioning normally. The colon flash is accomplished in a 2 second period of 1-1/2 seconds on the 1/2 second off.

Electrical Characteristics

Symbol	Characteristics/Conditions	V_{DD} V	0°C to 70°C			Unit
			Min.	Typ.	Max.	
V_{SS}	Operating Supply Range V_{DD} = 0.0V (Refer to Upconverter Pulse Output)		7.0		28	V
I_{SS}	Supply Current (No loads on Outputs)	12 25			12 15	mA mA
	Oscillator Frequency			4.194304		MHz
	Display Outputs					
	Multiplex Rate			512		Hz
	Duty Cycle (Each Digit Per Cycle)			18.8		%
	Output Current (Day/Night = LOW)					
I_{OH}	Digits, V_{OH} = 24V	25			−6.0	mA
I_{OL}	V_{OL} = 2V	25	40			μA
I_{OH}	Segments & Colon, V_{OH} = 24V	25			−1.5	mA
I_{OL}	V_{OL} = 2V	25	10			μA
	Output Voltage (V[Pin 14] − V(Digit or Seg)					
	Day/Night = High, V(Pin 14 ≥ /4V)					
ΔV_O	Digits (R_L = 8.2KΩ to V_{DD})	25			1	V
ΔV_O	Segment (R_L = 100KΩ to V_{DD})	25			1	V
	Upconverter Pulse Output					
	Pulse Frequency			8192		Hz
	Duty Cycle			25		%
	Output Current					
I_{OH}	V_{OH} = 7V	9			−1.5	mA
I_{OH}	V_{OH} = 23V	25			−3.0	mA
I_{OL}	V_{OL} = 1V	25	6.0			μA
	Time Set Input/Output					
	Input Voltage (No Load)					
V_{IH}	High	25	24		1	V
V_{IL}	Low	25	0		1	V
	Output Current					
I_{OH}	V_{OH} = 18V	25	−6.0		−2.0	mA
	Output Frequency			512		Hz
	Duty Cycle			25		%
	Ignition Monitor Input and Day/Night Input					
	Input Voltage					
V_{IH}	High	9.0 to 25	6.5		V_{SS}	V
V_{IL}	Low	9.0 to 25	0		2.0	V
I_{IH}	Input Current (Pull Down) V_{IH} = 12V	25	2		20	μA

Figure 1. Typical Application



AUTO CLOCK

Features

- ☐ **12 Hour, 4 Digit Auto Clock.**
- ☐ **Elapsed Time Counter (resettable, range to 99 hours).**
- ☐ **Calendar (4-year calendar with pin option for European date/month reversal).**
- ☐ **Ignition-Sensing Display Cut-off (to reduce battery drain when the auto is not operating).**
- ☐ **Crystal Input Accuracy (uses inexpensive 4.194 mHz crystal).**
- ☐ **Direct Display Drive (4-digit vacuum fluorescent displays, 24 Volts).**

Applications/Markets

- ☐ Automotive
- ☐ Avionics
- ☐ Marine
- ☐ Portable Clocks
- ☐ Industrial

General Description

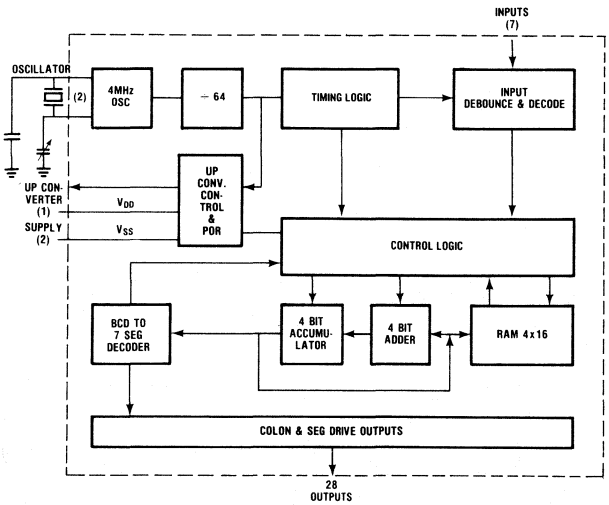
The S4003 Auto Clock is a PMOS integrated circuit which has found wide application in auto, avionic and marine applications as a portable or dashboard clock and as an industrial timer.

A functional description of the inputs/outputs and registers follows:

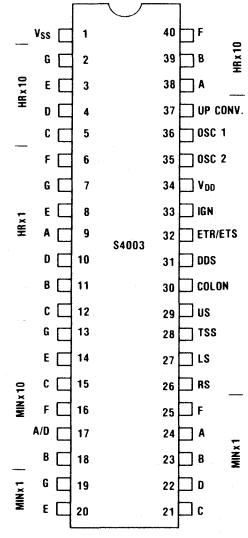
1. **Set Inputs**—Left digits set and right digits set will index the selected register at a 2Hz rate. Indexing either input will not upset the unselected digits.

2. **Time Set Select**—Enables set inputs to the timekeeping register. When updating hours, the minutes display will blank out and MX1 digit will display A or P. Minutes will update in a normal manner and reset seconds to zero. Seconds will restart on release of the time set select line. When deselected, the time will continue to be displayed for 5 seconds ±1 seconds. AM and PM indications will switch on the transfer from 11:59 to 12:00.

Block Diagram



Pin Configuration



AMERICAN MICROSYSTEMS, INC.

S2809

UNIVERSAL DISPLAY DRIVER

CONSUMER

Features

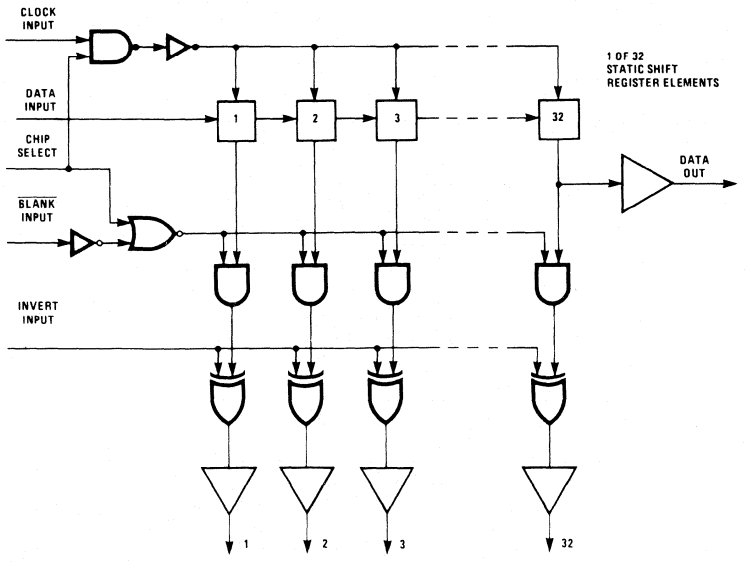
- ☐ 32 Bit Data Storage Register
- ☐ Drives LED, LCD, or Vacuum Fluorescent Displays
- ☐ 32 Output Buffers
- ☐ Drives up to 4 Digits
- ☐ Expansion Capability for More Digits
- ☐ Reduced RFI Emanation
- ☐ Wired OR Capability for Higher Current

General Description

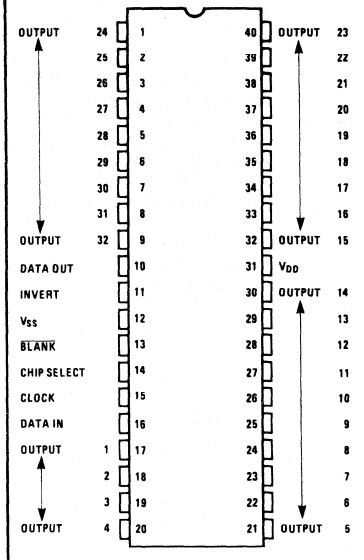
The S2809 Universal Display Driver is a P-channel MOS integrated circuits capable of driving LED, vacuum fluorescent, and liquid crystal displays. Data is clocked serially into a 32-bit master-slave static shift register. This provides static parallel drive to the display segments through display drive buffers. To reduce RFI emanation, capacitors have been integrated on the circuit for reduction of output switching speeds. Serial interconnection of circuits is made possible by the Data Out Output, allowing additional digits to be driven.

Two or more outputs may be wired together for higher sourcing currents; useful in applications such as triac triggering or low voltage incandescent displays. The S2809 can also be used as a parallel output device for μC's such as AMI's S2000 series single chip microcomputer.

Block Diagram



Pin Configuration



Absolute Maximum Ratings

Operating Ambient Temperature T_A	10°C to +70°C
Storage Temperature	−65°C to +150°C
V_{SS} Supply Voltage	+25V
Positive Voltage on Any Pin	V_{SS} +0.3V

Electrical Characteristics (V_{DD} = 0V, 8V V_{SS} 22V, T_A = 10°C to +70°C unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{IH}	Logic 1 Level (Data, Clock, Invert, Chip Select Inputs)	V_{SS} −0.7		V_{SS} +0.3	V	
V_{IL}	Logic 0 Level (Data, Clock Invert, Chip Select Inputs)	V_{DD}		V_{SS} −7	V	
V_{BH}	Logic 1 Level ($\overline{\text{Blank}}$ Input)	V_{SS} −4.0		V_{SS} +0.3	V	
V_{BL}	Logic 0 Level ($\overline{\text{Blank}}$ Input)	V_{DD}		V_{SS} −7	V	
I_B	Current Sinked or Sourced by $\overline{\text{Blank}}$ Input			1.0	μA	Voltage applied to $\overline{\text{Blank}}$ Input between V_{DD} & V
C_B	Capacitance of $\overline{\text{Blank}}$ Input			12	pF	
I_{OH}	Output Source Current	9.0			mA	$V_{OUT} = V_{SS}$ −3
I_{OH}	Output Source Current	4.0			mA	$V_{OUT} = V_{SS}$ −1.5
I_{OH}	Output Source Current	1.0			mA	$V_{OUT} = V_{SS}$ −0.2
I_{OS}	Sink Current Output Load Device			50	μA	Output voltage = V_{SS}
I_{OS}	Sink Current Output Load Device	10			μA	Output voltage = V_{DD} +3V
I_L	Output Leakage Current (Output Off)			10.0	μA	
I_{DD}	Supply Current			3.0	mA	Not including output source and sink current
I_{OM}	Maximum Total Output Loading			300	mA	All outputs on
f_c	Clock Frequency	DC		100K	Hz	
t_{ON}	Clock Input Logic 1 Level Duration	3.0			μs	
t_{OFF}	Clock Input Logic 0 Level Duration	6.5			μs	
t_{ro}, t_{fo}	Display Output Current Rise and Fall Times	10		150	μs	*Measured between 10% and 90% of output current V_{SS} +11V, I_{OH} = 9ma

* NOTE: With supply voltages higher than 11 volts, delay exists before an output rise or fall. This delay will not exceed 100μs with a 22 volt supply.

Functional Description

The 32-bit static shift register stores data to be used for driving 32 output buffers, which may be used to drive display segments or other circuitry. Data is clocked serially into the register by the signal applied to the Clock Input whenever a logic 1 level is applied to the Chip Select Input; during this time, outputs are not driven by the shift register but will go to the logic level of the invert input. With a logic 0 level applied to the Chip Select Input, the 32 outputs are driven in parallel by the 32-bit register. It is possible to connect S2809 circuits in series to drive additional displays by use of the Data Output.

Clock Input

The Clock Input is used to clock data serially into the 32-bit shift register. The signal at the Clock Input may be continuous, since the shift register is clocked only when a logic 1 level is applied to the Chip Select Input. As indicated in Table 1, data is transferred from QN-1 to QN on the negative transition of the Clock Input.

Data Input

Whenever a logic 1 level is applied to the Chip Select Input, data present at the Data Input is clocked into the 32-bit master-slave shift register. Data present at the input to the register is clocked into the master element during the logic 1 clock level and thus must be valid for the duration of the positive clock pulsewidth. This information is transferred to the slave section of each register bit during the clock logic 0 level.

Chip Select

The Chip Select Input is used to enable clocking of the shift register. When a logic 1 level is applied to this input, the register is clocked as described above. During this time, the output buffers are not driven by the register outputs, but will be driven to the logic level present at the Invert Input. With a logic 0 level at the Chip Select Input, clocking of the register is disabled, and the output buffers are driven by the 32 shift register elements.

Blank Input

This input may be used to control display intensity by varying the output duty cycles. With a logic 0 level at the Blank Input, all outputs will turn off (i.e., outputs will go the the logic level of the Invert Input). With a logic 1 level at the Blank Input, outputs are again driven in parallel by the 32 shift register elements (assuming the Chip Select Input is at logic 0).

The Blank Input has been designed with a high threshold to allow the use of a simple RC time constant to control the display intensity. This has been shown in Figure 1.

Invert Input

The Invert Input is used to invert the state of the outputs, if required. With a logic 0 level on this input, the logic level of the outputs is the same as the data clocked into the 32-bit shift register. A logic 1 level on the Invert Input causes all outputs to invert.

This input may also be used when driving liquid crystal displays, as shown in Figure 5.

Data Output

The Data Out signal is a buffered output driven by element 32 of the shift register. It is of the same polarity as this last register bit and may be used to drive the Data Input of another S2809. In this manner, S2809 circuits may be cascaded to drive additional display digits.

Table 1. Logic Truth Table

DATA IN	CLOCK	CHIP SELECT	$\overline{\text{BLANK}}$	INVERT	Q1	QN	DRIVER OUTPUT
X	X	0	0	0			0
X	X	0	0	1		NO CHANGE	1
X	X	0	1	0			QN
X	X	0	1	1			$\overline{\text{QN}}$
0	⌐	1	X	0	0	QN−1→QN	0
1	⌐	1	X	0	1	QN−1→QN	0
0	⌐	1	X	1	0	QN−1→QN	1
1	⌐	1	X	1	1	QN−1→QN	1

Figure 1. Typical Display Intensity Control

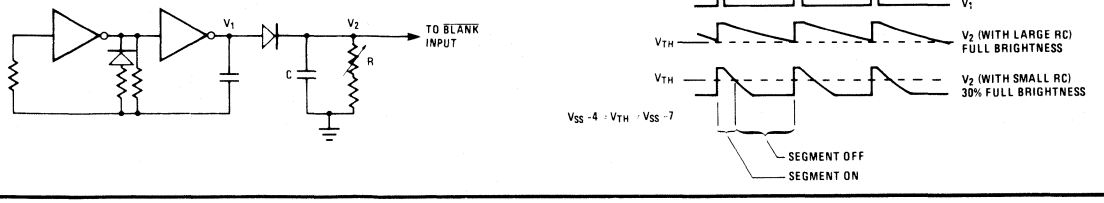


Figure 2. LED Drive — Series

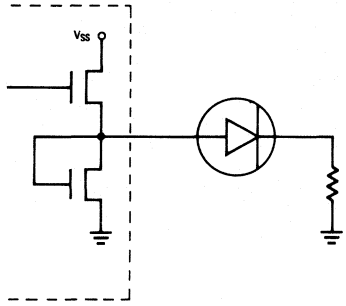


Figure 3. LED Drive — Shunt

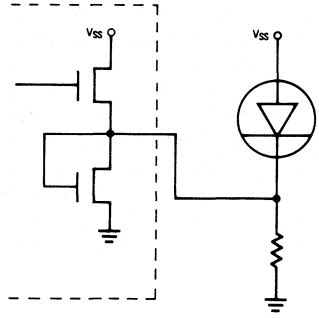


Figure 4. Vacuum Fluorescent Drive

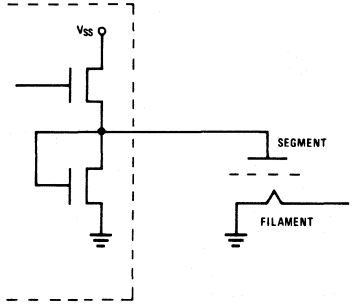


Figure 5. Liquid Crystal Drive

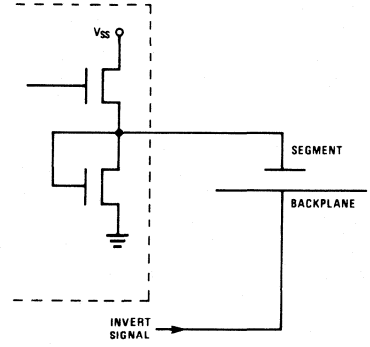
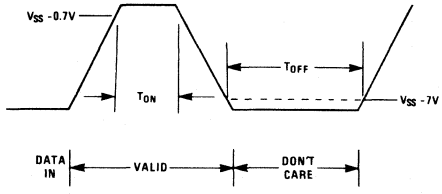
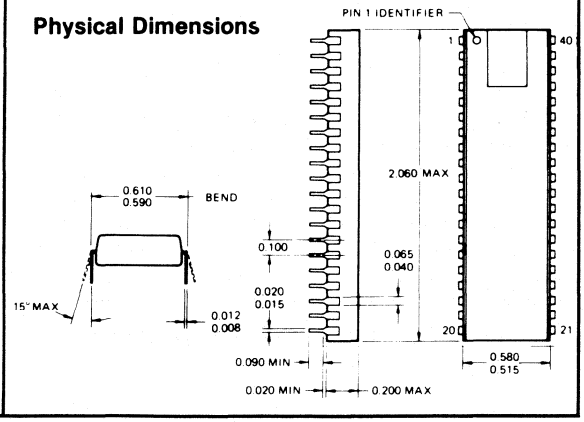


Figure 6. Clock Input Waveform



Physical Dimensions



AMERICAN MICROSYSTEMS, INC.

PRELIMINARY DATA SHEET

S10110

ANALOG SHIFT REGISTER

CONSUMER

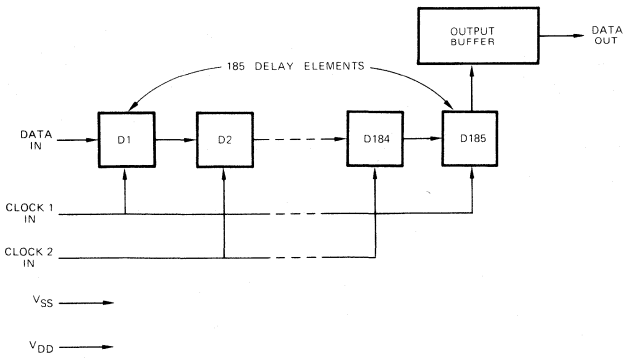
Features

- ☐ 185 Stage "Bucket Brigade" Delay Line
- ☐ Delays Audio Signals
- ☐ Accepts Clock Inputs up to 500 kHz
- ☐ Variable Delay
- ☐ Alternate to TCA 350

General Description

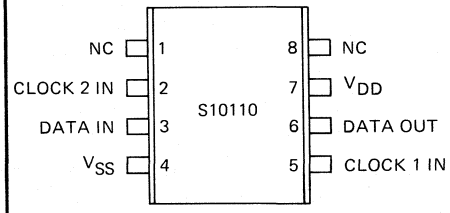
The S10110 analog shift register is a monolithic circuit fabricated with P-channel ion-implanted MOS technology. The part differs from a digital shift register, which is capable of only digital input and output information, in that an audio signal is typically supplied as the data input to the analog register, and the output is the same audio signal delayed in time. The amount of signal delay is dependent on the number of bits of delay (185) and the frequency of the two symmetrical clock inputs. Since each negative-going clock edge transfers data from one stage to the next, the analog signal delay equals 185 ÷ 2 × clock frequency.

Block Diagram



277181

Pin/Package Configuration



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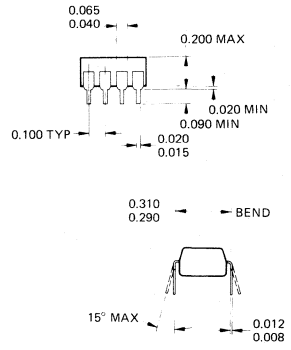


57639

Operation

Device operation may be understood by referring to Figure 1. This is an actual schematic diagram of the analog shift register, or "bucket brigade," showing typical external bias techniques.

Data In Input:

The analog signal, or audio signal, to be delayed is applied to pin 3. This input must be biased to a negative voltage of approximately −8 volts, and two resistors may be used as a voltage divider to provide this bias. They must be chosen so that $(R_1) \pm (R_2) \div (R_1 + R_2)$ is less than 20 KQ. The input signal applied to this input through series capacitor C_{IN} may be as high as 6 volts peak to peak.

Clock 1 and Clock 2 Inputs:

Applied respectively to pins 5 and 2, Clock 1 and Clock 2 are two symmetrical non-overlaping negative-going clocks used to transfer the analog data along the 185 bit delay line. Although these clocks may have a duty cycle as low as 25% (i.e.: each clock signal is at a negative level for 25% of its period), better output signals will be obtained with both clock duty cycles closer to 50%. It is important, however, that no overlap of the clock signals occurs at a level more negative than V_{SS}−0.8 volts.

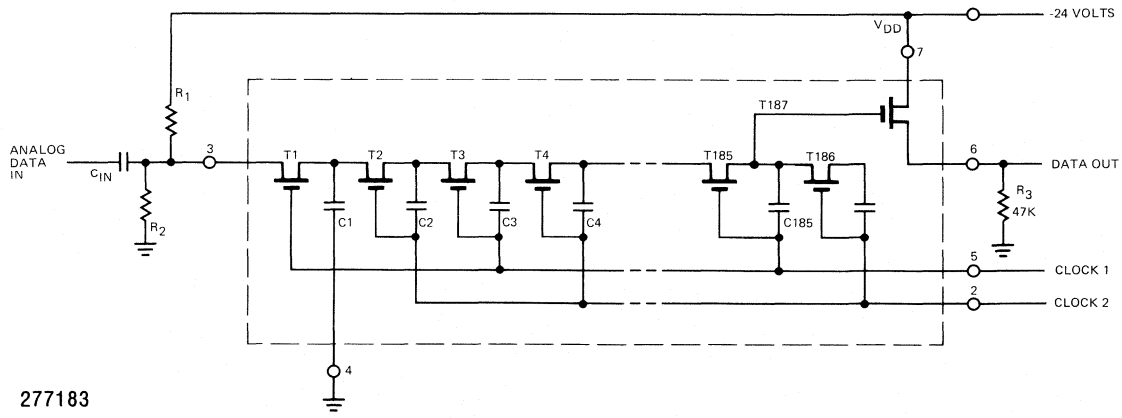
Referring again to Figure 1, it can be seen that when Clock 1 is negative, data is transferred from the data input to capacitor C1; likewise, data is transferred from each even-numbered capacitor to the capacitor to its right. When Clock 2 is negative, data is transferred from C1 to C2 and from each other odd-numbered capacitor to the capacitor to its right. In this manner, data is shifted from the input to C185 after a total of 185 negative clock pulses has occurred (i.e.: 93 periods of Clock 1 and 92 periods of Clock 2).

Data Out Output:

The output of the S10110 analog shift register is a single device, T187, with its drain at V_{DD} and its source connected to pin 6. If a 47K resistor to V_{SS} is supplied at this pin, T187 functions as a source follower.

Referring to Figure 3, it can be seen that the output potential during Clock 2 is a constant value near −10 volts. When Clock 1 switches on (negative), the output instantaneously drops to a level of approximately −30 volts; this is caused by the 20 volt swing of Clock 1 and C185. As Clock 1 remains on, device T185 transfers charge from C184 to C185, and the output voltage becomes more positive, depending on the charge previously stored on C184. It is during this part of Clock 1 that the output reflects the analog data stored on C1 185 bits earlier. Since the clock signal now appears on the output, it is necessary to apply the appropriate filtering to obtain the delayed analog signal.

Figure 1. Schematic Diagram and Pinouts of S10110



AMERICAN MICROSYSTEMS, INC.

S10129

SEVEN STAGE FREQUENCY DIVIDER

Features

- ☐ **Contains Seven Binary Dividers**
- ☐ **Triggers on Negative-Going Edge**
- ☐ **High Impedance Inputs**
- ☐ **Schmidt Trigger on Inputs**
- ☐ **No Minimum Input Rise or Fall Time Requirements**
- ☐ **Low Impedance Push-Pull Outputs**
- ☐ **Low Power Dissipation**
- ☐ **Resettable**

Applications

Electronic organ frequency generator, organ pedal frequency generator, electronic music synthesizers, N stage dividers, low frequency generation, binary counters.

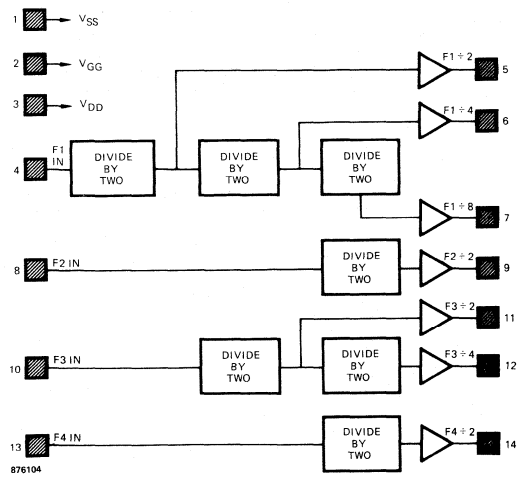
General Description

The S10129 is a monolithic frequency divider circuit fabricated with P-Channel ion-implanted MOS technology. The circuit provides seven stages of binary division in a 3-2-1-1 configuration; the S10129 is ideally suited for tone generation in electronic organs.

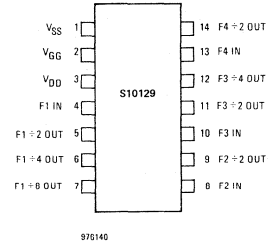
All inputs to the device are buffered to permit easy triggering of the divider stages. Outputs of each divider are buffered to provide low output impedance in both logic states to drive external circuitry as well as other dividers. The buffers have low standby current and are powered by V_{DD}. This voltage functions as a clamp voltage and thus sets the output amplitudes. Buffering the outputs also provides complete isolation between the dividers and the loads. If a buffer output is short-circuited, the divider will continue to function.

All divider outputs may be reset to a logic low level (V_{SS}) by momentarily applying a logic low level to the V_{GG} supply input. This is particularly desirable in some electronic organs in which phase relationships are important.

Block Diagram



Pin Configuration



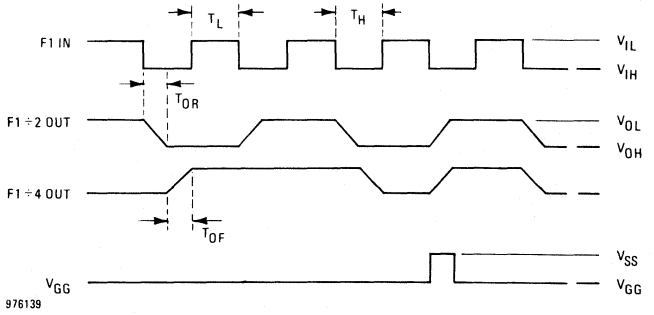
Absolute Maximum Ratings

Voltage on Any Pin Relative to V_{SS} ..... +0.3V to −20V
Voltage on V_{GG} Relative to V_{SS} ..... +0.3V to −30V
Storage Temperature ..... −55°C to +150°C
Operating Temperature (ambient) ..... 0°C to +70°C

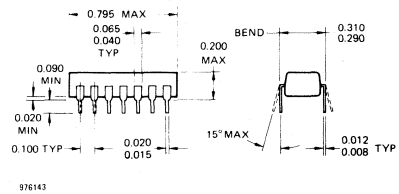
Electrical Characteristics ($0°C \le T_A \le 70°C$; $V_{DD} = -11V$ to $-16V$; $V_{GG} = -25V$ to $-29V$ unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{IL}	Input Clock Low	$V_{SS}+0.3$		$V_{SS}-2.0$	V	
V_{IH}	Input Clock High	$V_{SS}-8$		V_{GG}	V	
f_{IN}	Input Clock Frequency	DC		250	kHz	
T_H, T_L	Input Clock On and Off Times	1.5			μs	
V_R	Voltage Applied to V_{GG} Input to Cause a Reset Condition	V_{SS}		$V_{SS}-0.5$	V	
T_R	Duration of V_R to Cause Reset	10			μs	50% to 50% point
V_{OH}	Output High Level	−11		V_{DD}	V	$V_{DD} = -12V$ $V_{GG} = -26V$ 5.5KΩ load to V_{SS}
V_{OL}	Output Low Level	V_{SS}		−1	V	$V_{DD} = -12V$ $V_{GG} = -26V$ 5.5KΩ load to V_{DD}
C_{IN}	Input Capacitance		5	10	pF	Applies to clock inputs
T_{OR}, T_{OF}	Output Rise and Fall Time		1	2	μs	40pF load applied
I_{GG}	V_{GG} Supply Current		2	3	mA	$V_{DD} = -12V$ $V_{GG} = -26V$ No load
I_{DD}	V_{DD} Supply Current		5	7	mA	$V_{DD} = -12V$ $V_{CC} = -26V$ No load

Timing Characteristics



Physical Dimensions



AMERICAN MICROSYSTEMS, INC.

S10130

SIX STAGE FREQUENCY DIVIDER

CONSUMER

Features

- ☐ **Contains Six Binary Dividers**
- ☐ **Triggers on Negative-Going Edge**
- ☐ **High Impedance Inputs**
- ☐ **Schmidt Trigger on Inputs**
- ☐ **No Minimum Input Rise or Fall Time Requirements**
- ☐ **Low Impedance Push-Pull Outputs**
- ☐ **Low Power Dissipation**
- ☐ **Resettable**

Applications

Electronic organ frequency generator, organ pedal frequency generator, electronic music synthesizers, N stage dividers, low frequency generation, binary counters.

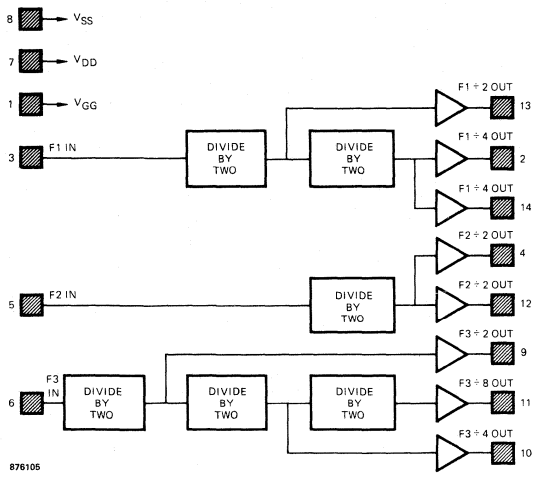
General Description

The S10130 is a monolithic frequency divider circuit fabricated with P-Channel ion-implanted MOS technology. The circuit provides six stages of binary division in a 3-2-1 configuration; the S10130 is ideally suited for tone generation in electronic organs.

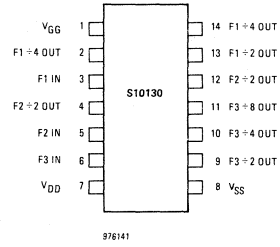
All inputs to the device are buffered to permit easy triggering of the divider stages. Outputs of each divider are buffered to provide low output impedance in both logic states to drive external circuitry as well as other dividers. The buffers have low standby current and are powered by V_{DD}. This voltage functions as a clamp voltage and thus sets the output amplitudes. Buffering the outputs also provides complete isolation between the dividers and the loads. If a buffer output is short-circuited, the divider will continue to function.

All divider outputs may be reset to a logic low level (V_{SS}) by momentarily applying a logic low level to the V_{GG} supply input. This is particularly desirable in some electronic organs in which phase relationships are important.

Block Diagram



Pin Configuration



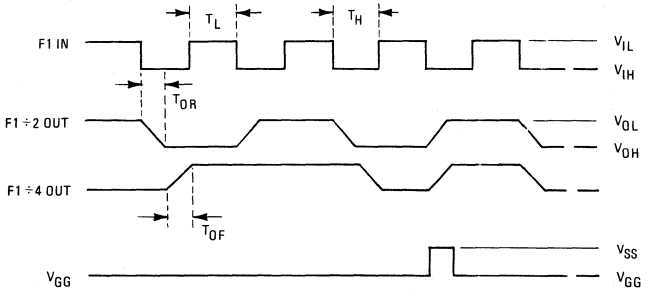
Absolute Maximum Ratings

Voltage on Any Pin Relative to V_{SS} ..... +0.3V to −20V
Voltage on V_{GG} Relative to V_{SS} ..... +0.3V to −30V
Storage Temperature ..... −55°C to +150°C
Operating Temperature (ambient) ..... 0°C to +70°C

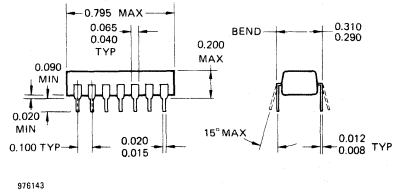
Electrical Characteristics ($0°C \le T_A \le 70°C$; $V_{DD} = -11V$ to $-16V$; $V_{GG} = -25V$ to $-29V$ unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{IL}	Input Clock Low	$V_{SS}+0.3$		$V_{SS}-2.0$	V	
V_{IH}	Input Clock High	$V_{SS}-8$		V_{GG}	V	
f_{IN}	Input Clock Frequency	DC		250	kHz	
T_H, T_L	Input Clock On and Off Times	1.5			μs	
V_R	Voltage Applied to V_{GG} Input to Cause a Reset Condition	V_{SS}		$V_{SS}-0.5$	V	
T_R	Duration of V_R to Cause Reset	10			μs	50% to 50% point
V_{OH}	Output High Level	−11		V_{DD}	V	$V_{DD} = -12V$ $V_{GG} = -26V$ 5.5KΩ load to V_{SS}
V_{OL}	Output Low Level	V_{SS}		−1	V	$V_{DD} = -12V$ $V_{GG} = -26V$ 5.5KΩ load to V_{DD}
C_{IN}	Input Capacitance		5	10	pF	Applies to clock inputs
T_{OR}, T_{OF}	Output Rise and Fall Time		1	2	μs	40pF load applied
I_{GG}	V_{GG} Supply Current		2	3	mA	$V_{DD} = -12V$ $V_{GG} = -26V$ No load
I_{DD}	V_{DD} Supply Current		5	7	mA	$V_{DD} = -12V$ $V_{CC} = -26V$ No load

Timing Characteristics



Physical Dimensions



AMERICAN MICROSYSTEMS, INC.

S10131

SIX STAGE FREQUENCY DIVIDER

CONSUMER

Features

- ☐ **Contains Six Binary Dividers**
- ☐ **Triggers on Negative-Going Edge**
- ☐ **High Impedance Inputs**
- ☐ **Schmidt Trigger on Inputs**
- ☐ **No Minimum Input Rise or Fall Time Requirements**
- ☐ **Low Impedance Push-Pull Outputs**
- ☐ **Low Power Dissipation**
- ☐ **Resettable**

Applications

Electronic organ frequency generator, organ pedal frequency generator, electronic music synthesizers, N stage dividers, low frequency generation, binary counters.

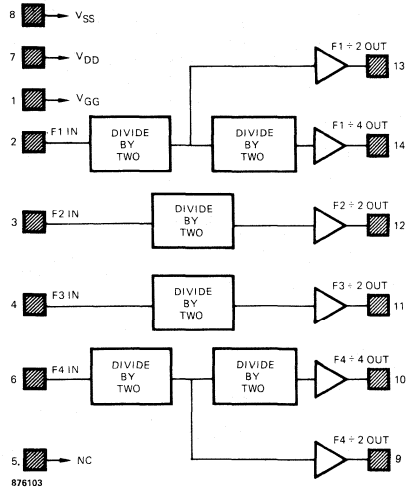
General Description

The S10131 is a monolithic frequency divider circuit fabricated with P-Channel ion-implanted MOS technology. The circuit provides six stages of binary division in a 2-2-1-1 configuration; the S10131 is ideally suited for tone generation in electronic organs.

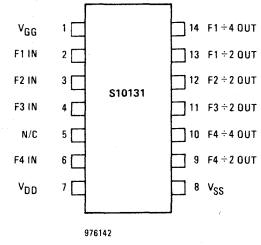
All inputs to the device are buffered to permit easy triggering of the divider stages. Outputs of each divider are buffered to provide low output impedance in both logic states to drive external circuitry as well as other dividers. The buffers have low standby current and are powered by V_{DD}. This voltage functions as a clamp voltage and thus sets the output amplitudes. Buffering the outputs also provides complete isolation between the dividers and the loads. If a buffer output is short-circuited, the divider will continue to function.

All divider outputs may be reset to a logic low level (V_{SS}) by momentarily applying a logic low level to the V_{GG} supply input. This is particularly desirable in some electronic organs in which phase relationships are important.

Block Diagram



Pin Configuration



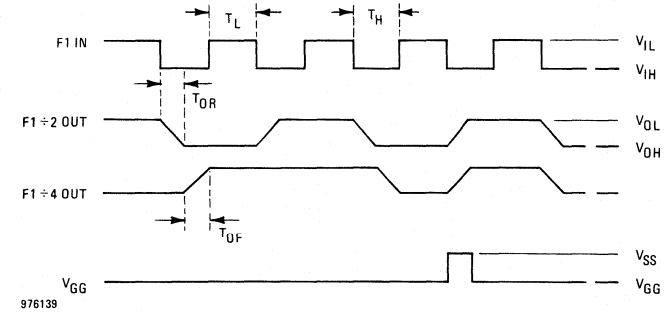
Absolute Maximum Ratings

Voltage on Any Pin Relative to V_{SS} ..... +0.3V to −20V
Voltage on V_{GG} Relative to V_{SS} ..... +0.3V to −30V
Storage Temperature ..... −55°C to +150°C
Operating Temperature (ambient) ..... 0°C to +70°C

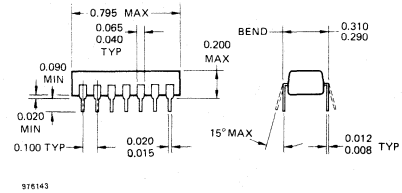
Electrical Characteristics ($0°C \le T_A \le 70°C$; V_{DD} = −11V to −16V; V_{GG} = −25V to −29V unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{IL}	Input Clock Low	$V_{SS}+0.3$		$V_{SS}-2.0$	V	
V_{IH}	Input Clock High	$V_{SS}-8$		V_{GG}	V	
f_{IN}	Input Clock Frequency	DC		250	kHz	
T_H, T_L	Input Clock On and Off Times	1.5			μs	
V_R	Voltage Applied to V_{GG} Input to Cause a Reset Condition	V_{SS}		$V_{SS}-0.5$	V	
T_R	Duration of V_R to Cause Reset	10			μs	50% to 50% point
V_{OH}	Output High Level	−11		V_{DD}	V	V_{DD} = −12V V_{GG} = −26V 5.5KΩ load to V_{SS}
V_{OL}	Output Low Level	V_{SS}		−1	V	V_{DD} = −12V V_{GG} = −26V 5.5KΩ load to V_{DD}
C_{IN}	Input Capacitance		5	10	pF	Applies to clock inputs
T_{OR}, T_{OF}	Output Rise and Fall Time		1	2	μs	40pF load applied
I_{GG}	V_{GG} Supply Current		2	3	mA	V_{DD} = −12V V_{GG} = −26V No load
I_{DD}	V_{DD} Supply Current		5	7	mA	V_{DD} = −12V V_{CC} = −26V No load

Timing Characteristics



Physical Dimensions



S10430

DIVIDER-KEYER

Features

- ☐ 22 Keyboard Inputs
- ☐ 88 DC Keyer Circuits
- ☐ 34 Binary Dividers
- ☐ Provides Four Pitch Outputs
- ☐ All Key Inputs Sustainable for Percussion
- ☐ All Dividers Resettable
- ☐ Provides "Any Key Down" Indication
- ☐ Eliminates Multiple-Contact Key Switches

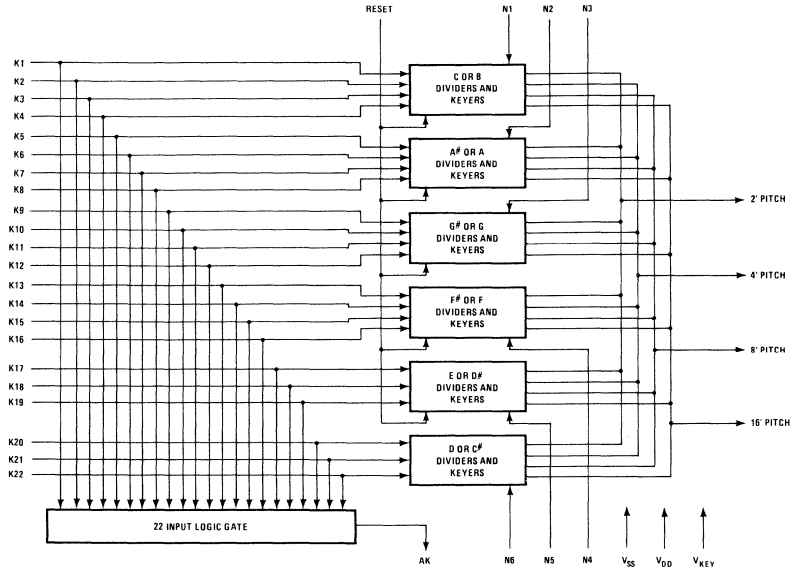
Typical Applications

- ☐ Generation and Keying of Musical Tones
- ☐ Standard Spinet Organ Keying (37 or 44 note keyboards)
- ☐ Keying of Sustained Tones
- ☐ Percussive Effects
- ☐ Generating Stair-stepped Waveforms
- ☐ Electronic Piano

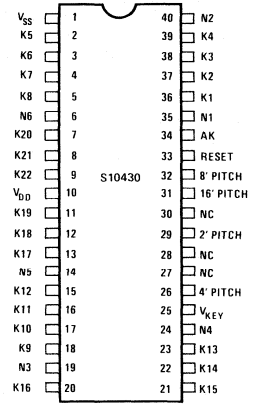
General Description

The S10430 divider-keyer is a monolithic integrated circuit fabricated with P-Channel ion-implanted MOS technology. It is intended for use in spinet organs or other electronic musical instruments having keyboards of up to 44 keys. This device has 22 key inputs, allowing all keying functions for a 44 note manual to be performed by two S10430 circuits. Each S10430 accepts six frequencies from a top octave synthesizer, such as an S50240, and provides squarewave outputs at 16 foot, 8 foot, 4 foot, and 2 foot pitches. For example, if a C key is depressed by itself a low C frequency appears at the 16 foot output, and a C frequency one octave higher appears at the 8 foot output; similarly, the 4 foot and 2 foot outputs provide C frequencies one and two octaves higher, respectively, than the C frequency of the 8 foot output. All appropriate frequency division is performed by the S10430, eliminating the need for external dividers.

Block Diagram



Pin Configuration



General Description (Continued)

The circuit also eliminates the need for multiple-contact key switches and discrete diode or transistor keyers. Because of the high input impedance of the MOS keyers used in this circuit, long sustain envelopes may be obtained by connecting low-value capacitors to the keying inputs.

Absolute Maximum Ratings

Voltage on any pin relative to V_{SS}	+0.3V to -27.0V
Operating temperature (ambient)	0°C to 70°C
Storage temperature	-65°C to 150°C

Electrical Characteristics

$0°C \leq T_A \leq 70°C$; $V_{SS} = 0V$; $V_{DD} = -12.6V$ to $-15.4V$; $V_{KEY} = -4.75V$ to $-5.25V$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{IL}	Logic Low Level TOS and Reset Inputs	0.0		0.8	V	
V_{IH}	Logic High Level TOS and Reset Inputs	-4.2		V_{DD}	V	
t_r, t_f	Rise and Fall Times TOS Inputs			50	μsec	Measured between 10% and 90% points
V_{OL}	Logic Low Level AK Output		-0.5	-1.0	V	100KΩ load to V_{DD}
t_{fo}	Transition of AK Output to 10% of V_{DD}			10	μs	100pF and 100KΩ load to V_{DD}
F_T	Operating Frequency TOS Inputs	DC		50K	Hz	
D_O	Output Duty Factor	48		52	%	Measured between 10% and 90% points
I_{PA}	Peak Output Current Absolute (any pitch output with 1 keyer on)	350		650	μA	$V_{DD} = -14V$ $V_{KEY} = -5V$ $V_{EN} = -25V$ $T_A = 25°C$
I_P	Peak Output Current	85		115	$\%I_{AVE}$*	$V_{DD} = -14V$ $V_{KEY} = -5V$ $V_{EN} = -25V$ $T_A = 25°C$
I_P	Peak Output Current	50		75	$\%I_{AVE}$*	$V_{DD} = -14V$ $V_{KEY} = -5V$ $V_{EN} = -15V$ $T_A = 25°C$

*I_{AVE} is the average of all peak output current values within one circuit.

AMERICAN MICROSYSTEMS, INC.

S2567

RESETTABLE RHYTHM COUNTER

CONSUMER

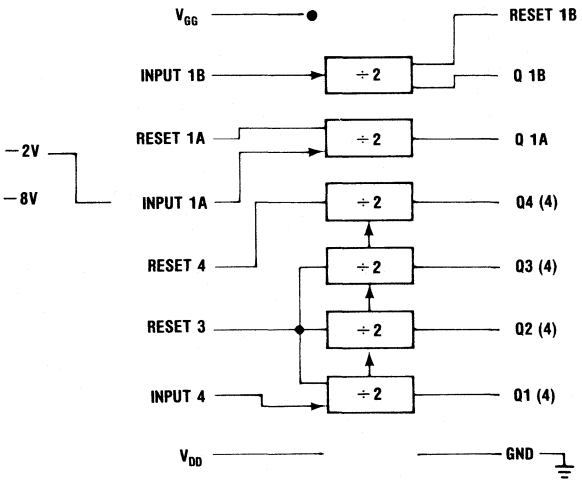
Features

- Pin for Pin Equivalent to GEM 567 and MC1181L
- Organ Rhythm Sections
- Portable Rhythm Sections
- Automatic Rhythm Organs

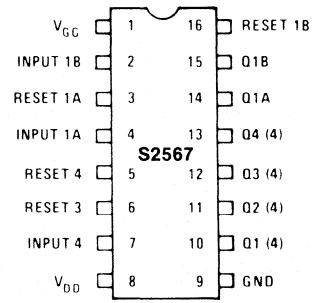
General Description

The S2567 Resettable Rhythm Counter is a six-stage asychronous binary counter designed for driving the count-address inputs of the S2566 Rhythm Generator. The internal partitioning and multiple-reset capability of the S2567 permit simultaneous generation of different meter rhythms. The S2567 Resettable Rhythm Counter is made by P-channel enhancement mode technology and is supplied in a 16-lead dual in-line package.

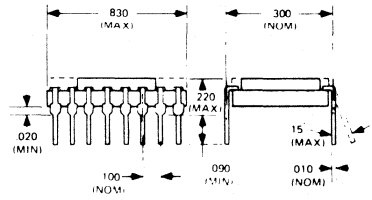
Block Diagram



Pin Configuration



Physical Dimensions



Absolute Maximum Ratings: @25°C, unless otherwise noted
Logic Supply Voltages:

V_{GG}	+0.3V to −33V
V_{DD}	+0.3V to −25V
V_I Trigger Voltage	+0.3V to −18V
P_D Power Dissipation	250mW
T_S Storage Temperature	−55°C to +100°C
T_A Operating Temperature	−0°C to +60°C

Dynamic Characteristics: $T_A = -25°C$
Operating Voltage Ranges:

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{GG}		−25	−27	−29	V
V_{DD}		−14	−15	−16	V
Inputs: (Pins 2 thru 7, and 16)					
f_I	Input Frequency	DC		100	kHz
V_{IH}	Logic "0" Level	+0.3		−2.0	V
V_{IL}	Logic "1" Level	−8.0		−18	V
t_r, t_f	Rise and Fall Times			25	μs
PW_I	Pulse Width	2			μs
I_{IL}	Leakage Current ($V_{ILT} = -18V$)			1	μA
Outputs: (Pins 10 thru 15, each loaded 20K to GND and 20K to V_{DD})					
V_{OH}	Logic "0" Level	0		−1.5	V
V_{OL}	Logic "1" Level	−9.0		V_{DD}	V
Reset Propagation Delay				2.0	μA
Supply Currents: (no output loads)					
I_{GG}			4	6	mA
I_{DD}				20	μA

AMERICAN MICROSYSTEMS, INC.

S2688

DIGITAL NOISE GENERATOR

CONSUMER

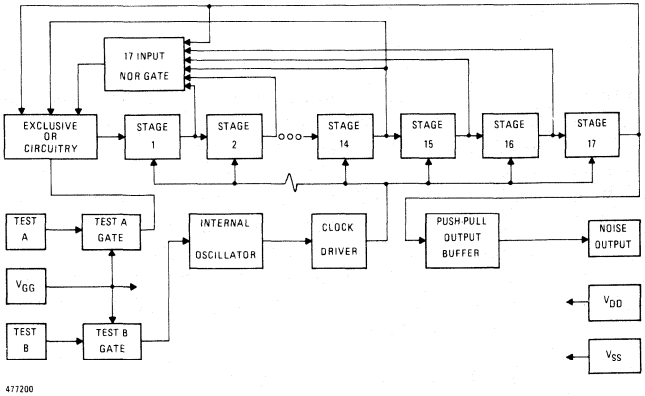
Features

- ☐ Internal Oscillator
- ☐ Consistent Noise Quality
- ☐ Consistent Noise Amplitude
- ☐ Zero State Lockup Prevention
- ☐ Zeros Can Be Externally Forced Into The Register
- ☐ Oscillator Can Be Driven Externally
- ☐ Operates With Single or Dual Power Supplies
- ☐ Eliminates Noise Preamps
- ☐ Alternate to MM5837

General Description

The S2688 noise generator circuit is fabricated in P-Channel ion implanted MOS technology and supplied in an eight-lead dual in-line plastic package. The device contains a 17-bit shift register which is continuously clocked by an internal oscillator. Exclusive OR feedback from the 14th and 17th stages causes the register to generate a pseudo-random noise pattern, and an internal gate is included to prevent the register from reaching an all zero lockup state. To facilitate testing, the device can be easily clocked by an external source.

Block Diagram



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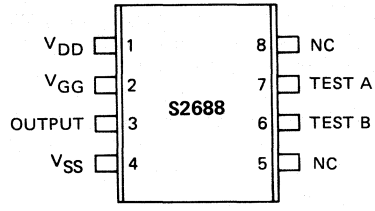
Pin Configuration



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Absolute Maximum Ratings

Positive Voltage on any Pin	V_{SS} +0.3V
Negative Voltage on any pin except V_{GG}	V_{SS} - 28V
Negative Voltage on V_{GG} Supply Pin	V_{SS} - 33V
Storage Temperature	-65°C to +150°C
Operating Ambient Temperature	0°C to +70°C

Electrical Specifications (0°C < T_A < 70°C; V_{SS} = 0 volts; V_{DD} = - 14.0V ± 1.0V; V_{GG} = 27.0V ± 2V; unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{OH}	Output Logic 1 Level	V_{SS} - 1.5		V_{SS}	Volts	20KΩ load to V_{DD}
V_{OL}	Output Logic 0 Level	V_{DD}		V_{DD} +1.5	Volts	20KΩ load to V_{SS}
V_{OL}	Output Logic 0 Level	V_{DD}		V_{DD} +3.5	Volts	20KΩ load to V_{SS} V_{GG} = V_{DD} = - 14V ± 1.0V
Z_{IN}	Input Impedance (Test Inputs)		10		pF	
I_L	Leakage Current (Test Inputs)			500	nA	
f_o	Frequency of Internal Oscillator		100		kHz	
I_{DD}	V_{DD} Supply Current			4.0	mA	No output load
I_{GG}	V_{GG} Supply Current			500	μA	
f_{TEST}	Test Frequency	80		105	kHz	

Operation

The S2688 is a 17-bit digital shift register driven by an internal oscillator circuit. Outputs from the 14th and 17th stages are connected to an Exclusive OR circuit whose output provides the data input for the register. The 17th stage of the register is connected to a push-pull buffer, which is the circuit's output. This output provides continuous constant amplitude pseudo-random noise; that is, for any time slot, ones and zeroes have an almost equal probability of occurrence.

Typical Applications

- ☐ Percussion Instrument Voice Generators for Rhythm Units
- ☐ Electronic Music Synthesizers
- ☐ Simulated Pipe "Wind" Noise
- ☐ Acoustics Testing

Power Supplies

The S2688 noise generator may be operated with either one or two power supplies. In applications where a high output drive level is not critical, or where the output is loaded with a resistive load connected to V_{DD}, it is possible to operate the device from a single supply voltage; in this case, the V_{GG} supply pin is connected to the V_{DD} supply voltage. If a low impedance logic "0" level output is required, this can be achieved by connecting the V_{GG} supply pin to a more negative voltage.

Zero State Lockup Prevention

If the outputs of all 17 stages of the shift register were simultaneously to reach a "0" logic level, and no logic were provided to prevent this state from occuring, then the register would remain in the "all-zero" state.

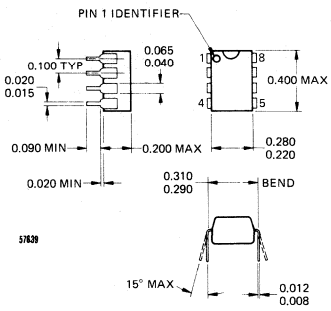
In this condition, the output would lockup and remain at a logic "0" level. This situation could occur when power is initially applied, or when triggered by noise spikes. To prevent this condition, a 17 input NOR gate is provided internally to decode the "all-zero" state and feed a logic "1" level into the register's data input.

Test Inputs

The S2688 has been designed to facilitate testing of the part. In the normal mode of operation, pins 6 and 7 are not used and appear to be open circuits. However, when the V_{GG} pin is connected to V_{SS}, these pins become test pins. Pin 7 (Test A) is used to force zeroes into the register, and pin 6 (Test B) becomes the clock input, driving the internal oscillator network. During the entire test period a 20KΩ load must be tied to V_{DD}.

Package Outline

8-Pin Plastic



AMERICAN MICROSYSTEMS, INC.

S8890

RHYTHM GENERATOR

Features

- ☐ Drives 9 Instruments
- ☐ 64 Bit Pattern
- ☐ 10 Rhythm Patterns per Instrument
- ☐ 5 Mask Programmable Reset Counts
- ☐ 7 Segment Count Display Output
- ☐ Internal Oscillator

Typical Applications

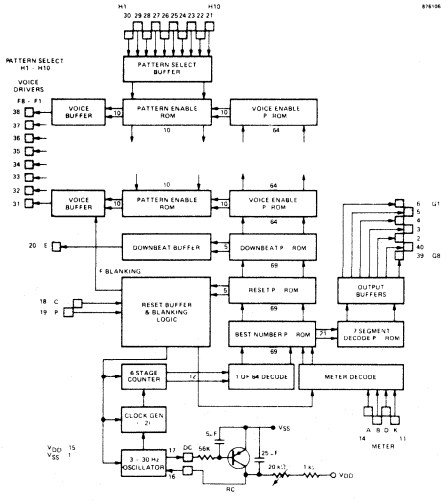
- ☐ Organ Rhythm Sections
- ☐ Portable Rhythm Sections
- ☐ Automatic Rhythm Organs
- ☐ Music Synthesizer

General Description

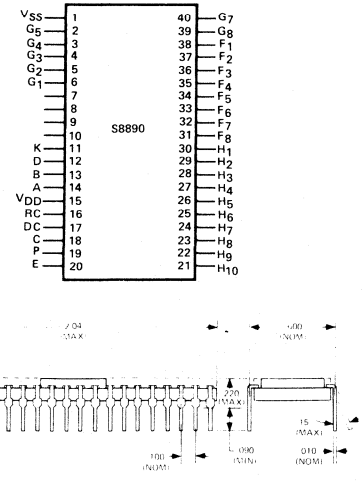
The rhythm generator is a counter-ROM specifically designed for electronic organ and other electronic instruments. This product contains an internal oscillator, a 6 bit counter, and a ROM that drives nine rhythm instruments and also drives a seven segment sequence count display.

The oscillator frequency is determined by an external network. The 6 bit counter has control inputs that allow the counter to reset at any one of five counts. Five reset counts are mask programmed to user requirements. The 64th count is normally programmed as the 5th reset selection option. The counter contains

Block Diagram



Pin/Package Configuration



a start input that holds the system in the reset mode until a start command is impressed.

The counter outputs drive a 64 word ROM. The ROM has two types of rhythm instrument outputs and a rhythm count output. The rhythm instrument outputs provide a trigger with up to 64 counts. One of the instrument outputs contains only one rhythm pattern for each reset option. This output can be programmed to generate a downbeat trigger at the beginning of each measure. The remaining eight instrument outputs each contain 10 rhythm patterns which may be simultaneously selected to overlay multiple rhythm patterns.

The rhythm count outputs a seven segment code that can be used as a visual display of the musical timing. For example, if 4/4 timing is provided by the programmable option, and the appropriate control lined (I_R) are activated then the seven segment display will provide the pattern in Figure 2. Four numbers (1, 2, 3 or 4) will be displayed, one for each group of four quarter notes in a 16 note measure. The pattern will repeat for subsequent measures. Other sequences can be programmed for alternate timing schemes.

Internal input pull-up resistors to V_{DD} are provided on all inputs except the oscillator input. Output buffers consist of a single ended device to V_{SS}. The product is fabricated with I^{2TM} technology and is packaged in a 40 lead dual in-line package.

Functional Description of Input/Output Pins

DUMP CHARGE

Provides base current when required through an RC delay of approximately 25 msec to a PNP transistor which should be connected across the capacitor in the oscillator.

Input	Rhythm	Bits/Beat
A	3/4	3
B	5/4	4
D	6/8	4
K	3/4	4
Default	4/4	4

RESET:

C Input

When allowed to approach V_{DD}, the outputs are held disabled and the system is held ready to begin with the first bit of the First measure. The system starts when V_{SS} is applied.

PATTERN SELECT:

H1-H10 Inputs

V_{SS} applied to one enables one combination of the voices in a specific rhythm pattern. Any combination of patterns may be enabled at the same time. The customer must provide the voice pattern as a function of each pattern selected and of each bit time.

OUTPUT DUTY CYCLE:

P Input

When allowed to approach V_{DD}, the voice inputs are held off for one half of each bit time. When held at V_{SS}, the voice outputs are constantly valid. Note that neither option hides the short (<80 μsec) decode spikes.

The chip output functions are as follows.

VOICE DRIVERS:

F1-*F8*

When selected, internally, the outputs provide a low resistance path to V_{SS} which is suitable for driving a transistor interface. The chip input functions are as follows.

METER:

V_{SS} applied to the following inputs sets up the chip with a programmable number of bits per beat, beats per measure and measures before reset. A currently programmed example follows.

Beats/Measure	Measure/Reset	Bits/Reset
3	4	36
5	2	40
6	2	48
3	4	48
4	4	64

BEAT NUMBER DISPLAY:

G1-*G8 (less 6)*

When selected, internally, the outputs provide a low resistance path to V_{SS} suitable for sinking the current required to drive a GE7 segment display tube. The ROM driving these outputs must be programmed to match the meter program.

DOWNBEAT:

$\overline{E}$

When selected internally, the output provides a low resistance path to V_{SS}.

The Oscillator Interconnects are as follows.

RC PAD:

A 25 μF capacitor to V_{SS} and a series combination of a 20 KΩ potentiometer and a 1 KΩ resistor to V_{DD} will allow a range of about 1.5 to 15 bits/second.

P-ROM PROGRAMMING FORMATS

Programming the Rhythm Generator requires 132 IBM cards punched with the data outlined below. Each card should end with CXXXX—NNN where XXXX is a number provided by AMI and NNN is the card number.

DOWNBEAT ROM:

Columns	Contents
1-64	Enter '1' for the first bit of each measure of the given meter. (No gate = '1')
72-80	CXXXX-NNN per above.

Card	Meter
001	N
002	K
003	D
004	B
005	A

RESET ROM:

Columns	Contents
1-64	Enter '1' for the last bit before a reset and for all subsequent bits. (No gate = '1')
72-80	CXXXX-NNN per above.

Card	Meter
006	N (Meter N must not have a reset before 64)
007	K
008	D
009	B
010	A

NOTE: '1' always means an activated output and thus, may represent a gate or a lack of one.

BEAT NUMBER ROM:

Card	Column	Content
A	1-50	Enter '1' for each bit where the NUMBER should be on. (No gate = '1'). Enter the first
B	1-14	50 bits on Card A, last 14 bits on Card B.
B	16-20	Meter bit pattern
B	22-28	7 Segment Display Pattern
A&B	72-80	CXXXX-NNN per above.

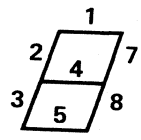
Enter the beat number data on adjacent cards starting with 011 for A and 012 for B and ending on or before 052.

Order data by Meter bit patterns as follows:

first	N	'00001'
first	K	'00010'
first	D	'00100'
first	B	'01000'
last	A	'10000'
unused		00000

Group beat numbers in order within each meter using the following decode for numerical compatibility with GE7 Segment tubes.

		Beat Number to be displayed							
		1	2	3	4	5	6	7	None
	G1 col. 22	0	1	1	0	1	1	1	0
	G2 col. 23	0	0	0	1	1	1	0	0
Segments to	G3 col. 24	0	1	0	0	0	1	0	0
be activated	G4 col. 25	0	1	1	1	1	1	0	0
(Gate='1')	G5 col. 26	0	1	1	0	1	1	0	0
	G7 col. 27	1	0	1	1	1	1	1	0
	G8 col. 28	1	1	1	1	0	0	1	0



RHYTHM GENERATOR

Features

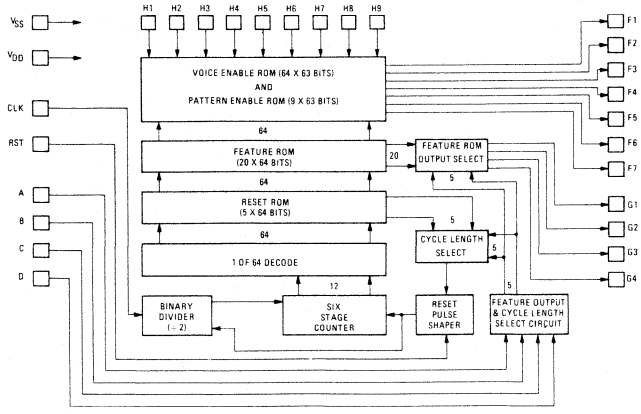
- ☐ Drives 7 Instruments
- ☐ 64 Bit Patterns
- ☐ 9 Rhythm Patterns
- ☐ 4 Feature Outputs
- ☐ 5 Programmable Feature Selections
- ☐ All Rhythm Patterns Additive
- ☐ 5 Programmable Resets
- ☐ All Counters and Decoders Internal
- ☐ All Patterns User Programmable

General Description

The S9660 rhythm generator is a counter-ROM specifically designed for use in rhythm sections of electronic organs and independent electronic rhythm units. This product contains a six stage counter, all internal ROM decoding, a 4K bit pattern ROM, and a 1K bit feature ROM. A total of nine distinct 64-bit rhythm patterns are generated and may be used to control up to seven rhythm instruments. In addition, the feature ROM provides four outputs that may be used for automatic chord gating, walking bass, or to create rhythm pattern variation.

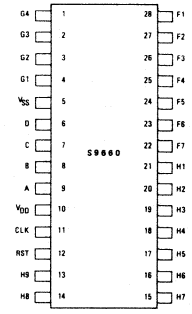
The 6-bit counter may be reset at any bit from 1

Block Diagram



177175

Pin/Package Configuration



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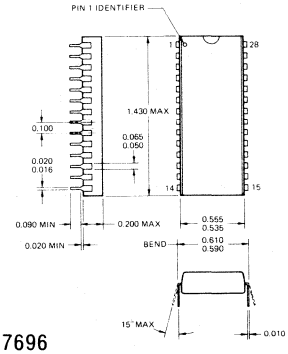


87696

through 64 to obtain any desired counter cycle. This counter cycle control is determined by the user's individually programmed ROM pattern, which allows the electrical selection of up to five different counter cycle lengths in one S9660.

The counter outputs drive a 64 × 63 bit rhythm pattern ROM and a 64 × 20 bit feature ROM. The rhythm pattern ROM drives seven instrument outputs and generates nine rhythm patterns which may be simultaneously selected to overlay multiple rhythm patterns. The feature ROM drives four outputs; depending on which of the five reset conditions is selected, the four outputs each contain five distinct 64 bit patterns. These may be used to drive such features as walking bass, automatic chording, or rhythm variation.

Internal input pull-up resistors to V_{DD} are provided on all inputs, and output buffers consist of open drain devices with source connected to V_{SS}. The product is fabricated with P-channel ion implanted MOS technology and is packaged in a 28 lead dual in-line plastic package.

Typical Applications

Organ Rhythm Sections, Portable Rhythm Units, Automatic Chording Systems, Walking Bass.

Operational Description

A block diagram of the S9660 appears on page 4, along with a typical timing diagram. All rhythm patterns, feature patterns, and counter cycle lengths are user programmable, and detailed instructions for this are given on page 5.

CLK Input (pin 11):

A clock frequency from an external oscillator is supplied to this pin to provide the timing information to the 6 bit rhythm counter. As this frequency is varied, the speed, or tempo, of the generated rhythm is varied.

As indicated in the block diagram, the CLK input is divided by two and then applied to the 6 stage counter. This means that each of the output bit periods is equal to two input clock periods. For example, if the rhythm counter is programmed to recycle every 48 bits, and the cycle is divided into two measures of 4 beats each, then each beat contains 6 bits; if the CLK input frequency is 30 Hz, then, rhythm timing will be 15 bits per second, or 900 bits per minute, or 150 beats per minute.

H Inputs (pins 13 through 21):

Normally pulled to V_{DD}, application of a V_{SS} level to any of the 9 H inputs enables one combination of voices that comprise a specific rhythm pattern. Any combination of patterns may be enabled simultaneously by applying V_{SS} to other H inputs. The user must provide the desired voice pattern as a function of each H pattern selected and of each bit time. This is programmed in the Voice Enable ROM.

RST Input (pin 12):

Normally pulled to V_{DD}, application of a V_{SS} level to the RST input enables the rhythm counter. When RST is left unconnected, the binary divider (÷ 2) and the rhythm counter chain are reset to count one, and all "F" outputs are held in an off condition. When V_{SS} is applied, the bit pattern selected for the first address of the ROM (count one) will activate the appropriate "F" outputs. Subsequent clock pulses at the CLK input will cause the counter to advance its count as indicated in the timing diagram.

A, B, C, D Inputs (pins 9, 8, and 6):

These inputs control two functions, the selection of cycle length (or counter reset bit) and the bit patterns of the four G outputs. Normally pulled to V_{DD}, these outputs may be selected (only one at a time) by applying V_{SS}. A fifth condition called "default," or "N", occurs when none of the four A, B, C, or D inputs is selected.

Up to five reset bits (or counter lengths) may be programmed so that five different counter lengths may be selected by use of A, B, C, or D. These resets are programmed by the Reset ROM. This allows a 4/4 rhythm to contain 64 bits and a 3/4 rhythm to contain 48 bits, for example, so that when switching from a swing beat to a jazz waltz it is not necessary for the player to adjust the tempo control.

For each of the five A, B, C, D, or Default conditions there is a unique pattern supplied on the four G outputs. This information is programmed into the Feature ROM.

F Outputs (pins 22 through 28):

When selected internally by the Voice Enable ROM, these seven open drain outputs provide a low resistance path to V_{SS}. These outputs are suitable for driving a transistor interface to electronic rhythm voice generators. Decode spikes may appear at the F

outputs, though they are of short enough duration (< 80 μs) that most instrument voice generators would be unaffected.

G Outputs (pins 1, 2, 3, and 4):

When selected internally by the Feature ROM, the four open drain G outputs provide a low resistance path to V_{SS}. Five distinct patterns are available on each of the outputs and are selected by the A, B, C, D, inputs. The decode spikes mentioned in the "F" output paragraph may also be present in the "G" outputs.

Absolute Maximum Ratings

Positive voltage on any pin	V_{SS} + 0.3 Volts
Negative voltage on any pin	V_{SS} − 28 Volts
Storage temperature	−65° to + 150°C
Operating Ambient Temperature	0°C to + 70°C

CONSUMER

Electrical Specifications

(0°C ≤ t_a ≤ 70°C; −10 Volts ≥ V_{DD} ≥ − 14 Volts unless otherwise specified)

Symbol	Parameter	Min	Max	Units	Conditions
V_{IL}	Input logic "0"	V_{DD}	V_{DD} + 2.0	Volts	See Note 1
V_{IH}	Input logic "1"	V_{SS} − 0.7	V_{SS}	Volts	
V_{CLK_L}	Input logic "0" (CLK input)	V_{DD}	V_{DD} + 1.0	Volts	
V_{CLK_H}	Input logic "1" (CLK input)	V_{SS} − 0.7	V_{SS}	Volts	
t_{cr}, t_{cf}	CLK input rise and fall time		100	μs	Measured at 10% to 90% of V_{DD}
f_c	Clock frequency (CLK input)	DC	5K	Hz	
V_{OL}	Output logic "0"				See Note 2
V_{OH}	Output logic "1"	V_{SS} − 2.0	V_{SS}	Volts	V_{DD} = −12.0 Volts I out = 1 mA maximum
P	Average power dissipation		300	MW	Measured at 25°C

NOTES: 1. *Internal 5μA minimum pullup to V_{DD} is provided.*
2. *External load to V_{DD} is required.*

Programming Instructions

Programming of the S9660 is a straightforward process requiring the user to supply a total of 110 cards. There are three ROM sections to be programmed, the Reset ROM, the Feature ROM, and the Voice Enable ROM. Detailed instructions for punching the cards required to program these three ROMs are supplied below. In column 72-80 of each card, as described below, two numbers appear-CXXXX and NNN. The CXXXX is a number to be given to the user by AMI prior to punching the card deck, and NNN is the sequence number of the card.

RESET ROM:

A total of five cards are required to program the reset ROM. Their card numbers are 001 through 005. Each card determines at what bit the rhythm counter will reset (i.e., the number of bits per cycle) for one of the five electrically selected conditions, A, B, C, D, or N (N = ABCD). Card 001 corresponds to N, 002 to D, 003 to C, 004 to B, and 005 to A.

Columns	Contents
1-64	Enter a "1" for the last bit before an internal reset occurs and for all subsequent bits through 64.
72-76	CXXXX—To be assigned by AMI, as stated above.
78-80	Enter number of the card (001 through 005).
Example:	If card 003 has all ones in columns 48 through 64, then whenever the C input is selected, the rhythm generator will reset at the end of bit 48, giving a 48 bit cycle length.

AMERICAN MICROSYSTEMS, INC.

S50240/S50241/S50242

TOP OCTAVE SYNTHESIZER

Features

- ☐ Single power supply
- ☐ Broad supply voltage operating range
- ☐ Low power dissipation
- ☐ High output drive capability
- ☐ S50240—50% output duty cycle
- ☐ S50241—30% output duty cycle
- ☐ S50242—50% output duty cycle

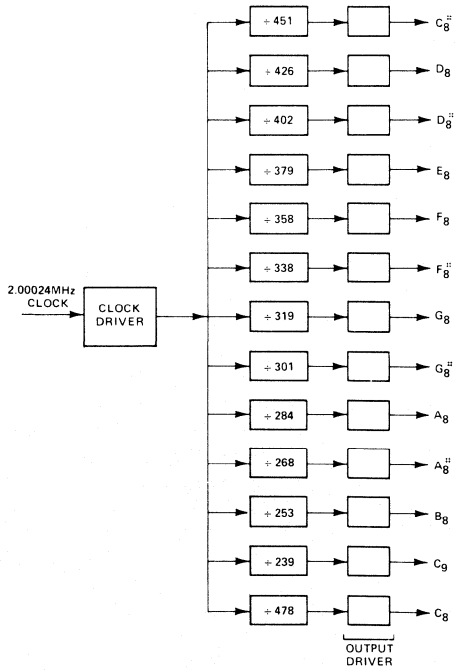
General Description

The S5024 is one of a family of ion-implanted, P-channel MOS, synchronous frequency dividers.

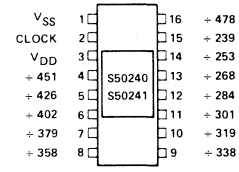
Each output frequency is related to the others by a multiple $12\sqrt{2}$ providing a full octave plus one note on the equal tempered scale.

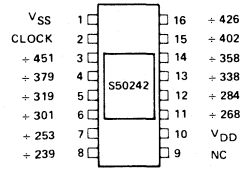
Low threshold voltage enhancement-mode, as well as depletion mode devices, are fabricated on the same chip allowing the S5024 family to operate from a single, wide tolerance supply. Depletion-mode technology also allows the entire circuit to operate on less than 360 mW of power. The circuits are packaged in 16 pin plastic dual-in-line packages.

Block Diagram



Pin Connections





RFI emination and feed-through are minimized by placing the input clock between the V_{DD} and V_{SS} pins. Internally the layout of the chip isolates the output buffer circuitry from the divisor circuit clock lines. Also, the output buffers limit the minimum rise time under no load conditions to reduce the R.F. harmonic content of each output signal.

Absolute Maximum Ratings

Voltage on any pin relative to V_{SS}	+0.3V to −20V
Operating Temperature (Ambient)	0 °C to 50 °C
Storage Temperature (Ambient)	−65 °C to +150 °C

CONSUMER

Recommended Operating Conditions

(0 °C ≤ T_A ≤ 50 °C)

Symbol	Parameter	Min	Typ	Max	Units	Figure
V_{SS}	Supply Voltage	0		0	V	
V_{DD}	Supply Voltage	−11.0	−14.0	−16.0	V	

Electrical Characteristics

(0 °C ≤ T_A ≤ 50 °C; V_{DD} = −11 to −16V unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units	Figure
V_{IL}	Input Clock, Low	0		−1.0	V	Figure 1
V_{IH}	Input Clock, High	−10.0		V_{DD}	V	Figure 1
f_I	Input Clock Frequency	100	2000.240	2250	kHz	
t_r, t_f	Input Clock Rise & Fall Times 10% to 90% @ 2.5MHz			50	nsec	Figure 1
t_{ON}, t_{OFF}	Input Clock On and Off Times @ 2.5MHz		200		nsec	Figure 1
C_I	Input Capacitance		5	10	pF	
V_{OH}	Output, High @ 1.0mA	V_{DD} +1.5		V_{DD}	V	Figure 2
V_{OL}	Output, Low @ 1.0 mA	V_{SS} −1.0		V_{SS}	V	Figure 2
t_{ro}, t_{fo}	Output Rise & Fall Times, 500 pF Load 10% to 90%	250		2500	nsec	Figure 3
t_{ON}	Output Duty Cycle-S50240, S50242		50		%	
	S50241		30		%	
I_{DD}	Supply Current		14	22	mA	Outputs Unloaded

Figure 1. Input Clock Waveform

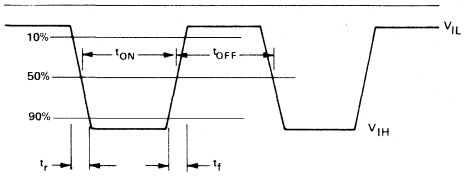


Figure 2. Output Signal DC Loading

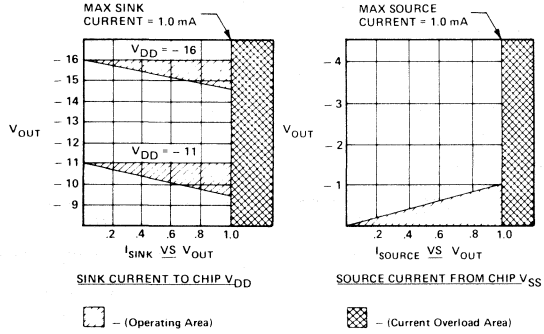
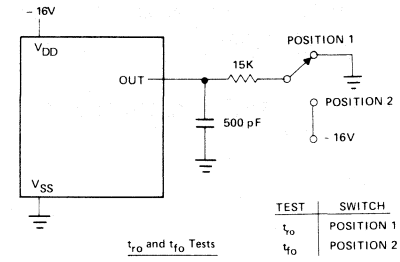
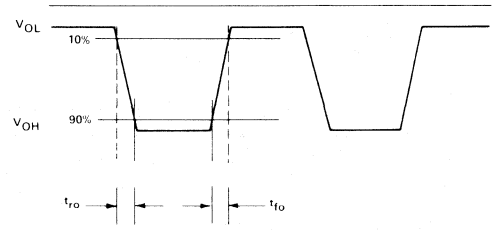


Figure 3. Output Rise and Fall Times



TEST	SWITCH
t_{ro}	POSITION 1
t_{fo}	POSITION 2



Consumer Products Late Addition

Remote Control Chip Set

S2747 Encoder
S2748 Decoder

- ☐ Low Power CMOS Encoder/Decoder
- ☐ 512 Codes/9-Bits
- ☐ Wide Supply Voltage Range
- ☐ Timer on Decoder Output

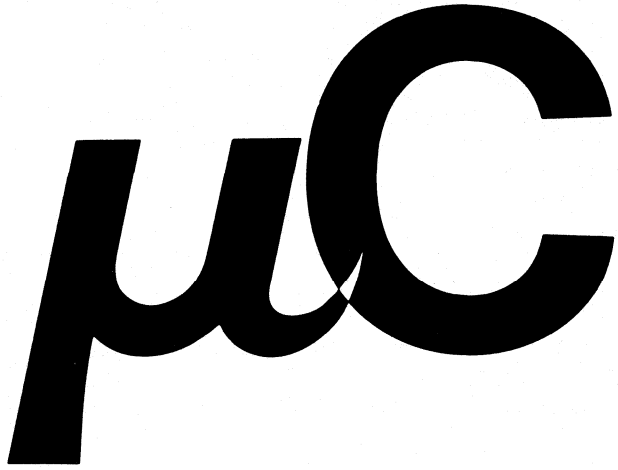
Contact factory for more information

AMI

AMERICAN MICROSYSTEMS, INC.

S2000

Single-Chip Microcomputer Family



Applications

The S2000 can lower the cost and enhance the performance of control circuits in applications such as the following:

- ☐ Vehicle instrumentation and systems control
- ☐ Major household appliances
- ☐ CB radios, stereo receivers, tape decks
- ☐ Electronic scales
- ☐ Toys and games
- ☐ Lab instruments
- ☐ Telephone equipment
- ☐ Programmable calculators
- ☐ Data sampling devices
- ☐ Data logging devices
- ☐ Test equipment
- ☐ Keyboard devices
- ☐ Display devices
- ☐ Remote monitors
- ☐ Security systems
- ☐ Set-back thermostats

Functional Description

The basic S2000 has an on-chip 1024-instruction ROM; other family members have ROMs ranging up to 2048 instructions (see tables). If necessary, additional program memory can be added externally up to a maximum of 8192 instructions. The Program counter is a pointer to the next instruction to be executed. The Program Counter Stack holds return addresses during execution of subroutines or interrupts.

The scratchpad RAM holds the temporary values of 4-bit data words, typically numeric quantities. The BA, BU and BL registers are used to access RAM words. The E Register can be used as a general purpose register or as an index limit register for controlling RAM access.

The ALU—Arithmetic Logic Unit—performas data operations, using the Accumulator and the Carry Register. Software can set reset and test Flags as temporary indicators.

The Control Logic includes three inputs and three outputs for interfacing external devices. The Oscillator generates all clocking signals and needs only an external RC circuit to set its rate. Optinally a crystal may be used to precisely control the oscillator frequency.

The K Lines range from a voltage comparator, Schmitt-trigger, and timer inputs on the S2000, to a full bidirectional port on the S2200 supporting A/D and D/A converters, interrupts, and a programmable counter.

The eight bi-directional three-state D Lines are general-purpose data signals. The thirteen A Lines are outputs for displays, keyboard strobes, control signals, or address lines for external ROM.

Various ROM and RAM options are available for the S2200.

"A" Versions for Vacuum Fluorescent Display

The "A" versions of the S2000 Family provide high voltage fluorescent display capability but are otherwise identical to their non-"A", LED counterparts. The output buffer drive (V_{DD}) is changed to a vacuum fluorescent drive (V_{FD}) and typically tied to 35 volts. The D_0 through D_7 and A_0 through A_4 are changed from LED drivers (nominal 5 to 9 volts) to vacuum fluorescent drivers (nominal 26 to 35 volts).

CMOS Version—S4200

For those applications which require micropower, the S4200 is a CMOS version of the S2200. The S4200 is functionally and software compatible to the S2200.

Various ROM and RAM options are available.

Microprocessor Bus-Compatible Version—S2300

The S2300 bus-compatible version of the S2200 can be used as a user programmable peripheral for multiprocessor systems. This processor is software compatible with all the other members of the family and is functionally identical (with the exception of some control lines and the D-line interface) to all the other members.

Various ROM and RAM options are available.

Peripheral Circuits

The S2809 can be used as a parallel output device for the S2000/2200. It provides 32 high current/voltage outputs for such applications as triac triggering, low voltage incandescent displays, LCD displays and VF displays.

Development Support Tools

For more information on support tools, both hardware and software, see the Development System Support section of this catalog.

Product Features	S2000	S2000A	S2150	S2200	S2300[1]	S4200[2]	S4300[1,2]
ROM (Bytes)	1K	1K	1.5K	2K	2K	2K	2K
RAM (Nibbles)	64	64	80	128	128	128	128
A/D Converter (8-Bit)	—	—	—	YES	YES	YES	YES
Counter	50/60Hz	50/60Hz	50/60Hz	Prog 8-Bit	Prog 8-Bit	Prog 8-Bit	Prog 8-Bit
Interrupts	—	—	—	2	2	2	2
Power Fail Detect	—	—	—	YES	YES	YES	YES
High Voltage Outputs	—	YES	—	—	—	—	—
Crystal Clock Option	—	—	YES	YES	YES	YES	YES
Touch Control Inputs	YES	YES	YES	YES	YES	YES	YES
Levels of Subroutine	3	3	3	3-5	3-5	3-5	3-5
# of Flags	2	2	2	262	262	262	262
Table Look-up	—	—	—	YES	YES	YES	YES
Power-Down RAM Option	—	—	—	YES	YES	YES	YES
D/A Converter Option	—	—	—	YES	YES	YES	YES
Zero Crossing Detect	YES	YES	YES	YES	YES	YES	
Cycle Time (μsec)	4.5	4.5	4.5	4.5	4.5	4.5	4.5
Instructions—Total	51	51	51	63	63	63	63
Single Cycle, Single Byte	49	49	49	52	52	52	52
Voltage (volts)	9	9/32	9	5	5	5	5
Development Support							
Software[3]	YES	YES	YES	YES	YES	YES	YES
Hardware Emulator[4]	SES-2150	SES-2150	SES2150	SES2200	—	—	—

1. Microprocessor bus compatible
2. CMOS
3. Motorola Exorcisor, Tektronix 8002A and Intel Intellec Development System Support for the S2000 Family also available.
4. Prototyping chips S2200PR and S2300PR also available.

AMI's S2000 Family of single-chip microcomputers brings the advantages of microprocessor control to low-cost, multi-feature keyboard/display systems. These circuits are optimized to reduce systems cost while at the same time providing the user with the ability to select from a variety of architectural features. Versatile input/output and an instruction set optimized for its intended applications make an S2000 Family member preferable to expensive multiple-chip solutions. Dramatic cost reductions are possible during product design, manufacture, testing, and maintenance. Two versions are available for the members of the S2000 Family: The standard version for direct drive of LED displays and the "A" version for direct drive of fluorescent displays.

Features

The S2000 Family members are entire computers on a chip, suitable for volume keyboard/display applications which require control in a minimum space at a minimum cost.

They are ideally suited for systems with the following requirements:

- ☐ Analog-to-digital and digital-to-analog conversion
- ☐ Time-of-day and interval timer control
- ☐ AC line synchronization
- ☐ Display drive
- ☐ Keyboard inputs (ohmic or TouchControl)
- ☐ Arithmetic operations
- ☐ Single power supply
- ☐ Program expandability and testability
- ☐ Triac drive

AMERICAN MICROSYSTEMS, INC.

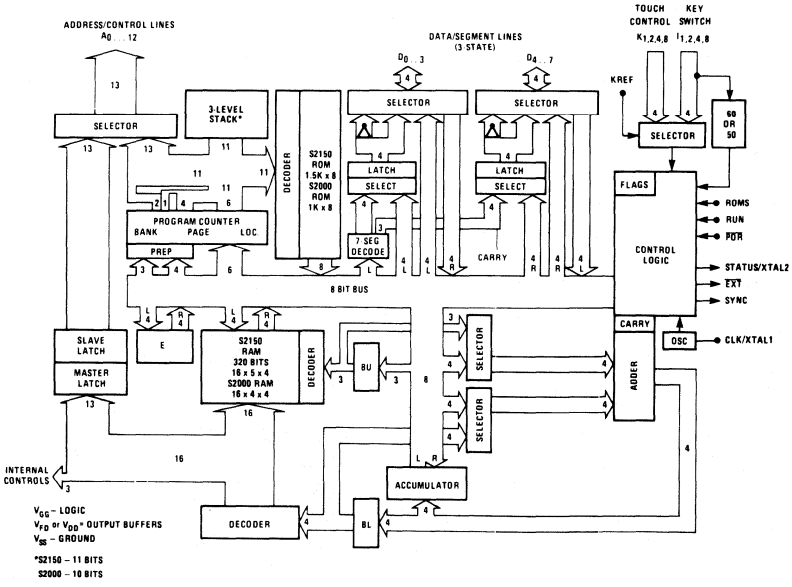
S2000/S2150

SINGLE-CHIP MICROCOMPUTERS

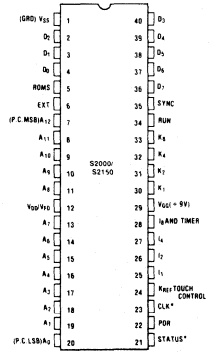
Features

- ☐ 1K Bytes Program ROM On-Chip; Externally Expandable to 8K Bytes—S2000
- ☐ 1.5K Bytes Program ROM On-Chip; Externally Expandable to 8K Bytes—S2150
- ☐ 64×4 Scratchpad RAM On-Chip—S2000
- ☐ 80×4 Scratchpad RAM On-Chip—S2150
- ☐ Seconds Timer for Both 60Hz and 50Hz Lines
- ☐ 7-Segment Decoder
- ☐ LED Display Drivers—S2000/S2150
- ☐ Vacuum Fluorescent Display Drivers—S2000/S2150A
- ☐ Single +9V Supply
- ☐ Fast 4.5μs Execution Cycle
- ☐ Three-Level Subrouting Stack
- ☐ TTL-Compatible Outputs
- ☐ Reset, Test, and Halt Modes
- ☐ Crystal Input for Accurate Clocking—S2150
- ☐ 30 I/O Lines
  - ☐ 13-Bit Output Port
  - ☐ 8-Bit Output Port with Strobe
  - ☐ Two 4-Bit Input Ports

Block Diagram



Pin Configuration



Functional Description

The S2000/S2150 are ideal for a wide range of appliance and process control designs. Versatile input/output and an instruction set optimized for its intended applications make the S2000 preferable to expensive multiple-chip solutions with dramatic cost reductions during product design, manufacture, testing, and maintenance.

The S2000/S2150 have an on-chip 1024/1536 instruction ROM. If necessary, additional program memory can be added externally up to a maximum of 8192 instructions. The Program Counter is a pointer to the next instruction to be executed. The Subroutine Stack holds return addresses during execution of subroutines.

The scratchpad RAM holds the temporary values of 64/80 4-bit data words, typically numeric quantities. The BU and BL registers are used to access RAM words. The E Register can be used as a general purpose register or as an index limit register for controlling RAM accesses.

The ALU—Arithmetic Logic Unit—performs data operations, using the Accumulator and the Carry Register. Software can set and test two Flags as temporary indicators.

The Control Logic includes three inputs and three outputs for interfacing external devices. The Oscillator generates all clocking signals and needs only an external RC circuit to set its rate. The KREF Input is the analog reference for TouchControl and similar interfaces. Software decision-making instructions sample the four K Inputs and the four I Inputs, one of which can be used as a line-frequency counter.

The eight bi-directional three-state D Lines are general-purpose data signals. The thirteen A Lines are outputs for displays, keyboard strobes, control signals, or address lines for external ROM.

S2000/S2150 Instruction Set Summary

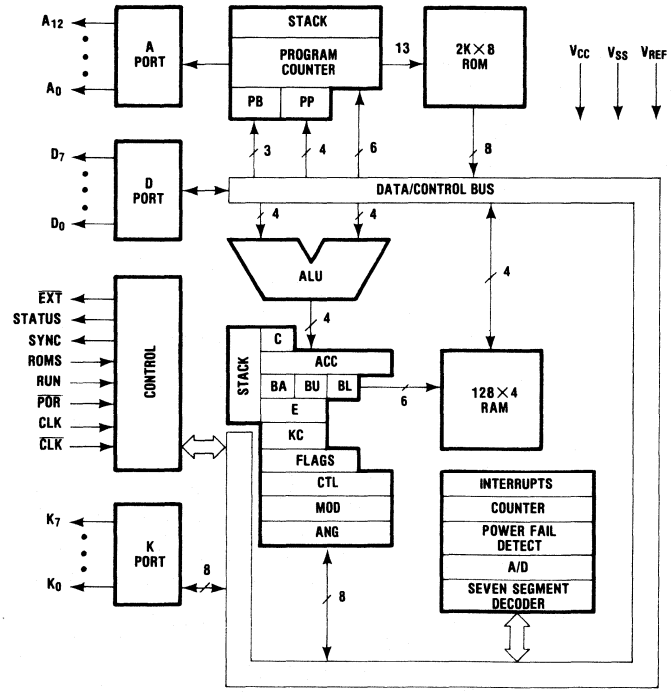
ADCS	ACC+RAM+CARRY, Skip if Sum $\leq$ 15
ADD	ACC+RAM
ADIS X	ACC+X, Skip if Sum $\leq$ 15
AND	ACC "AND" RAM
CMA	Complement ACC
DISB	Display Number in Binary Format
DISN	Display Number in Seven Segment Format
EUR	(European) SET 50/60Hz and Display Latch Polarity
INP	Input 8 Bits from D Lines
JMP X	Jump
JMS X	Jump to Subroutine
LAB	Load ACC with BL
LAE	Load ACC with E
LAI X	Load ACC with X
LAM Y	Load ACC with RAM then BU "XOR"Y
LBE Y	Load BL with E and BU with Y
LBF Y	Load BL with 15 and BU with Y
LBEP Y	Load BL with E+1 and BU with Y
LBZ Y	Load BL with 0 and BU with Y
MVS	Move Strobe to A Lines
NOP	No Operation
OUT	Output 8 Bits to D Lines
PP X	Prepare Page (or Bank)
PSH	Preset Master Strobe High
PSL	Preset Master Strobe Low
RF1	Reset Flag 1
RF2	Reset Flag 2
RSC	Reset Carry
RSM Z	Reset RAM Bit Z
RT	Return from Subroutine
RTS	Return from Subroutine and Skip
SAM	Skip if ACC=RAM
SBE	Skip if BL=E
SF1	Set Flag1
SF2	Set Flag2
SOS	Skip if Seconds Flag Set
STC	Set Carry
STM Z	Set RAM Bit Z
SZC	Skip if Carry=0
SZI	Skip if I=0
SZK	Skip if K=0
SZM Z	Skip if RAM Bit Z=0
TF1	Skip if Flag1=1
TF2	Skip if Flag2=1
XAB	Exchange ACC with BL
XABU	Exchange ACC with BU
XAE	Exchange ACC with E
XC Y	Exchange ACC with RAM then BU "XOR"Y
XCD Y	Exchange ACC and RAM, BU "XOR"Y, Decrement BL, and Skip if BL=0 Before Decrementing
XCI Y	Exchange ACC and RAM, BU "XOR"Y, Increment BL, and Skip if BL=0 After Incrementing
XOR	ACC "Exclusive-OR" RAM

SINGLE-CHIP FAMILY OF MICROCOMPUTERS

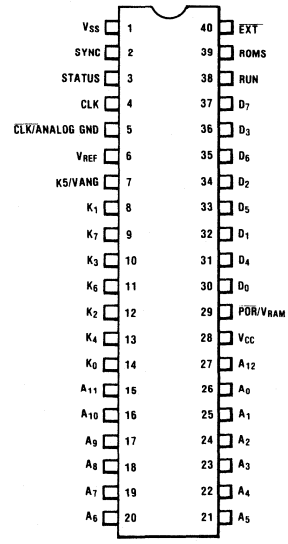
Features

- ☐ Up to 2K Bytes Program ROM On-Chip and Expandable to 8K Bytes (S2200/S4200)
- ☐ Up to 128×4 Scratchpad RAM On-Chip with Power-Down Mode
- ☐ 8-Bit A/D Converter with 8 Inputs
- ☐ 8-Bit D/A Converter
- ☐ 30 I/O Lines
  - ☐ 13-Bit Output Port
  - ☐ 8-Bit Bidirectional Port W/Strobe
  - ☐ 8-Bit Bidirectional Analog/Digital Port
- ☐ Two-Level Maskable Priority Interrupt System
- ☐ Programmable 8-Bit Counter
- ☐ Seven-Segment Display Decoder/Drivers
- ☐ Single +5V Power Supply 4.5μs Cycle Time
- ☐ 63 Instructions
- ☐ Microprocessor Bus-Compatible Versions S2300/S4300
- ☐ CMOS Versions S4200/S4300
- ☐ Table Look-Up Ability
- ☐ 3-Level Subroutine Stack (5-Level if Interrupts Not Used)
- ☐ 2-Level Parallel Interrupt Stack
- ☐ Power Failure Detection and Power-On-Reset Circuitry
- ☐ Single Step Capability
- ☐ Built-In Test Mode
- ☐ Up to 256 General Purpose Flags (RAM Bank 1)
- ☐ 6 Special Purpose Flags

Block Diagram



Pin Configuration



General Description

The S2200/S4200 provides a quantum jump in chip features beyond the S2000. In addition to all the features the S2000 offers, the S2200 gives the added flexibility of interrupts and the sophistication of an on-chip A/D and/or D/A converter capable of handling analog data making it suitable for a wide range of applications.

The 128×4 scratchpad RAM holds the temporary values of 4-bit data words, typically numeric quantities. The BA, BU and BL registers are used to access RAM words. The E Register can be used as a general purpose register or as an index limit register for controlling RAM access.

The ALU—Arithmetic Logic Unit—performs data operations, using the Accumulator and the Carry Register. Software can set reset and test Flags as temporary indicators.

The Control Logic includes three inputs and three outputs for interfacing external devices. The Oscillator generates all clocking signals and needs only an external RC circuit to set its rate. Optionally a crystal may be used to precisely control the oscillator frequency.

The K Lines are a full bi-directional port on the S2200/S4200 supporting A/D and D/A converters, interrupts, and a programmable counter/timer.

The eight bi-directional three-state D Lines are general-purpose data signals. The $\overline{EXT}$ signal is an output data strobe for the D Lines. On the S2300, the D Lines become the data bus interface. The thirteen A Lines are outputs for displays, keyboard strobes, control signals, or address lines for external ROM.

There are various family members which are designed to be cost effective solutions to a wide variety of markets and applications. All family members are functional and software compatible to maximize their use to end customers and to minimize the cost to upgrade or modify a design to use another family member. Table 4.1 gives a complete list of present members to the S2200/S2300/S4200/S4300 Families.

To aid the user in developing hardware designs, two other chips are available: S2200PR and S2300PR. These chips come in a 64-pin plastic package.

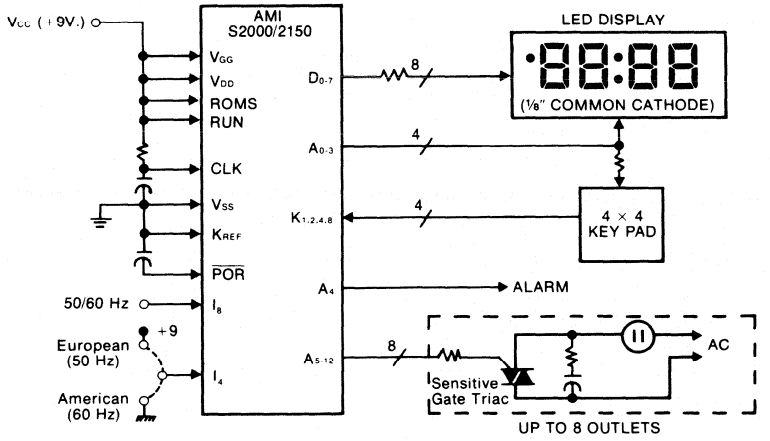
S2200/S2300/S4200/S4300 Instruction Set Summary

ADCS	ACC+RAM+CARRY, Skip if Sum ≤ 15
ADD	ACC+RAM
ADIS X	ACC+X, Skip if Sum ≤ 15
AND	ACC "AND" RAM
CMA	Complement ACC
DEV W	Skip Always
DISB	Display Number in Binary Format
DISN	Display Number in Seven Segment Format
IBLS	Increment BL and Skip if BL=0 after incrementing
IND	Input 8 Bits from D Lines
INK	Input 8 Bits from K Lines
JMP X	Jump
JMS X	Jump to Subroutine
JMSI	Jump to Subroutine Indexed
LAB	Load ACC from BL
LAE	Load ACC from E
LAI X	Load ACC with X
LAM Y	Load ACC with RAM then BU "XOR" Y
LAM Y	Load ACC from RAM then BU "XOR" Y
LANG	Load Analog Reg
LBE Y	Load BL with E and BU with Y
LBZ Y	Load BL with 0 and BU with Y
LMOD	Load Modulus Reg
LRAI W	Modify RAM Address
MVS	Move Strobe to A Lines
NOP	No Operation
OUTD	Output 8 Bits to D Lines
OUTK	Output 8 Bits to K Lines
PP X	Prepare Page (or Bank)
PSH	Preset A Register High
PSL	Preset A Register Low
RANG	Read Analog Reg
RAR	Rotate ACC Right
RBIN	Read Counter
RCTL	Read Control Reg

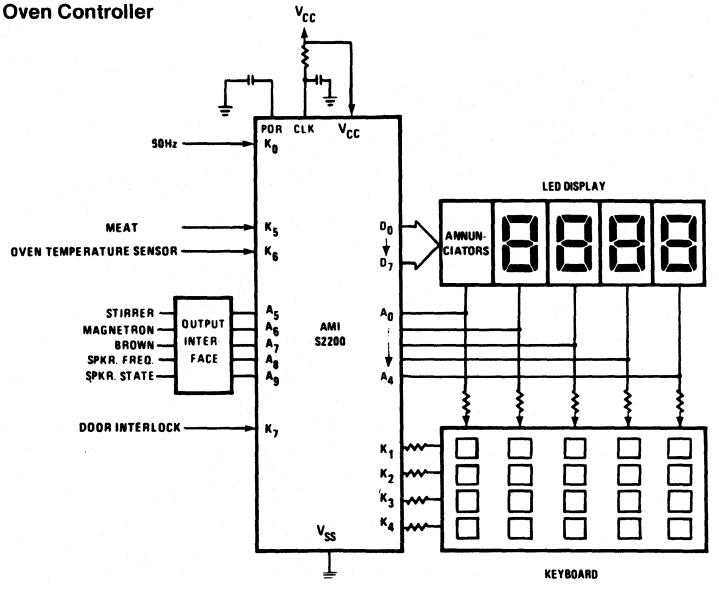
S2200/S2300/S4200/S4300
Instruction Set Summary (Continued)

RFLG W	Reset Flag W
RSC	Reset Carry
RSM Z	Reset RAM Bit Z
RSMI W	Reset RAM Bit W in Bank 1
RT	Return from Subroutine
RTI	Return from Interrupt
RTS	Return from Subroutine and Skip
SAM	Skip if ACC=RAM
SANG	Start A/D Conversion
SBE	Skip if BLE=E
SCTL	Set Control Reg
SFLG W	Set Flag W
STA	Store ACC in RAM
STC	Set Carry
STM Z	Set RAM Bit Z
STMI W	Set RAM Bit W in Bank 1
SWI	Software Interrupt
SZC	Skip if Carry=0
SZK	Skip if K=0
SZMI W	Skip if RAM Bit W in Bank 1=0
SZM Z	Skip if RAM Bit Z=0
TFLG W	Test Flag W
TLU	Table Look-Up
XAB	Exchange ACC and BL
XABU	Exchange ACC and BA, BU
XAE	Exchange ACC and E
XAK	Exchange ACC and KC
XC Y	Exchange ACC and RAM, then BU"XOR"Y
XCD Y	Exchange ACC and and RAM, Decrement BL, BU "XOR" Y, and Skip if BL=0 Before Decrementing
XOR	ACC "Exclusive-OR" RAM

S2000/S2150 Appliance/Outlet Controller



S2200 Microwave Oven Controller



The S2000/S2200 Family has several options which need to be specified before an order can be placed. The forms on the following two pages call out by part number which options are available and what must be specified, e.g., package type, operating temperature range, pin count, etc. For most options, simply circle the appropriate response. However, for the 28 pin package option, Table 1 details which pins cannot be deleted and which pins *may* be deleted. To assure that the customer's pin configuration can be bonded within the package, always consult with Microcomputer Product Marketing before placing an order.

S2000 Family
Mask Option Specification Form
For the S2000/S2000A, S2150

DATE _____

COMPANY NAME _____

CONTACT _____ PHONE NUMBER (_____)_____ EXT. _____

P.O.# _____ S.O.# (For Factory Use Only) _____

FILE NAME(For Diskette Only) _____

I. S2000/S2000A:

A. PACKAGE (Circle One): PLASTIC CERAMIC DIE

B. OPERATING TEMPERATURE RANGE (Circle One): T1 T2 T3 T4

C. PIN COUNT (Circle One): 28 40

IF 28, SPECIFY PINS (See Table 1): _____

_____

_____

T1 = 0°C to +55°C; T2 = 0°C to +70°C; T3 = 0°C to +85°C; T4 = −40°C to +85°C

I. S2150/S2150:

A. PACKAGE (Circle One): PLASTIC CERAMIC DIE

B. OPERATING TEMPERATURE RANGE (Circle One): T1 T2 T3 T4

C. PIN COUNT (Circle One): 28 40

IF 28, SPECIFY PINS (See Table 1): _____

_____

_____

D. CLOCK (Circle One): CRYSTAL R-C

Table 1. Optional/Required Pin Table for S2000/S2200 Families

S2000/S2150				S2200				
PIN#	**NAME**	**REQ.**	**OPT.**	**PIN#**	**NAME**	**REQ.**	**OPT.**	**CONDITIONS/REASONS**
1	V_{SS}	X		1	V_{SS}	X		Power supply-Ground
29	V_{GG}	X		28	V_{CC}	X		Power supply-most positive: +9V or +5V
2,3,4 36-40	D_0-D_7	X		30-37	D_0-D_7	X		Internal ROM Test
7-11 13-20	A_0-A_{12}		X	15-27	A_0-A_{11}, A_{12}		X	Program Counter Monitor, comprises skip, stack & jump test cannot reliably test if **all** lines deleted
5	ROMS	X		39	ROMS	X		Internal ROM test
6	$\overline{EXT}$		X	40	$\overline{EXT}$		X	Optional if SOS, OUTD instructions not used
35	SYNC	X		2	SYNC	X		Required
34	RUN	X		38	RUN	X		Required
22	POR	X		29	POR/	X		Required
					VRAM		X	Mask Option
23	CLK	X		4	CLK	X		
				5	$\overline{CLK}$		X	Required only if crystal option is exercised
21	Status		X	3	Status		X	
24	K_{REF}		X	6	V_{REF}		X	
				7-14	K_0-K_7		X	
12	V_{DD}/V_{FD}	X						Cannot be internally bonded to V_{GG}
25-28	I_1-I_8		X					
30-33	K_1-K_8		X					

This table shows which pins are required and optional for S2000/S2200 family devices. Those pins which are optional may be deleted in any mix to make a 28-pin package. If possible, pins should be deleted in as even a manner as possible to facilitate bonding the die to lead frame.

S2000 Family
Mask Option Specification Form
For the S2200

DATE _____

COMPANY NAME _____

CONTACT _____ PHONE NUMBER (_____)_____ EXT. _____

P.O.# _____ S.O.# (For Factory Use Only) _____

FILE NAME(For Diskette Only) _____

III. S2200:

A. PACKAGE (Circle One): PLASTIC CERAMIC DIE

C. PIN COUNT (Circle One): 28 40
IF 28, SPECIFY PINS (See Table 1): _____

C. R= _____ F. D= _____

G. C= _____

D P= _____ H. W= _____

E. I= _____ I. G= _____

J. OPERATING TEMPERATURE RANGE (Circle One): T1 T2 T3 T4

T1 = 0°C to +55°C; T2 = 0°C to +70°C; T3 = 0°C to +85°C; T4 = −40°C to +85°C

NAME OF OPTION	CODE		
RAM POWER	R	R = 1 TO 16:	RAM power is supplied from the $\overline{POR}/V_{RAM}$ Pin (see S2200 (PDS)
		R = 0:	RAM is supplied from V_{CC}
POWER-FAIL DETECTION	p	P = 1:	A non-maskable interrupt (jump to address 0046 HEX) occurs when V_{CC} V_{POR}
		P = 0:	No interrupt for low V_{CC}
LOW-PRIORITY INTERRUPT—K_7	I	I = 0:	K_6 & K_7 not connected to interrupt logic
		I = 1:	K_6 only connected to interrupt logic
HI-PRIORITY INTERRUPT—K_6		I = 2:	K_7 only connected to interrupt logic
		I = 3:	Both K_6 & K_7 conneced to interrupt logic
D/A OUTPUT		D = 1:	Digital-to-Analog converter output appears at K_5 (G must = 1)
		D = 0	Digital-to-Analog converter output not connected
ANALOG GROUND		G = 1:	The A/D-D/A converter ground connection is connected to the ANALOG GND pin 5 (C must = 0)
		G = 0:	ANALOG GND is not connected
CLOCK OSCILLATOR	C	C = 1:	On-chip master oscillator configured to accept a piezoelectric crystal; can be driven by an external oscillator (G must = 0)
		C = 0:	On-chip oscillator uses an external resistor and capacitor; or can be driven by an external oscillator
RESET STATE OF A-LINE	W	W = 1:	Whenever the chip enters power-on reset, the "A" outputs are all set to ones
		W = 0:	"A" outputs are all zeroes after POR

Choice of wide operating temperatures ranges may require slight derating of some electrical parameters; please consult with the factory

AMERICAN MICROSYSTEMS, INC.

S2809

UNIVERSAL DISPLAY DRIVER

Features

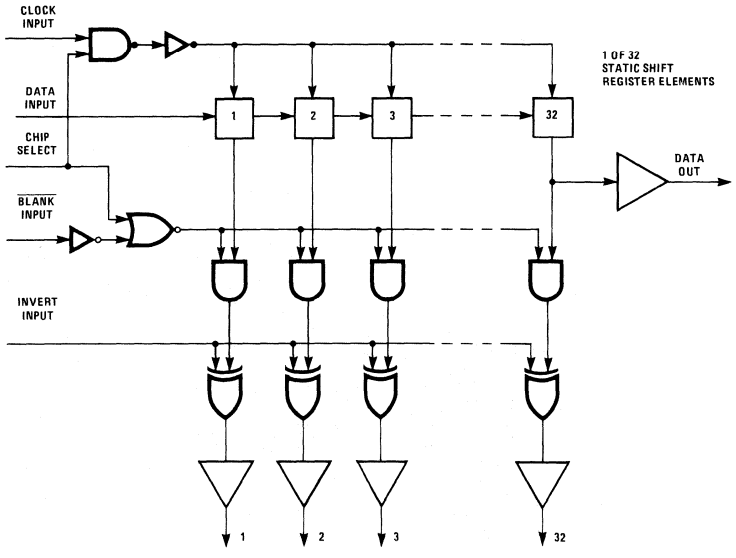
- ☐ 32 Bit Data Storage Register
- ☐ Drives LED, LCD, or Vacuum Fluorescent Displays
- ☐ 32 Output Buffers
- ☐ Drives up to 4 Digits
- ☐ Expansion Capability for More Digits
- ☐ Reduced RFI Emanation
- ☐ Wired OR Capability for Higher Current

General Description

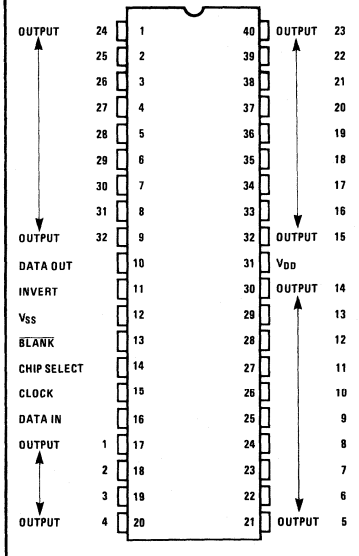
The S2809 Universal Display Driver is a P-channel MOS integrated circuits capable of driving LED, vacuum fluorescent, and liquid crystal displays. Data is clocked serially into a 32-bit master-slave static shift register. This provides static parallel drive to the display segments through display drive buffers. To reduce RFI emanation, capacitors have been integrated on the circuit for reduction of output switching speeds. Serial interconnection of circuits is made possible by the Data Out Output, allowing additional digits to be driven.

Two or more outputs may be wired together for higher sourcing currents; useful in applications such as triac triggering or low voltage incandescent displays. The S2809 can also be used as a parallel output device for μC's such as AMI's S2000 series single chip microcomputer.

Block Diagram



Pin Configuration



AMERICAN MICROSYSTEMS, INC.

S6800

Microprocessor Component Family

Contact factory for complete data sheet

MICROPROCESSORS	
S6800/S68A00/S68B00	8-Bit Microprocessor (1.0/1.5/2.0MHz XTAL)
S68H00	High Speed S6800 (2MHz Clock)
S6801/S6801E	Single Chip Microcomputer 2K ROM, 128×8 RAM, 31 I/O Lines, Enhanced Instruction Set (External [E] or Internal Clock)
S6802/S68A02	Microprocessor with Clock and RAM (1.0/1.5MHz Clock)
S6803/S6803N/R	S6801 Without ROM (N/R Model — No ROM and/or RAM)
S6805	Single Chip Microcomputer 1,152×8 ROM, 64×8 RAM, Clock, Pre-scaler, Bit Level Instructions.
S6808/S68A08	S6800 with Clock (1.0/1.5MHz Clock)
S6809(E)/S68A09(E)/S68B09(E)	Pseudo 16-Bit Microprocessor (1.0/1.5/2.0MHz Clock) (E Models — External Clock Mode)
PERIPHERALS	
S1602	Universal Asynchronous Receiver/Transmitter (UART)
S2350	Universal Synchronous Receiver/Transmitter (USRT)
S6821/S68A21/S68B21	Peripheral Interface Adapter (PIA) (1.0/1.5/2.0MHz Clock)
S68H21	High Speed Peripheral Interface Adapter (PIA) (2.5MHz Clock)
S6840/S68A40/S68B40	Programmable Timer (1.0/1.5/2.0MHz)
S68045	CRT Controller (CRTC)
S6846	2K ROM, Parallel I/O, Programmable Timer
S68047	Video Display Generator (VDG)
S6850/S68A50/S68B50	Asynchronous Communication Interface Adapter 800 Bus Compatible
S6852/S68A52/S68B52	Asynchronous Communication Interface (1.0/1.5/2.0MHz Clock) (ACIA)
S6854/S68A54/S68B54	Advanced Data Link Controller (ADLC) (1.0/1.5/2.0MHz Clock)
S68488	IEEE — 488 Bus Interface
S6894	Data Encryption Unit (DEU)
S2811	Signal Processing Peripheral
S2814A	Fast Fourier Transformer
MEMORIES	
S6810/S68A10/S68B10	128×8 Static RAM (450/360/20ns Access Time)
S6810-1	Low Cost S6810 (575ns Access Time)

AMERICAN MICROSYSTEMS, INC.

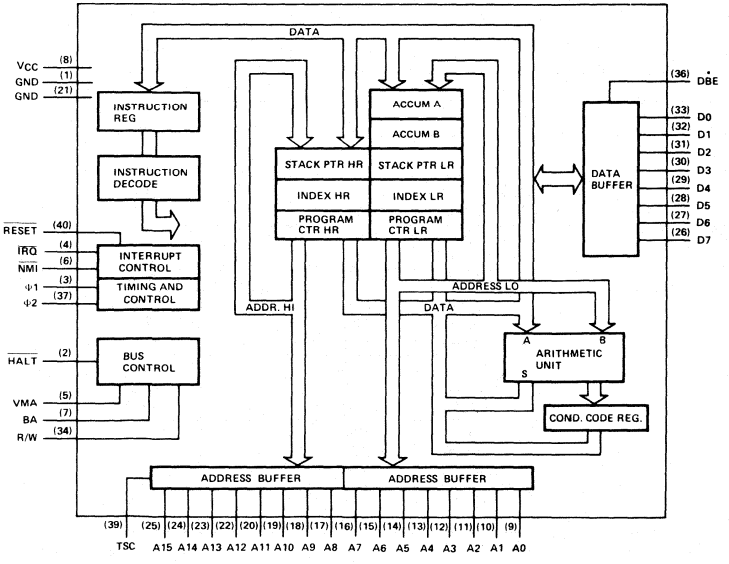
S6800/S68A00/S68B00

8-BIT MICROPROCESSOR

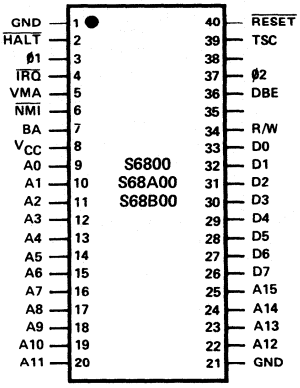
Features

- ☐ Eight-Bit Parallel Processing
- ☐ Bi-Directional Data Bus
- ☐ Sixteen-Bit Address Bus – 65536 Bytes of Addressing
- ☐ 72 Instructions – Variable Length
- ☐ Seven Addressing Modes – Direct, Relative Immediate, Indexed, Extended, Implied and Accumulator
- ☐ Variable Length Stack
- ☐ Vectored Restart
- ☐ 2 Microsecond Instruction Execution
- ☐ Maskable Interrupt Vector
- ☐ Separate Non-Maskable Interrupt – Internal Registers Saved in Stack
- ☐ Six Internal Registers – Two Accumulators, Index Register, Program Counter, Stack Pointer and Condition Code Register
- ☐ Direct Memory Access (DMA) and Multiple Processor Capability
- ☐ Clock Rates – S6800 – 1.0MHz
  – S68A00 – 1.5MHz
  – S68B00 – 2.0MHz
- ☐ Simple Bus Interface Without TTL
- ☐ Halt and Single Instruction Execution Capability

Block Diagram



Pin Configuration



Absolute Maximum Ratings

Supply Voltage V_{CC}	− 0.3 to + 7.0V
Input Voltage V_{IN}	− 0.3V to + 7.0V
Operating Temperature Range T_A	0°C to + 70°C
Storage Temperature Range T_{stg}	− 55°C to + 150°C

Electrical Characteristics

(V_{CC} = 5.0V, ± 5%, V_{SS} = 0, T_A unless otherwise noted.)

Symbol	Characteristics		Min.	Typ.	Max.	Unit
V_{IH} V_{IHC}	Input High Voltage (Normal Operating Levels)	Logic $\phi1, \phi2$	V_{SS} + 2.0 V_{CC} − 0.6	− −	V_{CC} V_{CC} + 0.3	Vdc
V_{IL} V_{ILC}	Input Low Voltage (Normal Operating Levels)	Logic $\phi1, \phi2$	V_{SS} − 0.3 V_{SS} − 0.3	− −	V_{SS} + 0.8 V_{SS} + 0.4	Vdc
I_{IN}	Input Leakage Current (V_{IN} = 0 to 5.25V, V_{CC} = Max) (V_{IN} = 0 to 5.25V, V_{CC} = 0.0V)	Logic* $\phi1, \phi2$	− −	1.0 −	2.5 100	μAdc
I_{TSI}	Three-State (Off State) Input Current V_{IN} = 0.4 to 2.4V, V_{CC} = Max	D0 − D7 A0 − A15, R/W	− −	2.0 −	10 100	μAdc
V_{OH}	Output High Voltage (I_{LOAD} = 205μAdc, V_{CC} = Min) (I_{LOAD} = 145μAdc, V_{CC} = Min) (I_{LOAD} = − 100μAdc, V_{CC} = Min)	D0 − D7 A0 − A15, R/W, VMA BA	V_{SS} + 2.4 V_{SS} + 2.4 V_{SS} + 2.4	− −	− −	Vdc
V_{OL}	Output Low Voltage (I_{LOAD} 1.6mAdc, V_{CC} = Min)		−	−	V_{SS} + 0.4	Vdc
P_D	Power Dissipation		−	0.5	1.0	W
C_{IN}	Capacitance# (V_{IN} = 0, T_A = 25°C, f = 1.0MHz)	$\phi1$ $\phi2$ D0 − D7 Logic Inputs	− − − −	− − 10 6.5	35 70 12.5 10	pF
C_{OUT}		A0 − A15, R/W, VMA	−	−	12	pF
f	Frequency of Operation	S6800 S68A00 S68B00	0.1 0.1 0.1	− − −	1.0 1.5 2.0	MHz
t_{CYC}	Clock Timing (Figure 1) Cycle Time	S6800 S68A00 S68B00	1.000 0.666 0.50	− − −	10 10 10	μs
$PW_{\phi H}$	Clock Pulse Width Measured at V_{CC} − 0.6V	$\phi1, \phi2$ − S6800 $\phi1, \phi2$ − S68A00 $\phi1, \phi2$ − S68B00	400 230 800	− − −	9500 9500 9500	ns ns
t_{UT}	Total $\phi1$ and $\phi2$ Up Time	S6800 S68A00 S68B00	900 600 440	− − −	− − −	ns
$t_{\phi r}, t_{\phi f}$	Measured between V_{SS} + 0.4 and V_{CC} − 0.6	Rise and Fall Times	5.0	−	100	ns
t_d	Measured at V_{OV} = V_{SS} + 0.6V	Delay Time or Clock Separation	0	−	9100	ns

**Except $\overline{IRQ}$ and $\overline{NMI}$, Which require KΩ pullup load resistor for wire-OR capability at optimum operation.*
#Capacitances are periodically sampled rather than 100% tested.

Read/Write Timing

Symbol	Characteristics	S6800			S68A00			S68B00			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{AD}	Address Delay										ns
	C = 90pF	–	–	270	–	–	180	–	–	150	
	C = 30pF	–	–	250	–	–	165	–	–	135	
t_{ACC}	Periph. Read Access Time $t_{AC} = t_{UT} - (t_{AD} + t_{DSR})$	–	–	530	–	–	360	–	–	250	ns
t_{DSR}	Data Setup Time (Read)	100	–	–	60	–	–	40	–	–	ns
t_H	Input Data Hold Time	10	–	–	10	–	–	10	–	–	ns
t_H	Output Data Hold Time	10	25	–	10	25	–	10	25	–	ns
t_{AH}	Address Hold Time (Address, R/W, VMA)	30	50	–	10	75	–	10	75	–	ns
t_{EH}	Enable High Time for DBE Input	450	–	–	280	–	–	220	–	–	ns
t_{DDW}	Date Delay Time (Write)	–	–	225	–	165	200	–	–	160	ns
	Processor Controls										
t_{PCS}	Proc. Control Setup Time	200	–	–	200	–	–	200	–	–	ns
t_{PCr};t_{PCf}	Processor Control Rise and Fall Time	–	–	100	–	–	100	–	–	100	ns
t_{BA}	Bus Available Delay	–	–	250	–	–	270	–	–	270	ns
t_{TSE}	Three-State Enable	–	–	270	–	–	40	–	–	40	ns
t_{TSD}	Three-State Delay	–	–	–	–	–	270	–	–	270	ns
$t_{\overline{DBE}}$	Data Bus Enable Down Time During $\phi 1$ Up Time	150	–	–	150	–	–	70	–	–	ns
t_{DBEr}, t_{DBEf}	Data Bus Enable Rise and Fall Times	–	–	25	–	–	25	–	–	25	ns

Measurement point for $\phi 1$ and $\phi 2$ are shown below. Other measurements are the same as for MC6800.

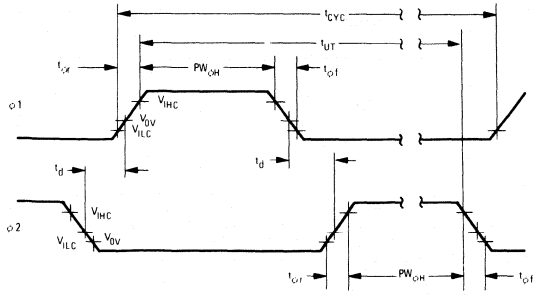


Figure 1. Clock Timing Waveform

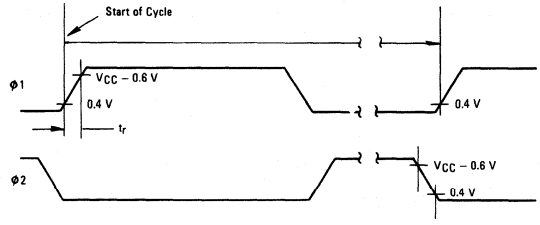


Figure 2. Read/Write Timing Waveform

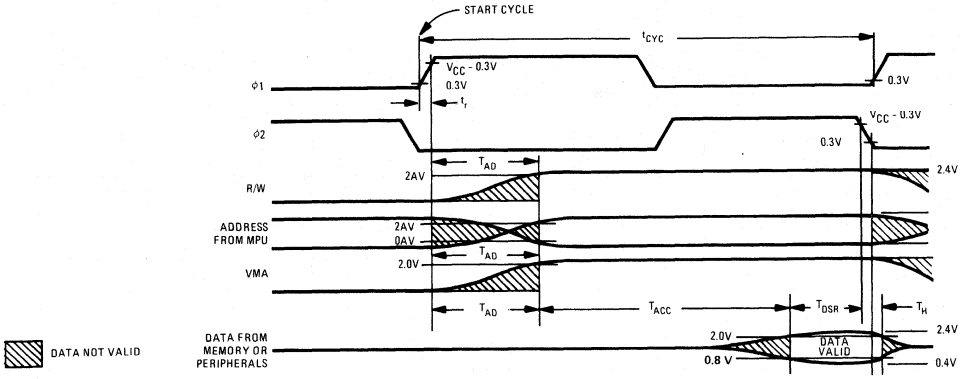


Figure 3. Read Data From Memory or Peripherals

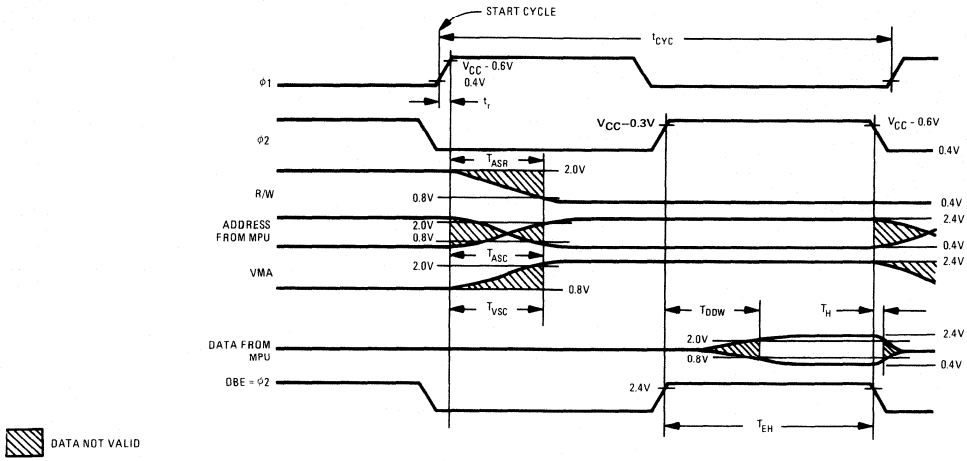


Figure 4. Write Data In Memory or Peripherals

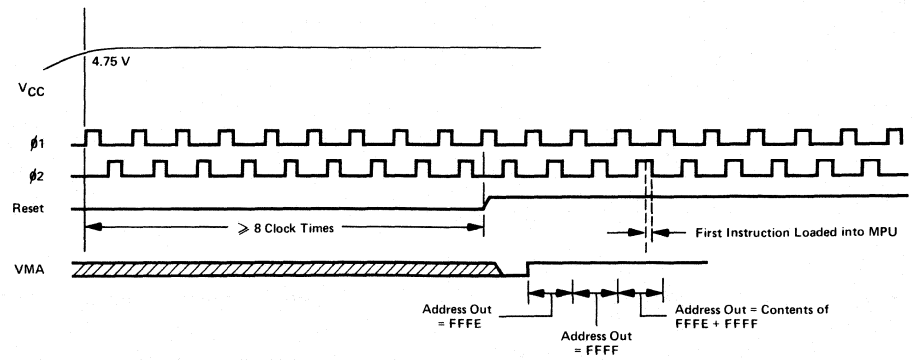


Figure 5. Initialization of MPU After Restart

Interface Description

Label	Pin	Function
ϕ1 ϕ2	(3) (37)	**Clocks Phase One and Phase Two** — Two pins are used for a two-phase non-overlapping clock that runs at the V_{CC} voltage level.
$\overline{\text{RESET}}$	(40)	**$\overline{\text{Reset}}$** — this input is used to reset and start the MPU from a power down condition, resulting from a power failure or an initial start-up of the processor. If a positive edge is detected on the input, this will signal the MPU to begin the restart sequence. This will start execution of a routine to initialize the processor from its reset condition. All the higher order address lines will be forced high. For the restart, the last two (FFFE, FFFF) locations in memory will be used to load the program that is addressed by the program counter. During the restart routine, the interrupt mask bit is set and must be reset before the MPU can be interrupted by $\overline{\text{IRQ}}$. $\overline{\text{Reset}}$ must be held low for at least eight clock periods after V_{CC} reaches 4.75 volts (Figure 4). If $\overline{\text{Reset}}$ goes high prior to the leading edge of ϕ2, on the next ϕ1 the first restart memory vector address (FFFE) will appear on the address lines. This location should contain the higher order eight bits to be stored into the program counter. Following, the next address FFFF should contain the lower order eight bits to be stored into the program counter.
VMA	(5)	**Valid Memory Address** — This output indicates to peripheral devices that there is a valid address on the address bus. In normal operation, this signal should be utilized for enabling peripheral interfaces such as the PIA and ACIA. This signal is not three-state. One standard TTL load and 30pF may be directly driven by this active high signal.
A0 • • • A15	(9) (25)	**Address Bus** — Sixteen pins are used for the address bus. The outputs are three-state bus drivers capable of driving one standard TTL load and 130pF. When the output is turned off, it is essentially an open circuit. This permits the MPU to be used in DMA applications.
TSC	(39)	**Three-State Control** — This input causes all of the address lines and the Read/Write line to go into the off or high impedance state. This state will occur 500ns after TSC = 2.4V. The Valid Memory Address and Bus Available signals will be forced low. The data bus is not affected by TSC and has its own enable (Data Bus Enable). In DMA applications, the Three-State Control line should be brought high on the leading edge of the Phase One Clock. The ϕ1 clock must be held in the high state and the ϕ2 in the low state for this function to operate properly. The address bus will then be available for other devices to directly address memory. Since the MPU is a dynamic device, it can be held in this state for only 50μs or destruction of data will occur in the MPU.
D0 • • D7	(33) (26)	**Data Bus** — Eight pins are used for the data bus. It is bi-directional, transferring data to and from the memory and peripheral devices. It also has three-state output buffers capable of driving one standard TTL load at 130pF.
DBE	(36)	**Data Bus Enable** — This input is the three-state control signal for the MPU data bus and will enable the bus drivers when in the high state. This input is TTL compatible; however in normal operation, it can be driven by the phase two clock. During an MPU read cycle, the data bus drivers will be disabled internally. When it is desired that another device control the data bus such as in Direct Memory Access (DMA) applications, DBE should be held low.
R/W	(34)	**Read/Write** — This TTL compatible output signals the peripherals and memory devices whether the MPU is in a Read (high) or Write (low) state. The normal standby state of this

signal is Read (high). Three-State Control going high will Read/Write to the off (high-impedance) state. Also, when the processor is halted, it will be in the off state. This output is capable of driving one standard TTL load and 130pF.

$\overline{HALT}$ (2) **$\overline{Halt}$** — When this input is in the low state, all activity in the machine will be halted. This input is level sensitive. In the halt mode, the machine will stop at the end of an instruction. Bus Available will be at a one level, Valid Memory Address will be at a zero, and all other three-state lines will be in the three-state mode.

Transition of the $\overline{Halt}$ line must not occur during the last 250ns of phase one. To insure single instruction operation, the $\overline{Halt}$ line must go high for one Phase One Clock cycle.

BA (7) **Bus Available** — The Bus Available signal will normally be in the low state; when activated, it will go to the high state indicating that the microprocessor has stopped and that the address bus is available. This will occur if the $\overline{Halt}$ line is in the low state or the processor is in the WAIT state as a result of the execution of a WAIT instruction. At such time, all three-state output drivers will go to their off state and other outputs to their normally inactive level. The processor is removed from the WAIT state by the occurrence of a maskable (mask bit I = 0) or nonmaskable interrupt. This output is capable of driving one standard TTL load and 30pF.

$\overline{IRQ}$ (4) **$\overline{Interrupt\ Request}$** — This level sensitive input requests that an interrupt sequence be generated within the machine. The processor will wait until it completes the current instruction that is being executed before it recognizes the request. At that time, if the interrupt mask bit in the Condition Code Register is not set, the machine will begin an interrupt sequence. The Index Register, Program Counter, Accumulators, and Condition Code Register are stored away on the stack. Next the MPU will respond to the interrupt request by setting the interrupt mask bit high so that no further interrupts may occur. At the end of the cycle, a 16-bit address will be loaded that points to a vectoring address which is located in memory locations FFF8 and FFF9. An adress loaded at these locations causes the MPU to branch to an interrupt routine in memory.

The $\overline{Halt}$ line must be in the high state for interrupts to be recognized.

The $\overline{IRQ}$ has a high impedance pullup device internal to the chip; however a 3kΩ external resistor to V_{CC} should be used for wire-OR and optimum control of interrupts.

$\overline{NMI}$ (6) **$\overline{Non\text{-}Maskable\ Interrupt}$**— A low-going edge on this input requests that a non-mask interrupt sequence be generated within the processor. As with the $\overline{Interrupt\ Request}$ signal, the processor will complete the current instruction that is being executed before it recognizes the $\overline{NMI}$ signal. The interrupt mask bit in the Condition Code Register has no effect on $\overline{NMI}$. The Index Register, Program Counter, Accumulators, and Condition Code Register are stored away in the stack. At the end of the cycle, a 16-bit address will be loaded that points to a vectoring address which is located in memory locations FFFC and FFFD. An address loaded at these locations causes the MPU to branch to a non-maskable interrupt routine in memory.

$\overline{NMI}$ has a high impedance pullup resistor internal to the chip; however a 3kΩ external resistor to V_{CC} should be used for wire-OR and optimum control of interrupts.

Inputs $\overline{IRQ}$ and $\overline{NMI}$ are hardware interrupt lines that are acknowledged during $\phi 2$ and will start the interrupt routine on the $\phi 1$ following the completion of an instruction.

INTERRUPTS — As outlined in the interface description the S6800 requires a 16-bit vector address to indicate the location of routines for Restart, Non-maskable Interrupt, and Maskable Interrupt. Additionally an address is required for the Software Interrupt Instruc-

tion (SWI). The processor assumes the uppermost eight memory locations, FFF8 – FFFF, are assigned as interrupt vector addresses as defined in Figure 6.

After completing the current instruction execution the processor checks for an allowable interrupt request via the $\overline{IRQ}$ or $\overline{NMI}$ inputs as shown by the simplified flow chart in Figure 7. Recognition of either external interrupt request or a Wait for Interrupt (WAI) or Software Interrupt (SWI) instruction causes the contents of the Index Register, Program Counter, Accumulators and Condition Code Register to be transferred to the stack as shown in Figure 8.

Vector MS	Vector LS	Description
FFFE	FFFF	Restart
FFFC	FFFD	Non-maskable Interrupt
FFFA	FFF9	Interrupt Request

Figure 6. Memory Map For Interrupt Vectors

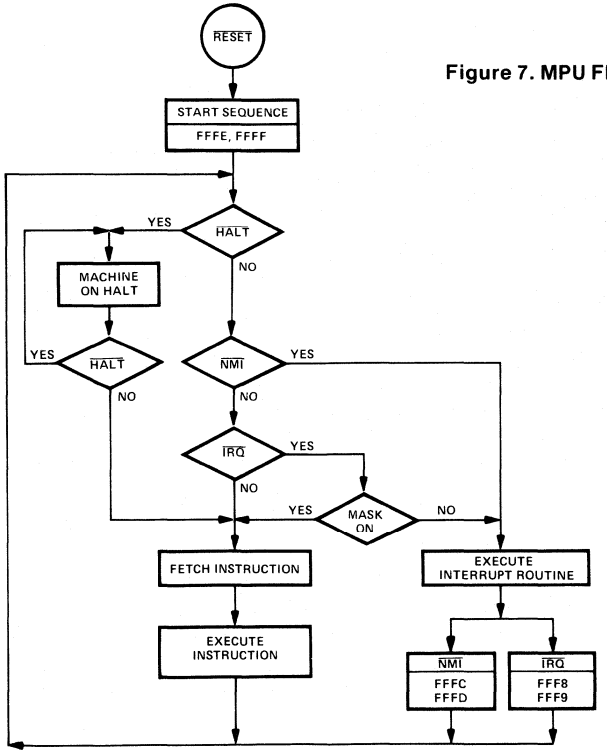


Figure 7. MPU Flow Chart

SP = Stack Pointer
CC = Condition Codes (Also called the Processor Status Byte)
ACCB = Accumulator B
ACCA = Accumulator A
IXH = Index Register, Higher Order 8 Bits
IXL = Index Register, Lower Order 8 Bits
PCH = Program Counter, Higher Order 8 Bits
PCL = Program Counter, Lower Order 8 Bits

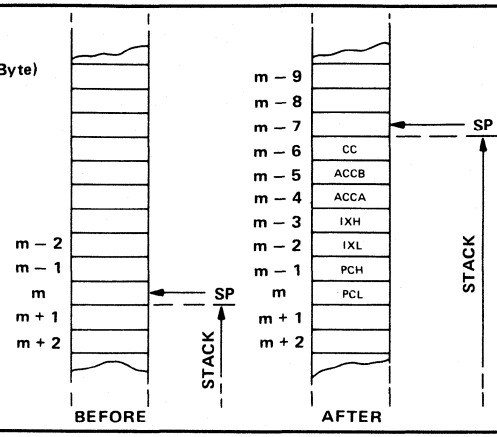


Figure 8. Saving The Status Of The Microprocessor In The Stack

MPU Registers

The MPU has three 16-bit registers and three 8-bit registers available for use by the programmer.

Program Counter – The program counter is a two byte (16-bits) register that points to the current program address.

Stack Pointer – The stack pointer is a two byte register that contains the address of the next available location in an external push-down/pop-up stack. This stack is normally a random access Read/Write memory that may have any location (address) that is convenient. In those applications that require storage of information in the stack when power is lost, the stack must be non-volatile.

Index Register – The index register is a two byte register that is used to store data or a sixteen bit memory address for the Indexed mode of memory addressing.

Accumulators – The MPU contains two 8-bit accumulators that are used to hold operands and results from the arithmetic logic unit (ALU).

Condition Code Register – The condition code register indicates the results of an Arithmetic Logic Unit operation: Negative (N), Zero (Z), Overflow (V), Carry from bit 7 (C), and half carry from bit 3 (H). These bits of the Condition Code Register are used as testable conditions for the conditional branch instructions. Bit 4 is the interrupt mask bit (I). The unused bits of the Condition Code Register (b6 and b7) are ones.

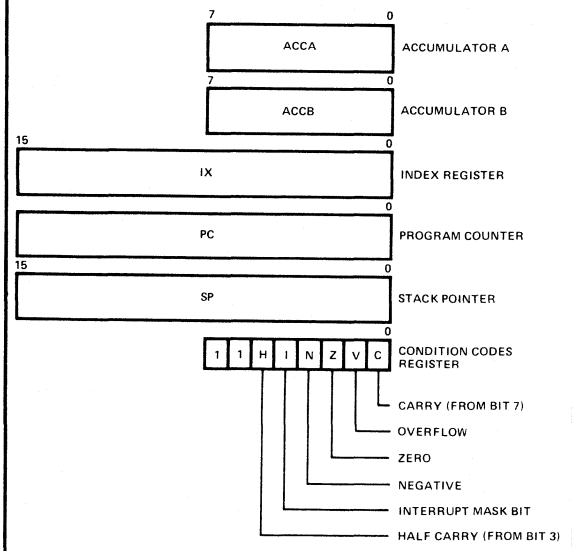


Figure 9. Programming Model of the Microprocessor

MPU Addressing Modes

The S6800 eight-bit microprocessing unit has seven address modes that can be used by a programmer, with the addressing mode a function of both the type of instruction and the coding within the instruction. A summary of the addressing modes for a particular instruction can be found in Figure 10 along with the associated instruction execution time that is given in machine cycles. With a clock frequency of 1 MHz, these times would be microseconds.

Accumulator Addressing (ACCX)

OP CODE

A single byte instruction addressing operands only in accumulator A or accumulator B.

Implied Addressing

OP CODE

Single byte instruction where the operand address is implied by instruction definition (i.e., Stack Pointer, Index Register or Condition Register).

Immediate Addressing

OP CODE	OPERAND

HIGHER	OPERAND	OPERAND LOWER

Two or three byte instructions with an eight or sixteen bit operand respectively. For accumulator operations the eight bit operand is contained in the second byte of a two byte instruction. For Index Register operations (e.g. LDX) sixteen bit operand is contained in the second and third byte of a three byte instruction.

Direct Addressing

OP CODE	ADDRESS 0-255

Two byte instructions with the address of the operand contained in the second byte of the instruction. This format allows direct addressing of operands within the first 256 memory locations.

Extended Addressing

OP CODE	ADDRESS HIGHER	ADDRESS LOWER

Three byte instructions with the higher eight bits of the operand address contained in the second byte and the lower eight bits of address contained in the third byte of the instruction. This format allows direct addressing of all 65,536 memory locations.

Indexed Addressing

OP CODE	INDEX ADDRESS

Two byte instructions where the 8-bit unsigned address contained in the second byte of the instruction is added to the sixteen bit Index Register resulting in a sixteen bit effective address. The effective address is stored in a temporary register and the contents of the Index Register are unchanged.

Relative Addressing

OP CODE	RELATIVE ADDRESS

Two byte instructions where the relative address contained in the second byte of the instruction is added to the sixteen bit program counter plus two. The relative address is interpreted as a two's complement number allowing relative addressing within a range of – 126 to + 129 bytes of the present instruction.

		Addressing Mode							Condition Reg
		Implied	Immediate	Direct	Extended	Indexed	Relative	Boolean/Arith	5 4 3 2 1 0
Instruction	Mnemonic	OP MC PB	OP MC PB	OP MC PB	OP MC PB	OP MC PB	OP MC PB	Operation	H I N Z V C
Load accumulator	LDAA		86 2 2	96 3 2	B6 4 3	A6 5 2		M → A	• • ↕ ↕ R •
	LDAB		C6 2 2	D6 3 2	F6 4 3	E6 5 2		M → B	• • ↕ ↕ R •
Load stack pointer	LDS		8E 3 3	9E 4 2	BE 5 3	AE 6 2		M → SP_H, (M + 1) → SP_L	• • 9 ↕ R •
Load index register	LDX		CE 3 3	DE 4 2	FE 5 3	EE 6 2		M → X_H, (M + 1) → X_L	• • 9 ↕ R •
Store accumulator	STAA			97 4 2	B7 5 3	A7 6 2		A → M	• • ↕ ↕ R •
	STAB			D7 4 2	F7 5 3	E7 6 2		B → M	• • ↕ ↕ R •
Store stack pointer	STS			9F 5 2	BF 6 3	AF 7 2		SP_H → M, SP_L → (M + 1)	• • 9 ↕ R •
Store index register	STX			DF 5 2	FF 6 3	EF 7 2		X_H → M, X_L → (M + 1)	• • 9 ↕ R •
Transfer accumulators	TAB	16 2 1						A → B	• • ↕ ↕ R •
	TBA	17 2 1						B → A	• • ↕ ↕ R •
Transfer Acc. to cond. reg.	TAP	06 2 1						A → CCR	Note 12
Transfer cond. reg. to Acc.	TPA	07 2 1						CCR → A	• • • • • •
Transfer stck ptr to index	TSX	30 4 1						SP + 1 → X	• • • • • •
Transfer index to stck ptr	TXS	35 4 1						X − 1 → SP	• • • • • •
Pull data	PULA	32 4 1						SP + 1 → SP, M_{SP} → A	• • • • • •
	PULB	33 4 1						SP + 1 → SP, M_{SP} → B	• • • • • •
Push data	PSHA	36 4 1						A → M_{SP}, SP − 1 → SP	• • • • • •
	PSHB	37 4 1						B → M_{SP}, SP − 1 → SP	• • • • • •
Add accumulators	ABA	1B 2 1						A + B → A	↕ • ↕ ↕ ↕ ↕
Add	ADDA		8B 2 2	9B 3 2	BB 4 3	AB 5 2		A + M → A	↕ • ↕ ↕ ↕ ↕
	ADDB		CB 2 2	DB 3 2	FB 4 3	EB 5 2		B + M → B	↕ • ↕ ↕ ↕ ↕
Add with carry	ADCA		89 2 2	99 3 2	B9 4 3	A9 5 2		A + M + C → A	↕ • ↕ ↕ ↕ ↕
	ADCB		C9 2 2	D9 3 2	F9 4 3	E9 5 2		B + M + C → B	↕ • ↕ ↕ ↕ ↕
Subtract accumulators	SBA	10 2 1						A − B → A	• • ↕ ↕ ↕ ↕
Subtract	SUBA		80 2 2	90 3 2	B0 4 3	A0 5 2		A − M → A	• • ↕ ↕ ↕ ↕
	SUBB		C0 2 2	D0 3 2	F0 4 3	E0 5 2		B − M → B	• • ↕ ↕ ↕ ↕
Subtract with carry	SBCA		82 2 2	92 3 2	B2 4 3	A2 5 2		A − M − C → A	• • ↕ ↕ ↕ ↕
	SBCB		C2 2 2	D2 3 2	F2 4 3	E2 5 2		B − M − C → B	• • ↕ ↕ ↕ ↕
Increment	INCA	4C 2 1						A + 1 → A	• • ↕ ↕ 5 •
	INCB	5C 2 1						B + 1 → B	• • ↕ ↕ 5 •
	INC				7C 6 3	6C 7 2		M + 1 → M	• • ↕ ↕ 5 •
Increment stack pointer	INS	31 4 1						SP + 1 → SP	• • • • • •
Increment index reg.	INX	08 4 1						X + 1 → X	• • • ↕ • •
Decrement	DECA	4A 2 1						A − 1 → A	• • ↕ ↕ 4 •
	DECB	5A 2 1						B − 1 → B	• • ↕ ↕ 4 •
	DEC				7A 6 3	6A 7 2		M − 1 → M	• • ↕ ↕ 4 •
Decrement stack pointer	DES	34 4 1						SP − 1 → SP	• • • • • •
Decrement index register	DEX	09 4 1						X − 1 → X	• • • ↕ • •
Complement (1's)	COMA	43 2 1						$\overline{A}$ → A	• • ↕ ↕ R S
	COMB	53 2 1						$\overline{B}$ → B	• • ↕ ↕ R S
	COM				73 6 3	63 7 2		$\overline{M}$ → M	• • ↕ ↕ R S
Complement (2's)	NEGA	40 2 1						00 − A → A	• • ↕ ↕ 1 2
	NEGB	50 2 1						00 − B → B	• • ↕ ↕ 1 2
	NEG				70 6 3	60 7 2		00 − M → M	• • ↕ ↕ 1 2
Decimal adjust accumulator	DAA	19 2 1							• • ↕ ↕ ↕ 3

OP = Operation Code MC = Number of MPU Cycles PB = Number of Program Bytes

Figure 10. S6800 Instruction Set

Instruction	Mnemonic	Addressing Mode: Implied OP MC PB	Immediate OP MC PB	Direct OP MC PB	Extended OP MC PB	Indexed OP MC PB	Relative OP MC PB	Boolean/Arith Operation	Condition Reg 5 | 4 | 3 | 2 | 1 | 0 — H | I | N | Z | V | C
Logical and	ANDA		84 2 2	94 3 2	B4 4 3	A4 5 2		A • M → A	• • ‡ ‡ R •
	ANDB		C4 2 2	D4 3 2	F4 4 3	E4 5 2		B • M → B	• • ‡ ‡ R •
Inclusive or	ORAA		8A 2 2	9A 3 2	BA 4 3	AA 5 2		A + M → A	• • ‡ ‡ R •
	ORAB		CA 2 2	DA 3 2	FA 4 3	EA 5 2		B + M → B	• • ‡ ‡ R •
Exclusive or	EORA		88 2 2	98 3 2	B8 4 3	A8 5 2		A ⊕ M → A	• • ‡ ‡ R •
	EORB		C8 2 2	D8 3 2	F8 4 3	E8 5 2		B ⊕ M → B	• • ‡ ‡ R •
Shift left arithmetic	ASLA	48 2 1						A, B, M { C b7 b0 }	• • ‡ ‡ 6 ‡
	ASLB	58 2 1							• • ‡ ‡ 6 ‡
	ASL				78 6 3	68 7 2			• • ‡ ‡ 6 ‡
Shift right arithmetic	ASRA	47 2 1						A, B, M { b7 b0 C }	• • ‡ ‡ 6 ‡
	ASRB	57 2 1							• • ‡ ‡ 6 ‡
	ASR				77 6 3	67 7 2			• • ‡ ‡ 6 ‡
Shift right logical	LSRA	44 2 1						A, B, M { 0 b7 b0 C }	• • R ‡ 6 ‡
	LSRB	54 2 1							• • R ‡ 6 ‡
	LSR				74 6 3	64 7 2			• • R ‡ 6 ‡
Rotate left	ROLA	49 2 1						A, B, M { C b7 b0 }	• • ‡ ‡ 6 ‡
	ROLB	59 2 1							• • ‡ ‡ 6 ‡
	ROL				79 6 3	69 7 2			• • ‡ ‡ 6 ‡
Rotate right	RORA	46 2 1						A, B, M { C b7 b0 }	• • ‡ ‡ 6 ‡
	RORB	56 2 1							• • ‡ ‡ 6 ‡
	ROR				76 6 3	66 7 2			• • ‡ ‡ 6 ‡
Compare accumulators	CBA	11 2 1						A − B	• • ‡ ‡ ‡ ‡
Compare	CMPA		81 2 2	91 3 2	B1 4 3	A1 5 2		A − M	• • ‡ ‡ ‡ ‡
	CMPB		C1 2 2	D1 3 2	F1 4 3	E1 5 2		B − M	• • ‡ ‡ ‡ ‡
Compare index register	CPX		8C 3 3	9C 4 2	BC 5 3	AC 6 2		$X_H - M, X_L - (M+1)$	• • 7 ‡ 8 •
Test (zero or minus)	TSTA	4D 2 1						A − 00	• • ‡ ‡ R R
	TSTB	5D 2 1						B − 00	• • ‡ ‡ R R
	TST				7D 6 3	6D 7 2		M − 00	• • ‡ ‡ R R
Bit test	BITA		85 2 2	95 3 2	B5 4 3	A5 5 2		A • M	• • ‡ ‡ R •
	BITB		C5 2 2	D5 3 2	F5 4 3	E5 5 2		B • M	• • ‡ ‡ R •
								TEST	
Branch	BRA						20 4 2		• • • • • •
Branch if carry clear	BCC						24 4 2	C = 0	• • • • • •
Branch if carry set	BCS						25 4 2	C = 1	• • • • • •
Branch if overflow clear	BVC						28 4 2	V = 0	• • • • • •
Branch if overflow set	BVS						29 4 2	V = 1	• • • • • •
Branch if equal to zero	BEQ						27 4 2	Z = 1	• • • • • •
Branch if greater or equal to zero	BGE						2C 4 2	N ⊕ V = 0	• • • • • •
Branch if greater than zero	BGT						2E 4 2	Z + (N ⊕ V) = 0	• • • • • •
Branch if less than zero	BLT						2D 4 2	N ⊕ V = 1	• • • • • •
Branch if less than or equal to zero	BLE						2F 4 2	Z + (N ⊕ V) = 1	• • • • • •
Branch if not equal to zero	BNE						26 4 2	Z = 0	• • • • • •
Branch if minus	BMI						2B 4 2	N = 1	• • • • • •
Branch if plus	BPL						2A 4 2	N = 0	• • • • • •
Branch if higher	BHI						22 4 2	C + Z = 0	• • • • • •
Branch if lower or same	BLS						23 4 2	C + Z = 1	• • • • • •

OP = Operation Code MC = Number of MPU Cycles PB = Number of Program Bytes

Figure 10. S6800 Instruction Set (Cont'd.)

Instruction	Mnemonic	Addressing Modes: Implied OP MC PB	Direct OP MC PB	Immediate OP MC PB	Extended OP MC PB	Indexed OP MC PB	Relative OP MC PB	Boolean/Arith Operation	Condition Reg. 5 4 3 2 1 0 H I N Z V C
Branch to subroutine	BSR						8D 8 2		• • • • • •
Jump to subroutine	JSR				BD 9 3	AD 8 2		See Special Operations	• • • • • •
Jump	JMP				7E 3 3	6E 4 2			• • • • • •
Return from subroutine	RTS	39 5 1							• • • • • •
Return from interrupt	RTI	3B 10 1							Note 10
Software interrupt	SWI	3F 12 1							• S • • • •
Wait for interrupt	WAI	3E 9 1							• 1 • • • •
No operation	NOP	02 2 1						PC + 1 → PC	• • • • • •
Clear	CLRA	4F 2 1						00 → A	• • R S R R
	CLRB	5F 2 1						00 → B	• • R S R R
	CLR				7F 6 3	6F 7 2		00 → M	• • R S R R
Clear carry	CLC	0C 2 1						0 → C	• • • • • R
Clear interrupt mask	CLI	0E 2 1						0 → I	• R • • • •
Clear overflow	CLV	0A 2 1						0 → V	• • • • R •
Set carry	SEC	0D 2 1						1 → C	• • • • • S
Set interrupt mask	SEI	0F 2 1						1 → I	• S • • • •
Set overflow	SEV	0B 2 1						1 → V	• • • • S •

Figure 10. S6800 Instruction Set (Cont'd.)

CONDITION CODE SYMBOLS:

H	Half-carry from bit 3;
I	Interrupt mask
N	Negative (sign bit)
Z	Zero (byte)
V	Overflow, 2's complement
C	Carry from bit 7
R	Reset Always
S	Set Always
↕	Test and set if true, cleared otherwise
•	Not Affected

LEGEND:

OP	Operation Code (Hexadecimal):
MC	Number of MPU Cycles;
PB	Number of Program Bytes;
+	Arithmetic Plus;
−	Arithmetic Minus;
•	Boolean AND;
M_{SP}	Contents of memory location pointed to by Stack Pointer;
+	Boolean Inclusive OR;
⊕	Boolean Exclusive OR;
$\overline{M}$	Complement of M;
→	Transfer Into;
0	Bit = Zero;
00	Byte = Zero;

Note – Accumulator addressing mode instructions are included in the IMPLIED addressing.

CONDITION CODE REGISTER NOTES:

(Bit set if test is true and cleared otherwise)

1	(Bit V)	Test: Result = 10000000?
2	(Bit C)	Test: Result = 00000000?
3	(Bit C)	Test: Decimal value of most significant BCD Character greater than nine? (Not cleared if previously set.)
4	(Bit V)	Test: Operand = 10000000 prior to execution?
5	(Bit V)	Test: Operand = 01111111 prior to execution?
6	(Bit V)	Test: Set equal to result of N ⊕ C after shift has occurred.
7	(Bit N)	Test: Sign bit of most significant (MS) byte = 1?
8	(Bit V)	Test: 2's complement overflow from subtraction of MS bytes?
9	(Bit N)	Test: Result less than zero? (Bit 15 = 1)
10	(All)	Load Condition Code Register from Stack. (See Special Operations)
11	(Bit I)	Set when interrupt occurs, if previously set, a Non-Maskable Interrupt is required to exit the wait state.
12	(ALL)	Set according to the contents of Accumulator A

AMERICAN MICROSYSTEMS, INC.

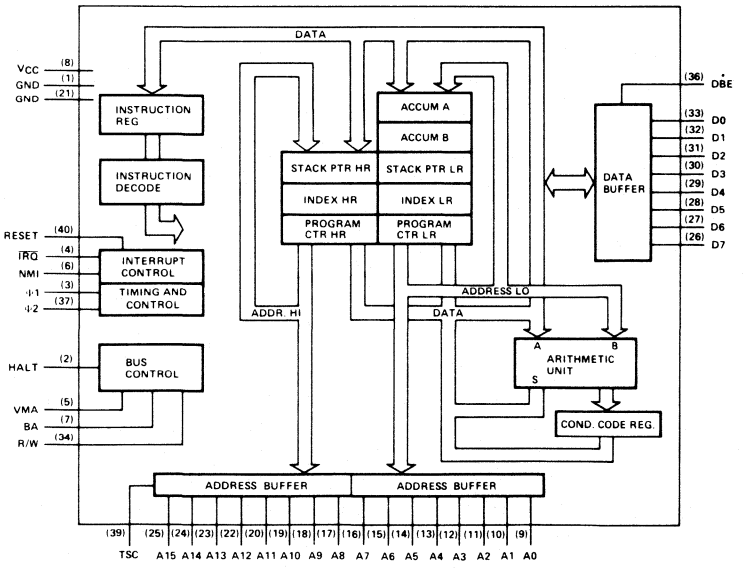
S68H00

8-BIT HIGH SPEED MICROPROCESSOR

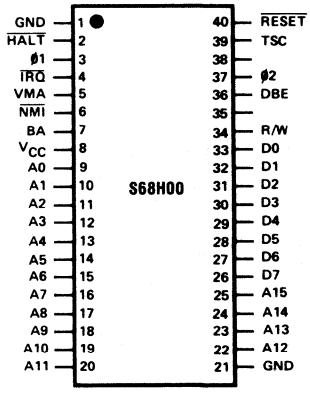
Features

- ☐ Eight-Bit Parallel Processing
- ☐ Bi-Directional Data Bus
- ☐ Sixteen-Bit Address Bus — 65536 Bytes of Addressing
- ☐ 72 Instructions — Variable Length
- ☐ Seven Addressing Modes — Direct, Relative Immediate, Indexed, Extended, Implied and Accumulator
- ☐ Variable Length Stack
- ☐ Vectored Restart
- ☐ 400nsec Instruction Execution
- ☐ Maskable Interrupt Vector
- ☐ Separate Non-Maskable Interrupt — Internal Registers Saved in Stack
- ☐ Six Internal Registers — Two Accumulators, Index Register, Program Counter, Stack Pointer and Condition Code Register
- ☐ Direct Memory Access (DMA) and Multiple Processor Capability
- ☐ Clock Rate 2.5MHz
- ☐ Simple Bus Interface Without TTL
- ☐ Halt and Single Instruction Execution Capability

Block Diagram



Pin Configuration



Absolute Maximum Ratings

Supply Voltage V_{CC}	−0.3 to +7.0V
Input Voltage V_{IN}	−0.3V to +7.0V
Operating Temperature Range T_A	0°C to +70°C
Storage Temperature Range T_{stg}	−55°C to +150°C

Electrical Characteristics

(V_{CC} = 5.0V, ±5%, V_{SS} = 0, T_A unless otherwise noted.)

Symbol	Characteristics		Min.	Typ.	Max.	Unit
V_{IH} V_{IHC}	Input High Voltage (Normal Operating Levels)	Logic φ1, φ2	V_{SS} +2.0 V_{CC} −0.6	— —	V_{CC} V_{CC} +0.3	Vdc
V_{IL} V_{ILC}	Input Low Voltage (Normal Operating Levels)	Logic φ1, φ2	V_{SS} −0.3 V_{SS} −0.3	— —	V_{SS} +0.8 V_{SS} +0.4	Vdc
I_{IN}	Input Leakage Current (V_{IN} = 0 to 5.25V, V_{CC} = Max) (V_{IN} = 0 to 5.25V, V_{CC} = 0.0V)	 Logic* φ1, φ2	 — —	 1.0 —	 2.5 100	μAdc
I_{TSI}	Three-State (Off State) Input Current V_{IN} = 0.4 to 2.4V, V_{CC} = Max	D0 — D7 A0 — A15, R/W	— —	2.0 —	10 100	μAdc
V_{OH}	Output High Voltage (I_{LOAD} = 205μAdc, V_{CC} = Min) (I_{LOAD} = 145μAdc, V_{CC} = Min) (I_{LOAD} = −100μAdc, V_{CC} = Min)	 D0 — D7 A0 — A15, R/W, VMA BA	 V_{SS} +2.4 V_{SS} +2.4 V_{SS} +2.4	 — —	 — —	Vdc
V_{OL}	Output Low Voltage (I_{LOAD} = 1.6mAdc, V_{CC} = Min)		—	—	V_{SS} +0.4	Vdc
P_D	Power Dissipation		—	0.5	1.0	W
C_{IN}	Capacitance# (V_{IN} = 0, T_A = 25°C, f = 1.0MHz)	 φ1 φ2 D0 — D7 Logic Inputs	 — — — —	 — — 10 6.5	 35 70 12.5 10	pF
C_{OUT}		A0 — A15, R/W, VMA	—	—	12	pF
f	Frequency of Operation	S68H00	0.1	—	2.5	MHz
t_{CYC}	Clock Timing (Figure 1) Cycle Time	S68H00	0.4 —	— —	10 10	 μs
$PW_{\phi H}$	Clock Pulse Width Measured at V_{CC} −0.6V	φ1, φ2 — S68H00	165 —	— —	9500 9500	ns ns
t_{UT}	Total φ1 and φ2 Up Time	S68H00	4.20	—	—	ns
$t_{\phi r}$, $t_{\phi f}$	Measured between V_{SS} +0.4 and V_{CC} −0.6	Rise and Fall Times	5.0	—	100	ns
t_d	Measured at V_{OV} = V_{SS} +0.6V	Delay Time or Clock Separation	0	—	9100	ns

**Except $\overline{IRQ}$ and $\overline{NMI}$, Which require KΩ pullup load resistor for wire-OR capability at optimum operation.*

#Capacitances are periodically sampled rather than 100% tested.

Read/Write Timing

Symbol	Characteristics	Min	Typ	Max	Unit
t_{AD}	Address Delay				ns
	C = 90pF	—	—	140	
	C = 30pF	—	—	125	
t_{ACC}	Periph. Read Access Time $t_{AC} = t_{UT} - (t_{AD} + t_{DSR})$	—	—	235	ns
t_{DSR}	Data Setup Time (Read)	35	—	—	ns
t_H	Input Data Hold Time	10	—	—	ns
t_H	Output Data Hold Time	10	25	—	ns
t_{AH}	Address Hold Time (Address, R/W, VMA)	10	75	—	ns
t_{EH}	Enable High Time for DBE Input	205	—		ns
t_{DDW}	Date Delay Time (Write)	—	165	155	ns
	Processor Controls				
t_{PCS}	Proc. Control Setup Time	200	—	—	ns
t_{PCr};t_{PCf}	Processor Control Rise and Fall Time	—	—	100	ns
t_{BA}	Bus Available Delay	—	—	270	ns
t_{TSE}	Three-State Enable	—	—	40	ns
t_{TSD}	Three-State Delay	—	—	270	ns
t_{DBE}	Data Bus Enable Down Time During $\phi 1$ Up Time	65	—	—	ns
t_{DBEr}, t_{DBEf}	Data Bus Enable Rise and Fall Times	—	—	25	ns

S6800

Measurement point for $\phi 1$ and $\phi 2$ are shown below.
Other measurements are the same as for MC6800.

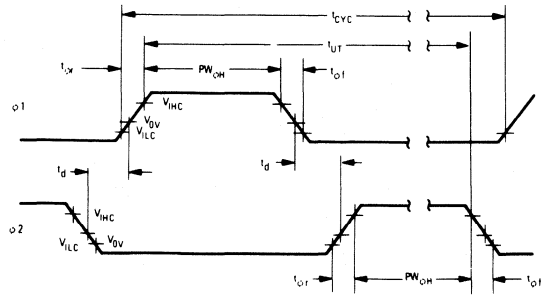


Figure 1. Clock Timing Waveform

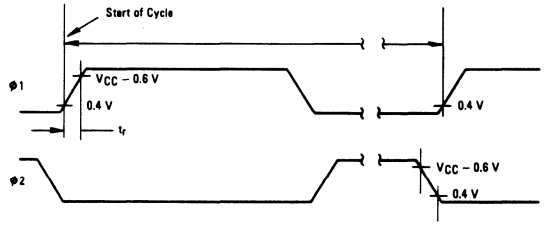


Figure 2. Read/Write Timing Waveform

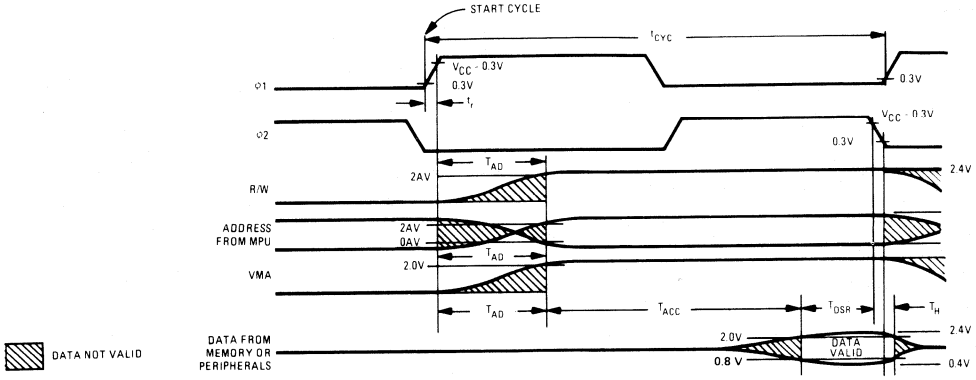


Figure 3. Read Data From Memory or Peripherals

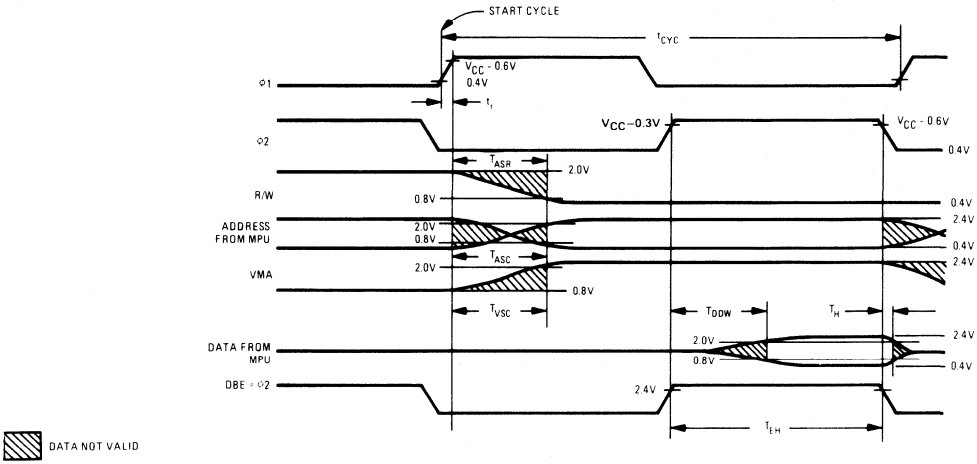


Figure 4. Write Data In Memory or Peripherals

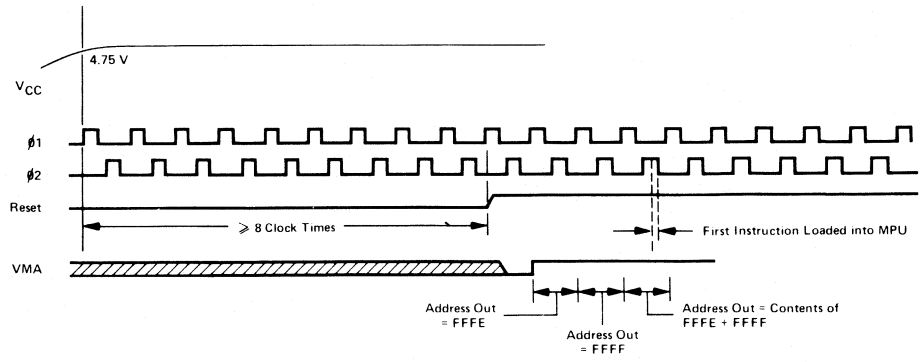


Figure 5. Initialization of MPU After Restart

AMERICAN MICROSYSTEMS, INC.

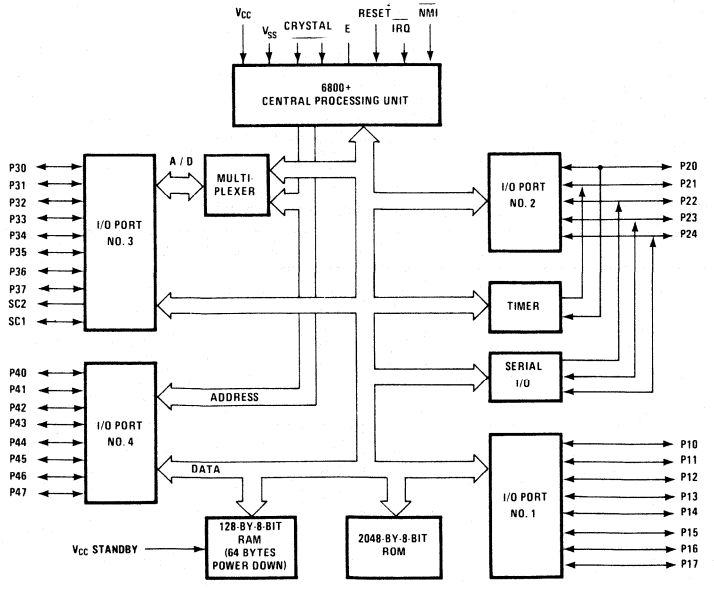
S6801/S6801E

SINGLE CHIP MICROCOMPUTER

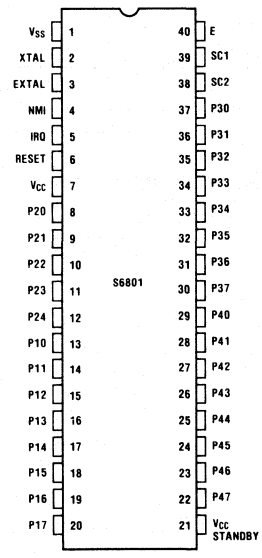
Features

- ☐ Instruction and Addressing Compatible
- ☐ Object Code Compatible
- ☐ 16-Bit Programmable Timer
- ☐ Single Chip or Expandable to 65K Words
- ☐ On-Chip Serial Communications Interface (SCI)
  - — Simplex
  - — Half Duplex
    - — Mark/Space (NRZ)
    - — Biphase (FM)
  - — Port Expansion
    - — Full/Half Duplex
- ☐ Four Internal Baud Rates Available: $\phi 2 \div 16$, 128, 1024, 4096
- ☐ 2K Bytes of ROM
- ☐ 128 Bytes of RAM (64 Bytes Power Down Retainable)
- ☐ 31 Parallel I/O Lines
- ☐ Divide-by-Four Internal Clock
- ☐ Hardware 8×8 Multiply
- ☐ Three Operating Modes
  - — Single Chip
  - — Expanded Multiplex (up to 65K Addressing)
  - — Expanded Non-Multiplex
- ☐ S6801E Operating Modes
  - — Peripheral Controller
  - — Expanded Non-Multiplexed
  - — Expanded Multiplex
- ☐ Expanded Instruction Set
- ☐ Interrupt Capability
- ☐ Low Cost Versions
  - — S6803—No ROM Version
  - — S6803NR—No ROM or RAM
- ☐ TTL-Compatible with Single 5 Volt Supply

Block Diagram



Pin Configuration



General Description

The S6801 MCU is an 8-bit single-chip microcomputer system which is compatible with the S6800 family of parts. The S6801 is object code compatible with the S6800 instruction set.

The S6801 features improved execution times of key S6800 instructions including Jump to Subroutine (JSR) and all Conditioned Branches (BRA, etc.). In addition, several new 16-bit and 8-bit instructions have been added including Push/Pull to/from Stack, Hardware 8×8 Multiply, and store concatenated A and B accumulators (D accumulator).

The S6801 MCU can be operated in three modes: Single-Chip, Expanded Multiplex (up to 65K Byte Addressing), and Expanded Non-Multiplex. In addition, the S6801 is available with two mask options: an on-chip (÷4) Clock, or an external (÷1) Clock. The external mode is especially useful in Multiprocessor Applications. The S6801E can be configured as a peripheral by using the Read/Write (R/$\overline{W}$), Chip Select (CS), and Register Select (RS). The Read/Write line controls the direction of data on Port 3 and the Register Select (RS) allows for access to either Port 3 data register or control register.

The S6801 Serial Communications Interface (SCI) permits full serial communication using no external components in several operating modes—Full and/or Half Duplex operation—and two formats—Standard Mark/Space for typical Terminal/Modem interfaces and the Bi-Phase (FM, F2F, and Manchester) Format primarily for use between processors. Four software addressable registers are provided to configure the Serial Port; to provide status information; and as transmit/receive data buffers.

The S6801 includes a 16-bit timer with three effectively independent timing functions: (1) Variable pulse width measurement, (2) Variable pulse width generation, and (3) A Timer Overflow—Find Time Flag. This makes the S6801 ideal for applications such as Industrial Controls, Automotive Systems, A/D or D/A Converters, Modems, Real-Time Clocks, and Digital Voltage Controlled Oscillators (VCO).

The S6801 is fully TTL-compatible and requires only a single +5 volt supply.

Absolute Maximum Ratings

Supply Voltage, V_{CC}	−0.3V to +7.0V
Input Voltage, V_{IN}	−0.3V to +7.0V
Operating Temperature Range, T_A	0° to +70°C
Storage Temperature Range, T_{stg}	−55°C to +150°C
Thermal Resistance, θ_{JA}	
Plastic	100°C/W
Ceramic	50°C/W

This device contains circuitry to protect the inputs against damage due to high static voltage or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{IN} and V_{OUT} be constrained to the range V_{SS} (V_{IN} or V_{OUT}) V_{DD}.

Electrical Characteristics: $V_{CC}=5.0V\pm5\%$, $V_{SS}=0$, $T_A=T_L$ to T_H unless otherwise noted

Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{IH}	Input High Voltage	$V_{SS}+2.0$		V_{CC}	Vdc
	$\overline{\text{Reset}}$	$V_{SS}+4.0$		V_{CC}	
V_{IL}	Input Low Voltage	$V_{SS}-0.3$		$V_{SS}+0.8$	Vdc
I_{TSI}	Three-State (Off State) Input Current P10-P17		2.0	10	μAdc
I_{TSI}	(V_{IN}=0.4 to 2.4 Vdc) P20-P24, P30-P37		2.0	10	μAdc
V_{OH}	Output High Voltage All Outputs Except XTAL 1 and EXTAL 2 $I_{LOAD}=-200\mu Adc$	$V_{SS}+2.4$			Vdc
V_{OL}	Output Low Voltage All Outputs Except XTAL 1 and EXTAL 2 $I_{LOAD}=1.6mAdc$			$V_{SS}+0.4$	Vdc

Electric Characteristics (Continued)

Symbol	Characteristic	Min.	Typ.	Max.	Unit
P_D	Power Dissipation			1200	mW
C_{IN}	Capacitance $V_{IN}=0$, $T_A=25°C$, f=1.0MHz P10-P17, P20-P24, P40-P47, P30-P37 Reset SC1, SC2, IRQ			 12.5 10 7.5	pF
t_{PDSU}	Peripheral Data Setup Time (Figure 3)	200			ns
t_{PDH}	Peripheral Data Hold Time (Figure 3)	0			ns
t_{OSD1}	Delay Time, Enable negative transition to OS3 Neg. Trans.			1.0	μs
t_{OSD2}	Delay Time, Enable neg. trans. to OS3 positive transition			1.0	μs
t_{PWD}	Delay Time, Enable negative transition to Peripheral Data Valid (Figure 4)			350	ns
t_{CMOS}	Delay Time, Enable negative transition to Peripheral Data Valid ($V_{SS}-30\%$ V_{CC}, P20-P24 (Figure 4)			2.0	μs
I_{OH}	Darlington Drive Current $V_O=1.5$Vdc — P10-P17	−1.0	−2.5	−10	mAdc
V_{SBB} V_{SB}	Standby Voltage (Not Operating) (Operating)	4.00 4.75		5.25 5.25	Vdc

NOTE: The above electricals satisfy Ports 1 and 2 always, and Ports 3 and 4 in the single chip mode only.

Bus Timing (Figure 7)

Symbol	Characteristic	Min.	Typ.	Max.	Unit
t_{CYC}	Cycle Time	1000			ns
P_{WASH}	Address Strobe Pulse Width High	220			ns
t_{ASR}	Address Strobe Rise Time			50	ns
t_{ASF}	Address Strobe Fall Time			50	ns
t_{ASD}	Address Strobe Delay Time	60			ns
t_{ER}	Enable Rise Time			50	ns
t_{EF}	Enable Fall Time			50	ns
P_{WEH}	Enable Pulse Width High Time	450			ns
P_{WEL}	Enable Pulse Width Low Time	450			ns
t_{ASED}	Address Strobe to Enable Delay Time	60			ns
t_{AD}	Address Delay Time			270	ns
t_{DDW}	Data Delay Write Time			225	ns
t_{DSR}	Data Set-up Time	100			ns
t_{HR}	Hold Time Read	20		100	ns
t_{HW}	Hold Time Write	20			ns
t_{ADL}	Address Delay Time for Latch			200	ns
t_{AHL}	Address Hold Time for Latch	20			ns
PW_O	Pulse Width	370	370		ns
t_{AH}	Address Hold Time	20			ns
t_{UT}	Total Up Time	750			ns

MCU Signal Description

This section gives a description of the MCU signals for the various modes. General pin assignments for the signals are shown on page 1. SC1 and SC2 are signals which vary with the mode that the chip is in. Table 1 gives a summary of their function.

Table 1. Mode and Port Summary

MODE	PORT 1 EIGHT LINES	PORT 2 FIVE LINES	PORT 3 EIGHT LINES	PORT 4 EIGHT LINES	SC1	SC2
SINGLE CHIP	I/O	I/O	I/O	I/O	$\overline{IS3(I)}$	$\overline{OS3(O)}$
EXPANDED MUX	I/O	I/O	ADDRESS BUS (A0-A7) DATA BUS D0-D7	ADDRESS BUS* (A8-A15)	AS(O)	R/$\overline{W}$(O)
EXPANDED NON-MUX	I/O	I/O	DATA BUS D0-D7	ADDRESS BUS* (A0-A7)	$\overline{IOS}$(O)	R/$\overline{W}$(O)

*THESE LINES CAN BE SUBSTITUTED FOR I/O (INPUT ONLY) STARTING WITH THE MOST SIGNIFICANT ADDRESS LINE.

I = INPUT
O = OUTPUT
R/$\overline{W}$ = READ/$\overline{WRITE}$
IS = INPUT STROBE
OS = OUTPUT STROBE
IOS = I/O SELECT
SC = STROBE CONTROL
AS = ADDRESS STROBE

Read/Write Timing for Ports 3 and 4 (Figures 1-2)

Symbol	Characteristic	Min.	Typ.	Max.	Unit
t_{AD}	Address Delay			270	ns
t_{ACC}	Peripheral Read Access Time $t_{ACC}=t_{UT}-(t_{AD}+t_{DSR})$			530	ns
t_{DSR}	Data Setup Time (Read)	100			ns
t_{HR}	Input Data Hold Time	10			ns
t_{HW}	Output Data Hold Time	20			ns
t_{AH}	Address Hold Time (Address, R/W)	20			ns
t_{DDW}	Data Delay Time (Write)		165	225	ns
t_{PCS}	Processor Controls				
	Processor Control Setup Time	200			ns
t_{PCr}, t_{PCf}	Processor Control Rise and Fall Time (Measured between 0.8V and 2.0V)			100	ns

Port 3 Strobe Timing (Figures 5-6)

Symbol	Characteristic	Min.	Typ.	Max.	Unit
t_{DSD1}	Output Strobe Delay 1			100	μs
t_{OSD2}	Output Strobe Delay 2			100	μs
PW_{IS}	Input Strobe Pulse Width	200			ns
t_{IH}	Input Data Hold Time	20			ns
t_{IS}	Input Data Setup Time	100			ns

Figure 1. Read Data From Memory or Peripherals Expanded Non-Multiplexed

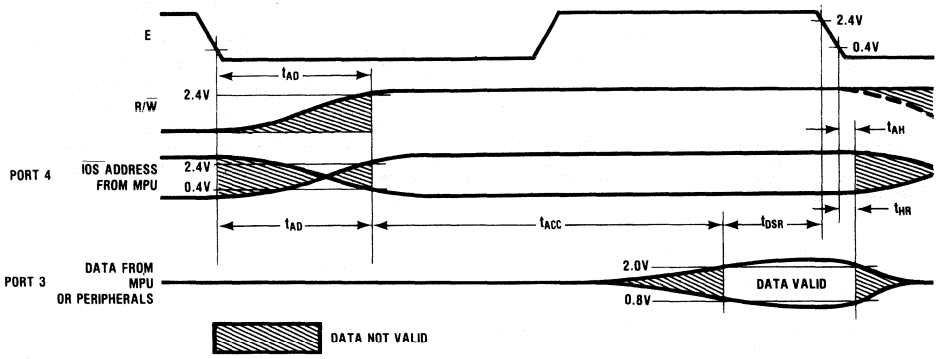
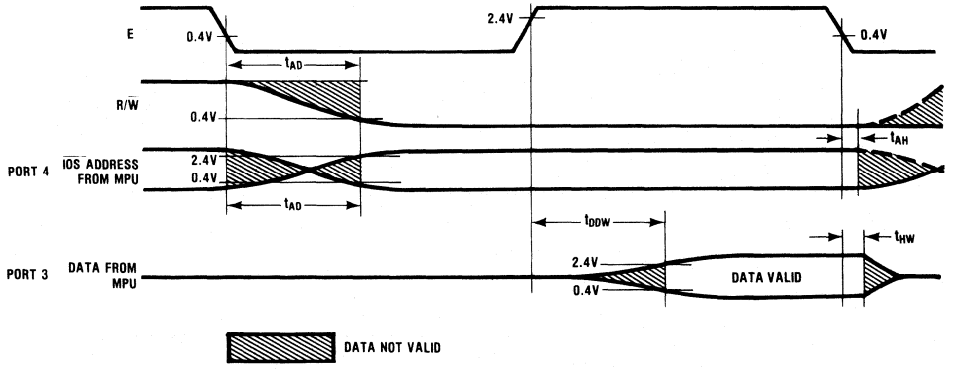


Figure 2. Write Data In Memory or Peripherals Expanded Non-Multiplexed



Ports 1 and 2, and Ports 3 and 4 in the Single Chip Mode

Figure 3. Peripheral Data Setup and Hold Times (Read Mode)

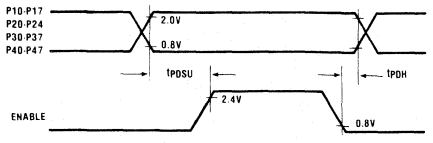


Figure 4. Peripheral CMOS Data Delay Times (Write Mode)

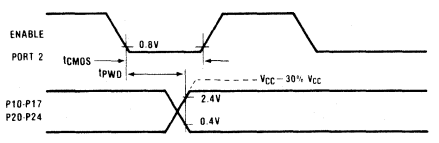


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Figure 5. Output Strobe Timing — Single Chip Mode

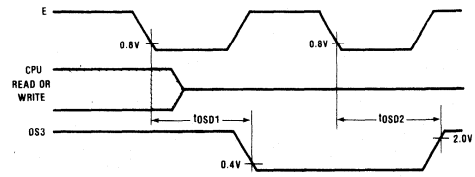


Figure 6. Input Strobe Timing — Single Chip Mode

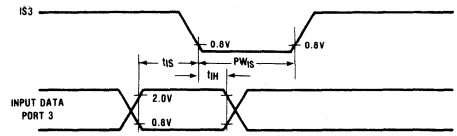


Figure 7. Multiplexed Bus Timing

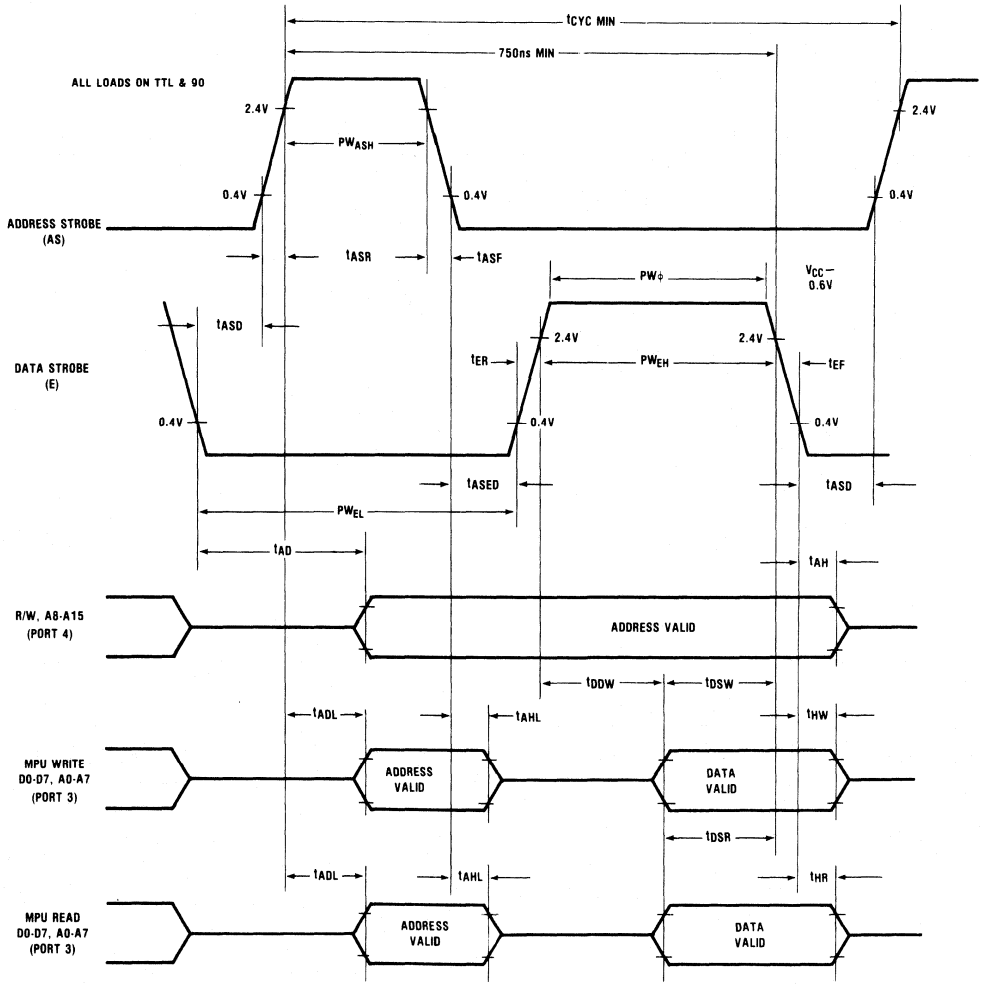


Figure 8. CMOS Load

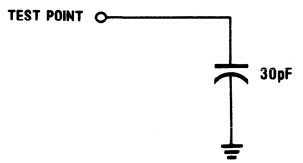
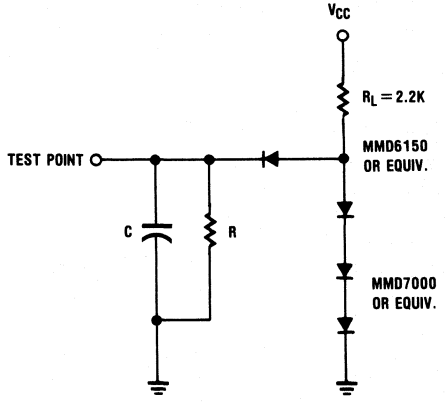
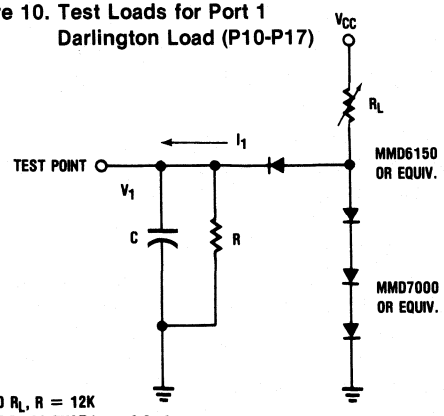


Figure 9. Bus Timing Test Load and Ports 1, 3 and 4 for Single Chip Mode



C = 90pF FOR P30-P37, P40-P47, E, SC1, SC2
R = 16.5KΩ FOR P30-P37, P40-P47, E, SC1, SC2

Figure 10. Test Loads for Port 1 Darlington Load (P10-P17)



C = 40 R_L, R = 12K
ADJUST R_L SO THAT I_1 = 3.2mA
WITH V_1 = 0.4V and V_{CC} = 5.25V

Figure 11. Typical Data Bus Output Delay versus Capacitive Loading

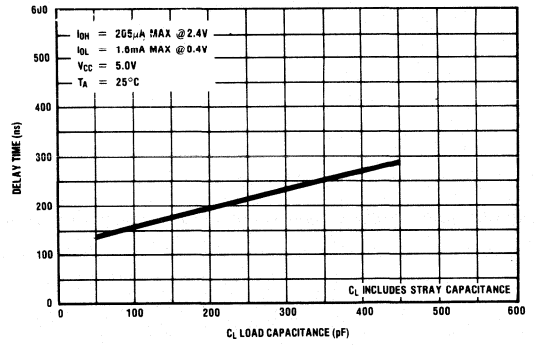
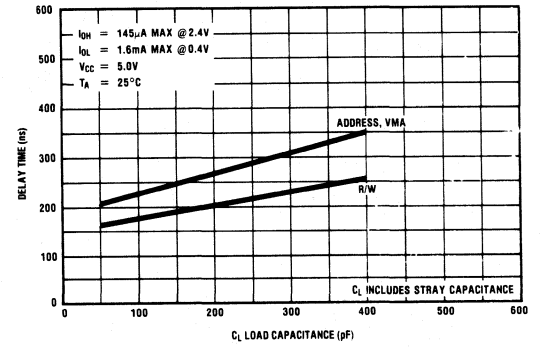


Figure12. Typical Read/Write, VMA, and Address Output Delay Versus Capacitive Loading



Signal Descriptions

V_{CC} and V_{SS}

These two pins are used to supply power and ground to the chip. The voltage supplied will be +5 volts±5%.

XTAL 1 and EXTAL 2

These connections are for a parallel resonant fundamental crystal, AT cut. Divide by 4 circuitry is included with the internal clock, so a 4 MHz crystal may be used to run the system at 1MHz. The divide by 4 circuitry allows for use of the inexpensive 3.56 MHz Color TV crystal for non-time critical applications. Two 27pF capacitors are needed from the two crystal pins to ground to insure reliable operation. EXTAL 2 may be driven by an external clock source at a 4 MHz rate to run at 1 MHz with a 40/60% duty cycle. It is not restricted to 4 MHz. XTAL 1

must be grounded if an external clock is used. The following are the recommended crystal parameters:

AT=Cut Parallel Resonance Crystal
C_o=7pF Max
FREQ=4.0 MHz @ C_L=24pF
R_S=50 ohms Max
Frequency Tolerance=±5% to ±0.02%
The best E output "Worst Case Design" tolerance is ±0.05% (500ppM) using a ±0.02% crystal.

V_{CC} Standby

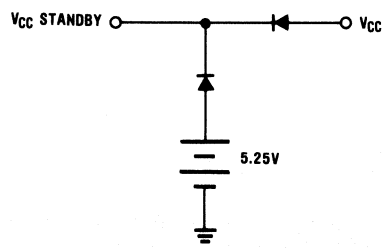
This pin will supply +5 volts ±5% to the standby RAM on the chip. The first 64 bytes of RAM will be maintained in the power down mode with 8 mA current max in the ROM version. The circuit of Figure 15 can be utilized to assure that V_{CC} Standby does not go below V_{SBB} during power down.

To retain information in the RAM during power down the following procedure is necessary:

1) Write "0" into the RAM enable bit, RAM E. RAM E is bit 6 of the RAM Control Register at location $0014. This disables the standby RAM, thereby protecting it at power down.

2) Keep V_{CC} Standby greater than V_{SBB}.

Figure 13. Battery Backup for V_{CC} Standby



Reset

This input is used to reset and start the MPU from a power down condition, resulting from a power failure or an initial startup of the processor. On power up, the reset must be held low for at least 20 ms. During operation, $\overline{\text{Reset}}$, when brought low, must be held low at 3 clock cycles.

When a high level is detected, the MPU does the following:

a) All the higher order address lines will be forced high.

b) I/O Port 2 bits, 2, 1, and 0 are latched into programmed control bits PC2, PC1 and PC0.

c) The last two (FFFE, FFFF) locations in memory will be used to load the program addressed by the program counter.

d) The interrupt mask bit is set, must be cleared before the MPU can recognize maskable interrupts.

Enable (E)

This supplies the external clock for the rest of the system when the internal oscillator is used. It is a single phase, TTL compatible clock, and will be the divide by 4 result of the crystal frequency. It will drive one TTL load and 90pF.

Non-Maskable Interrupt ($\overline{\text{NMI}}$)

A low-going edge on this input requests that a non-maskable-interrupt sequence be generated within the processor. As with the Interrupt Request signal, the processor will complete the current instruction that is being executed before it recognizes the $\overline{\text{NMI}}$ signal. The interrupt mask bit in the Condition Code Register has no effect on $\overline{\text{NMI}}$.

In response to an $\overline{\text{NMI}}$ interrupt, the Index Register, Program Counter, Accumulators, and Condition Code Register are stored on the stack. At the end of the sequence, a 16-bit address will be loaded that points to a vectoring address located in memory locations FFFC and FFFD. An address loaded at these locations causes the MPU to branch to a non-maskable interrupt service routine in memory.

A 3.3 KΩ external resistor to V_{CC} should be used for wire-OR and optimum control of interrupts.

Inputs $\overline{\text{IRQ}}$ and $\overline{\text{NMI}}$ are hardware interrupt lines that are sampled during E and will start the interrupt routine on the clock bar following the completion of an instruction.

Interrupt Request ($\overline{\text{IRQ}}$)

This level sensitive input requests that an interrupt sequence be generated within the machine. The processor will wait until it completes the current instruction that is being executed before it recognizes the request. At that time, if the interrupt mask bit in the Condition Code Register is not set, the machine will begin an interrupt sequence. The Index Register, Program Counter, Accumulators, and Condition Code Register are stored on the

stack. Next the MPU will respond to the interrupt request by setting the interrupt mask bit high so that no further maskable interrupts may occur. At the end of the cycle, a 16-bit address will be loaded that points to a vectoring address which is located in memory locations FFF8 and FFF9. An address loaded at these locations causes the MPU to branch to an interrupt routine in memory.

The IRQ requires a 3.3KΩ external resistor to V_{CC} which should be used for wire-OR and optimum control of interrupts. Internal Interrupts will use an internal interrupt line (IRQ2). This Interrupt will operate the same as IRQ except that it will use the vector address of FFF0 and FFF7. IRQ1 will have priority over IRQ2 if both occur at the same time. The Interrupt Mask Bit in the condition mode register masks both interrupts. (See Figure 23.)

The following pins are available in the Single Chip Mode, and are associated with Port 3 only.

Input Strobe ($\overline{IS3}$) (SC1)

This sets an interrupt for the processor when the IS3 Enable bit is set. As shown in Figure 6 Input Strobe Timing, IS3 will fall T_{IS} minimum after data is valid on Port 3. If IS3 Enable is set in the I/O Port Control/Status Register, an interrupt will occur. If the latch enable bit in the I/O Control Status Register is set, this strobe will latch the input data from another device when that device has indicated that it has valid data.

Output Strobe ($\overline{OS3}$) (SC2)

This signal is used by the processor to strobe an external device, indicating valid data is on the I/O pins. The timing for the Output Strobe is shown in Figure 5. I/O Port Control/Status Register is discussed in the following section.

The following pins are available in the Expanded Modes.

Read Write (R/W) (SC2)

This TTL compatible output signals the peripherals and memory devices whether the MPU is in a Read (high) or a Write (low) state. The normal standby state of this signal is Read (high). This output is capable of driving one TTL load and 90pF.

I/O Strobe ($\overline{IOS}$) (SC1)

In the expanded non-multiplexed mode of operation, $\overline{IOS}$ internally decodes A9 through A15 as zero's and A8 as a one. This allows external access of the 256 locations from $0100 to $01FF. The timing diagrams are shown as Figures 1 and 2.

Address Strobe (AS) (SC1)

In the expanded multiplexed mode of operation address strobe is output on this pin. This signal is used to latch the 8 LSB's of address which are multiplexed with data on Port 3. An 8-bit latch is utilized in conjunction with Address Strobe, as shown in Figure 27. Expanded Multiplexed Mode. Address Strobe signals the latch when it is time to latch the address lines so the lines can become data bus lines during the E pulse. The timing for this signal is shown in the MC6801 Bus Timing Figure 7. This signal is also used to disable the address from the multiplexed bus allowing a deselect time, T_{ASD} before the data is enabled to the bus.

S6801 Ports

There are four I/O ports on the S6801MCU; three 8-bit ports and one 5-bit port. There are two control lines associated with one of the 8-bit ports. Each port has an associated write only Data Direction Register which allows each I/O line to be programmed to act as an input or an output. *A "1" in the corresponding Data Direction Register bit will cause that I/O line to be an output A "0" in the corresponding Data Direction Register bit will cause the I/O line to be an input. There are four ports: Port 1, Port 2, Port 3, and Port 4. Their addresses and the addresses of their Data Direction registers are given in Table 2.

**The only exception is bit 1 of Port 2, which can either be data input or Timer output.*

Table 2. Port and Data Direction Register Addresses

Ports	Port Address	Data Direction Register Address
I/O Port 1	$0002	$0000
I/O Port 2	$0003	$0001
I/O Port 3	$0006	$0004
I/O Port 4	$0007	$0005

I/O Port 1

This is an 8-bit port whose individual bits may be defined as inputs or outputs by the corresponding bit in its data direction register. The 8 output buffers have three-state capability, allowing them to enter a high impedance state when the peripheral data lines are used as inputs. In

order to be read properly, the voltage on the input lines must be greater than 2.0 volts for a logic "1" and less than 0.6 volt for a logic "0". As outputs, these lines are TTL compatible and may also be used as a source of up to 1 mA at 1.5 volts to directly drive a Darlington base. After Reset, the I/O lines are configured as inputs. In all three modes, Port 1 is always parallel I/O.

I/O Port 2

This port has five lines that may be defined as inputs or outputs by its data direction register. The 5 output buffers have three-state capability, allowing them to enter a high impedance state when used as an input. In order to be read properly, the voltage on the input lines must be greater than 2.0 volts for a logic "1" and less than 0.8 volt for a logic "0". As outputs, this port has no internal pullup resistors but will drive TTL inputs directly. For driving CMOS inputs, external pullup resistors are required. After Reset, the I/O lines are configured as inputs. Three pins on Port 2 (pins 10, 9 and 8 of the chip) are used to program the mode of operation during reset. The values of these pins at reset are latched into the three MSB's (bits 7, 6, and 5) of Port 2 which are read only. This is explained in the Mode Selection Section.

In all three modes, Port 2 can be configured as I/O and provides access to the Serial Communications Interface and the Timer. Bit 1 is the only pin restricted to data input or Timer output.

I/O Port 3

This is an 8-bit port that can be configured as I/O, a data bus, or an address bus multiplexed with the data bus — depending on the mode of operation hardware programmed by the user at reset. As a data bus, Port 3 is bidirectional. As an input for peripherals, it must be supplied regular TTL levels, that is, greater than 2.0 volts for a logic "1" and less than 0.5 volt for a logic "0".

Its TTL compatible three-state output buffers are capable of driving one TTL load and 90pF. In the Expanded Modes, after reset, the data direction register is inhibited and data flow depends on the state of the R/W line. The input strobe (IS3) and the output strobe (OS3) used for handshaking are explained later.

In the three modes Port 3 assumes the following characteristics:

Single Chip Mode: Parallel Inputs/Outputs as programmed by its associated Data Direction Register. There are two control lines associated with this port in this mode, an input strobe and an output strobe, that can be used for handshaking. They are controlled by the I/O Port Control/Status Register explained at the end of this section.

Expanded Non-Multiplexed Mode: In this mode Port 3 become the data bus (D7-D0).

Expanded Multiplexed Mode: In this mode Port 3 becomes both the data bus (D7-D0) and lower bits of the address bus (A7-A0). An address strobe output is true when the address is on the port.

I/O Port 3 Control/Status Register

	7	6	5	4	3	2	1	0
$000F	IS3 FLAG	IS3 ENABLE	X	OSS	LATCH ENABLE	X	X	X

Bit 0 Not used.
Bit 1 Not used.
Bit 2 Not used.
Bit 3 Latch Enable. This controls the input latch for I/O Port 3. If this bit is set high the input data will be latched with the falling edge of the Input Strobe, IS3. This bit is cleared by reset, or CPU Read Port 3.
Bit 4 (OSS) Output Strobe Select. This bit will select if the Output Strobe should be generated by a write to I/O Port 3 or a read of I/O Port 3. When this bit is cleared the strobe is generated by a read Port 3. When this bit is set the strobe is generated by a write Port 3.
Bit 5 Not used.
Bit 6. IS3 ENABLE. This bit will be the interrupt caused by IS3. When set to a low level the IS3 FLAG will be set by input strobe but the interrupt will not be generated. This bit is cleared by reset.
Bit 7 IS3 FLAG. This is a read only status bit that is set by the failing edge of the input strobe, IS3. It is cleared by a read of the Control/Status Register followed by a read or write of I/O Port 3. Reset will clear this bit.

I/O Port 4

This is an 8-bit port that can be configured as I/O or as address lines depending on the mode of operation. In order to be read properly, the voltage on the input lines must be greater than 2.0 volts for a logic "1" and less

than 0.8 volt for a logic "0". As outputs, each line is TTL compatible and can drive 1 TTL load and 90pF. After reset, the lines are configured as inputs. To use the pins as addresses, therefore, they should be programmed as outputs in the three modes. Port 4 assumes the following characteristics.

Single Chip Mode: Parallel Inputs/Outputs as programmed by its associated Data Direction Register.

Expanded Non-Multiplexed Mode: In this mode Port 4 is configured as the lower order address lines (A7-A0) by writing one's to the data direction register. When all eight address lines are not needed, the remaining line starting with the most significant bit, may be used as I/O (inputs only).

Expanded Multiplexed Mode: In this mode Port 4 is configured as the high order address lines (A15-A8) by writing one's to the data direction register. When all eight address lines are not needed, the remaining line, starting with the most significant bit, may be used as I/O (inputs only).

Mode Selection

The mode of operation that 6801 will operate in after Reset is determined by hardware that the user must wire on pins 10, 9, and 8 of the chip. These pins are the three

LSB's (I/O2, I/O1, and I/O0 respectively) of Port 2. They are latched into programmed control bits PC2, PC1, and PC0 when reset goes high. I/O Port 2 Register is shown below.

	7	6	5	4	3	2	1	0
$0003	PC2	PC1	PC0	I/O4	I/O3	I/O2	I/O1	I/O0

An example of external hardware that could be used in the Expanded Non-Multiplexed Mode is given in Figure 14. In the Expanded Non-Multiplexed Mode, pins 10, 9 and 8 are programmed Hi, Lo, Hi respectively as shown.

Couplers between the pins on Port 2 and the peripherals attached may be required. If the lines go to devices which require signals at power up differing from the signals needed to program the 6801's mode, couplers are necessary.

The 14066B can be used to provide this isolation between the peripheral device and the MCU during reset. Figure 15 shows the logic diagram and xxxxx? for the MC14066B. It is bidirectional and requires no external logic to determine the direction of the information flow.

The logic shown insures that the data on the peripheral will not change before it is latched into the MCU and the MCU has started the reset sequence.

Figure 14. Diode Configuration for the Expanded Non-Multiplexed Mode

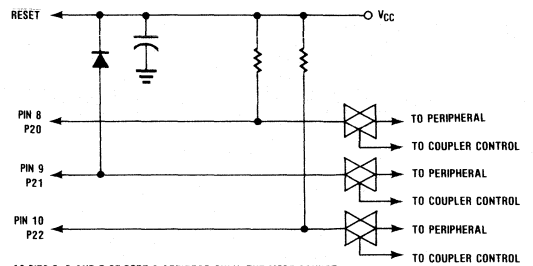
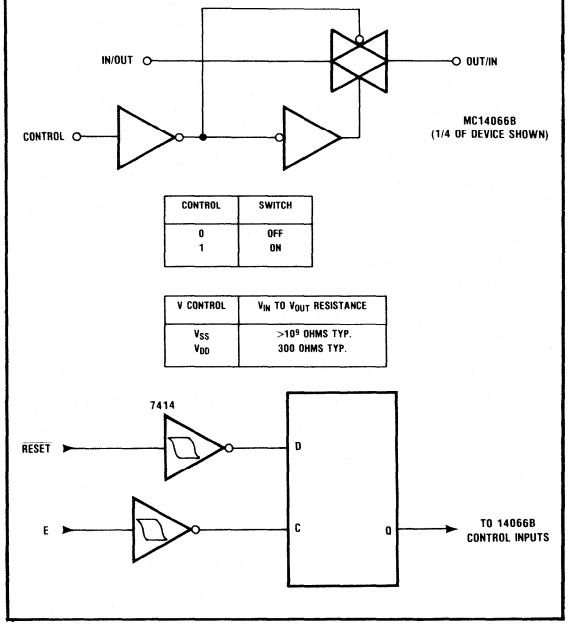


Figure 15. Quad Analog, Switch/Multiplexer In a Typical S6801 Circuit



S6800

S6801 Basic Modes

The S6801 is capable of operating n three basic modes, (1) Single Chip Mode, (2) Expanded Multiplexed Mode (compatible with S6800 peripheral family, (3) Expanded Non-Multiplexed Mode.

Single Chip Mode

Both mask options will operate in this mode. In the Single Chip Mode the parts are configured for I/O.

Internal Clock/Divide-by-Four (S6801)—This mask option is shown in Figure 16. In this mode, Port 3 has two associated control lines, an input strobe and an output strobe for handshaking data.

External Clock/Divide-by-One (S6801E)—This mask option is shown in Figure 16a. The Read/Write (R/W) line, Chip Select (CS), and Register Select (RS) are associated with Port 3 only. The Read/Write (R/W) line controls the direction of data on Port 3 and Chip Select (CS) enables Port 3. The Register Select (RS) allows for the access of Port 3 data register or Port 3 control register.

Figure 16. S6801 MCU Single Chip Mode

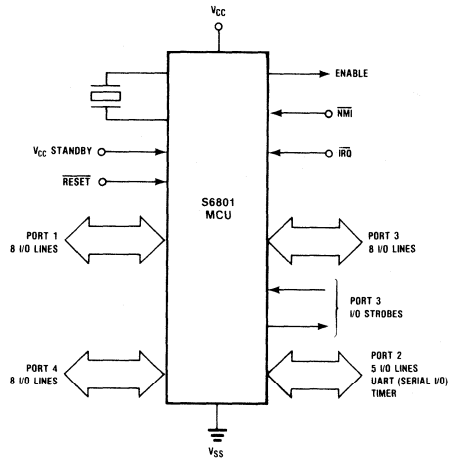
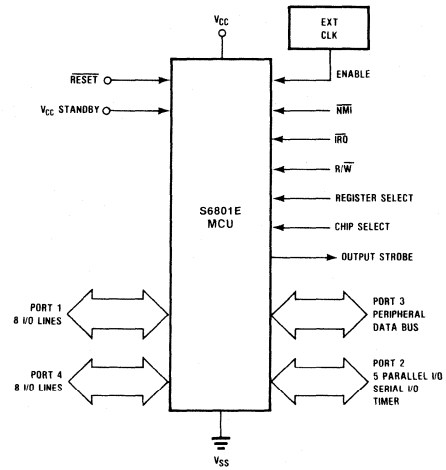


Figure 16a. S6801E MCU Single-Chip Mode



Expanded Non-Multiplexed Mode

In this mode the S6801 will directly address S6800 peripherals with no external logic. In this mode Port 3 becomes the data bus. Port 4 becomes the A7-A0 address bus or partial address and I/O (inputs only). Port 2 can be parallel I/O, serial only. In this mode the S6801 is expandable to 256 locations. The eight address lines associated with Port 4 may be substituted for I/O (inputs only) if a fewer number of address lines will satisfy the application.

Internal Clock/Divide-by-Four—This mask option is shown in Figure 17. The Internal Clock requires only the addition of a crystal for operation. This input will also accept an external TTL or CMOS input, but in either case, the clock frequency will be divided by four for this mask option.

External Clock/Divide-by-One—This mask option is shown in Figure 17a. The External Clock/Divide-by-One allows for an external clock to be applied to the Enable Pin. This is a divide-by-one input only.

Expanded Multiplexed Mode

In this mode Port 4 becomes higher order address lines with an alternative of substituting some of the address lines for I/O (inputs only). Port 3 is the data bus multiplexed with the lower order address lines differentiated by an output called Address Strobe. Port 2 is 5 lines of Parallel I/O, SC1, Timer, or any combination thereof. Port 1 is 8 Parallel I/O lines. In this mode it is expandable to 65K words.

Internal Clock/Divide-by-Four—This mask option is shown in Figure 18. Only an external crystal is required for operation.

External Clock/Divide-by-One—This mask option is shown in Figure 18a. This accepts an external clock input to the enable pin.

Figure 17. S6801 MCU Expanded Non-Multiplexed Mode

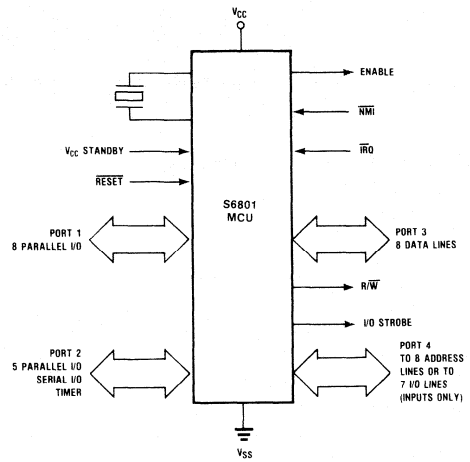


Figure 17a. S6801E MCU Expanded Non-Multiplexed-Mode

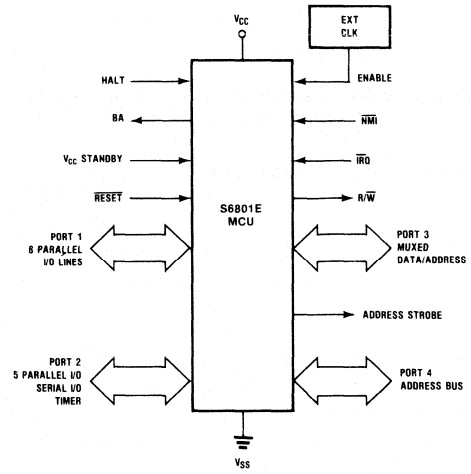


Figure 18. S6801 MCU Expanded Multiplexed Mode

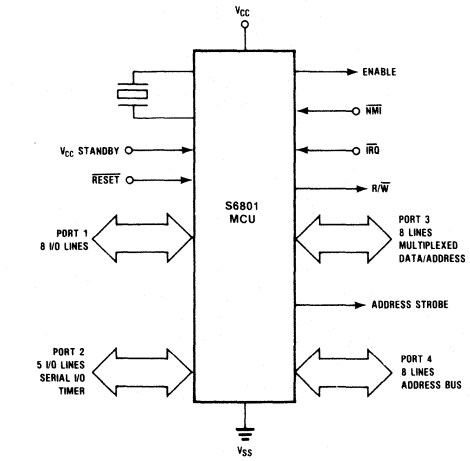


Figure 18a. S6801E MCU Expanded Multiplexed-Mode

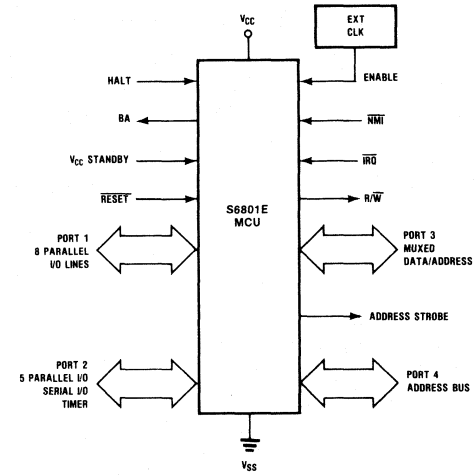


Table 3. Mode Selects

MODE		PROGRAM CONTROL			ROM	RAM	INTERRUPT VECTORS	BUS
7	Single Chip	Hi	Hi	Hi	I	I	I	I
6	Expanded Multiplexed	Hi	Hi	Lo	I	I	I	Ep/M
5	Expanded Non-Multiplexed	Hi	Lo	Hi	I	I	I	Ep
4	Single Chip Test	Hi	Lo	Lo	I(2)	I(1)	I	I
3	64K Address I/O	Lo	Hi	Hi	E	E	E	Ep/M
2	Ports 3 & 4 External	Lo	Hi	Lo	E	I	E	Ep/M
1		Lo	Lo	Hi	I	I	E	Ep/M
0	Test Data Outputted from ROM & ROM to I/O Port 3	Lo	Lo	Lo	I	I	I*	Ep/M

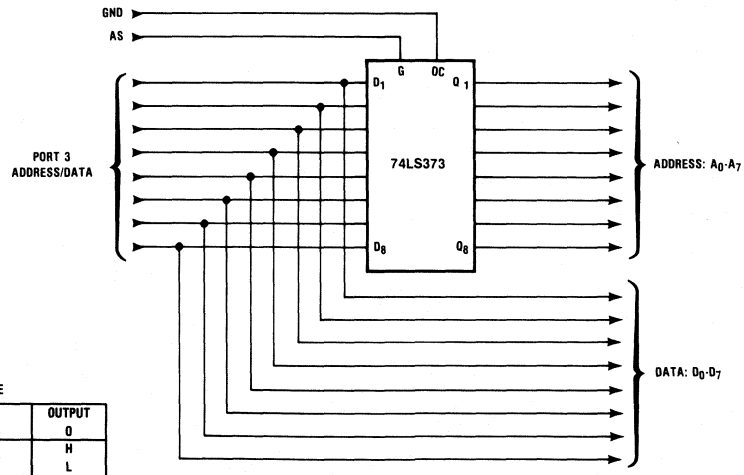
E—EXTERNAL all vectors are external
I—INTERNAL
Ep—EXPANDED MULTIPLEXED

*First two addresses read from external after reset
(1) Address for RAM XX80-XXFF
(2) ROM disabled

Lower Order Address Bus Latches

Since the data bus is multiplexed with the lower order address bus in Port 3, latches are required to latch those address bits. The SN74LS373 Transparent octal D-type latch can be used with the S6801 to latch the least significant address byte. Figure 19 shows how to connect the latch to the S6801. The output control to the LS373 may be connected to ground.

Figure 19. Latch Connection



FUNCTION TABLE

OUTPUT CONTROL	ENABLE G	ENABLE D	OUTPUT Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

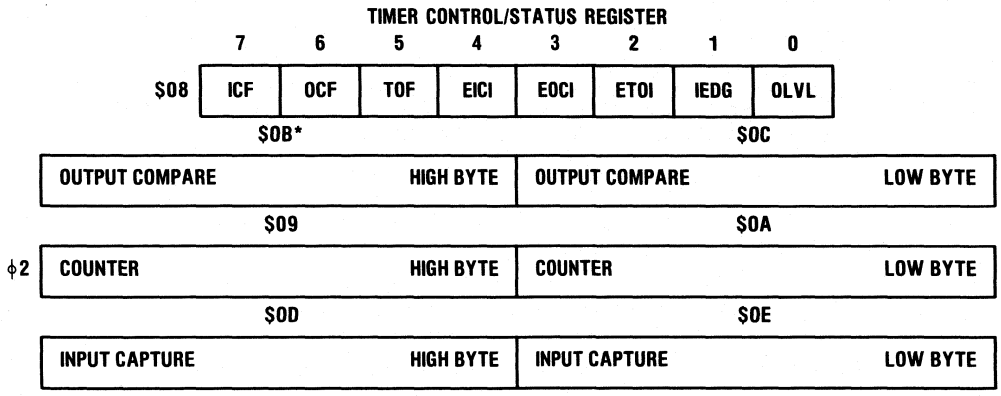
Programmable Timer

The S6801 contains an on-chip 16-bit programmable timer which may be used to perform measurements on an input waveform while independently generating an output waveform. Pulse widths for both input and output signals may vary from a few microseconds to many seconds. The timer hardware consists of

- an 8-bit control and status register
- a 16-bit free running counter
- a 16-bit output compare register, and
- a 16-bit input capture register

A block diagram of the timer registers is shown in Figure 20.

Figure 20. Block Diagram of Timer Registers



*THE CHARACTERS ABOVE THE REGISTERS REPRESENT THEIR ADDRESS IN HEX.

Free Running Counter ($0009:000A)

The key element in the programmable timer is a 16-bit free running counter which is driven to increasing values by the MPUϕ. The counter value may be read by the MPU software at any time. The counter is cleared to zero on RESET and may be considered a read-only register with one exception. Any MPU write to the counter's address ($09) will always result in a preset value of $FFF8 being loaded into the counter regardless of the value involved in the write. The preset feature is intended for testing operation of the part, but may be of value in some applications.

Output Compare Register ($000B:000C)

The Output Compare Register is a 16-bit read/write register which is used to control an output waveform. The contents of this register are constantly compared with the current value of the free running counter. When a match is found a flag is set (OCF) in the Timer Control and Status Register (TCSR) and the current value of the Output Level bit (OLVL) in the TCSR is clocked to the output level register. Providing the Data Direction Register for Port 2, Bit 1 contains a "1" (output), the output level register value will appear on the pin for Port 2 Bit 1. The values in the Output Compare Register and Output level bit may then be changed to control the output level on the next compare value. The Output Compare Register is set to $FFFF during RESET. The Compare function is inhibited for one cycle following a write to the high byte of the Output Compare Register to insure a valid 16-bit value is in the register before a compare is made.

Input Capture Register ($000D:000E)

The Input Capture Register is a 16-bit read-only register used to store the current value of the free running counter when the proper transition of an external input signal occurs. This input transition change required to trigger the counter transfer is controlled by the input Edge bit (EDG) in the TOSR. The Data Direction Register bit for Port 1 Bit 0 should *be clear (zero) in order to gate in the external input signal to the edge defect unit in the timer.

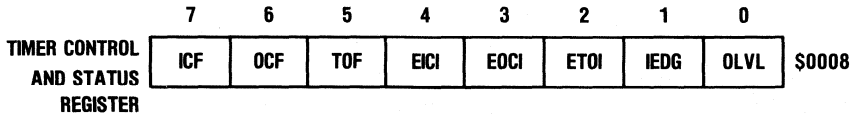
*With Port 2 Bit 0 configured as an output and set to "1". the external input will still be seen by the edge detect unit.

Timer Control and Status Register (TCSR) ($0008)

The Timer Control and Status Register consists of an 8-bit register of which all 8 bits are readable but only the low order 5 bits may be written. The upper three bits contain read-only timer status information and indicate that:

- a proper transition has taken place on the input pin with a subsequent transfer of the current counter value to the input capture register.
- a match has been found between the value in the free running counter and the output compare register, and
- when $0000 is in the free running counter.

Each of the flags may be enabled onto the S6801 internal bus (RO2) with an individual Enable bit in the tCSR. If the 1-bit in the S6801 Condition Code Register has been cleared, a priority vectored interrupt will occur corresponding to the flag bit(s) set. A description for each bit follows:



Bit 0 OLVL — **Output Level**—This value is clocked to the output level register on an output compare. If the DDR for Port 2 bit 1 is set, the value will appear on the output pin.

Bit 1 IEDG — **Input Edge**—This bit controls which transition of an input will trigger a transfer of the counter to the input capture register. The DDR for Port 2 Bit 0 must be clear for this function to operate.
IEDG = 0 Transfer takes place on a negative (high-to-low transition).
IEDG = 1 Transfer takes place on a positive edge (low-to-high transition).

Bit 2 ETOI — **Enable Timer Overflow Interrupt**—When *set*, this bit enables IRQ2 to occur on the internal bus for a TOF Interrupt; when *clear* the interrupt is inhibited.

Bit 3 EOCI — **Enable Output Compare Interrupt**—When *set*, this bit enables IRQ2 to appear on the internal bus for an input capture interrupt; when *clear* the interrupt is inhibited.

Bit 4 EICI — **Enable Input Capture Interrupt**—When *set*, this bit enables IRQ2 to occur on the internal bus for an input capture interrupt; when *clear* the interrupt is inhibited.

Bit 5 TOF — **Timer Overflow Flag**—This read-only bit is *set* when the counter contains $0000. It is *cleared* by a read of the TCSR (with TOF set) followed by an MPU read of the Counter ($09).

Bit 6 OCF — **Output Compare Flag**—This read-only bit is *set* when a match is found between the output compare register and the free running counter. It is *cleared* by a read of the TCSR (with ODF set) followed by an MPU write to the output compare register ($0B or $0C).

Bit 7 CF — **Input Capture Flag**—This read-only status bit is *set* by a proper transition on the input to the edge detect unit; it is *cleared* by a read of the TCSR (with ICF set) followed by an MPU read of the input Capture Register ($0D).

Serial Communications Interface

The S6801 contains a full-duplex asynchronous serial communications interface (SCI) on board. Two serial data formats (standard mark/space [NRZ] or Bi-phase) are provided at several different data rates. The controller comprises a transmitter and a receiver which operate independently or each other but in the same data format and at the same data rate. Both transmitter and receiver communicate with the MPU via the data bus and with the outside world via pins 2, 3, and 4 of Port 2. The hardware, software, and registers are explained in the following paragraphs.

Wake-up Feature

In a typical multi-processor application, the software protocol will usually contain a destination address in the initial byte(s) of the message. In order to permit non-

selected MPU's to ignore the remainder of the message, a wake-up feature is included whereby all further interrupt processing may be optionally inhibited until the beginning of the next message. When the next messge appears, the hardware re-enables (or "wakes-up") for the next message. The "wake-up" is automatically triggered by a string of ten consecutive 1's which indicates an idle transmit line. The software protocol must provide for the short idle period between any two consecutive messages.

Programmable Options

The following features of the S6801 serial I/O section have programmable:

- format—standard mark/space (NRZ) or Bi-phase
- clock—external or internal
- baud rate—one of 14 per given MPUϕ2 clock frequency or external clock X8 input
- wake-up feature—enabled or disabled
- interrupt requests—enabled or masked indivually for transmitter and receiver data registers
- clock output—internal clock enabled or disabled to Port 2 (Bit 2)
- Port 2 (bits 3 and 4)—dedicated or not dedicated to serial I/O individually for transmitter and receiver

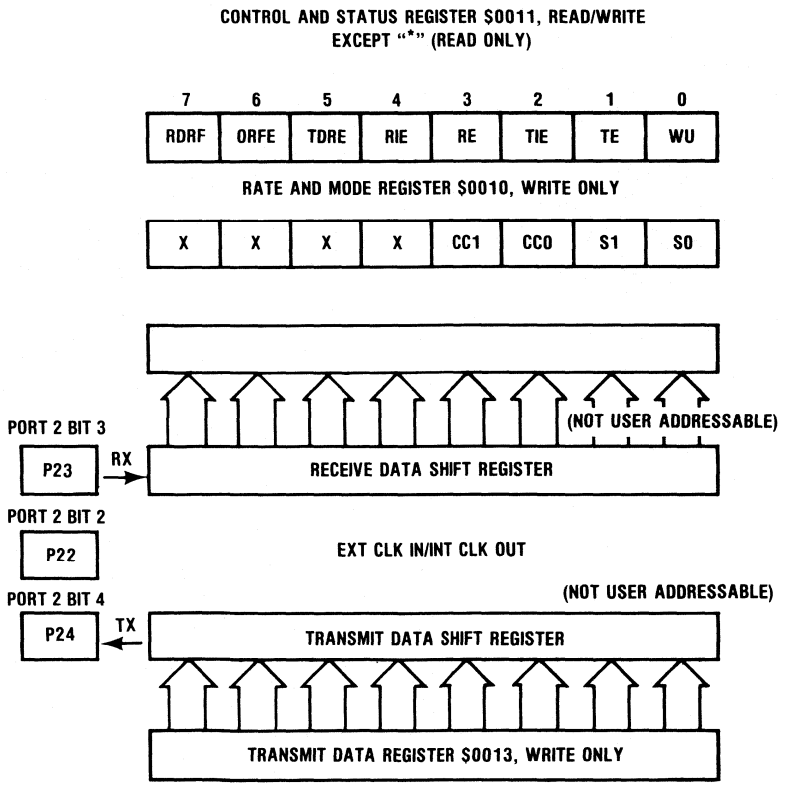
Serial Communications Hardware

The serial communications hardware is controlled by 4 registers as shown in Figure 21. The registers include:

- an 8-bit control and status register
- a 4-bit rate and mode control register (write only)
- an 8-bit read-only receive data register and
- an 8-bit write-only transmit data register

In addition to the four registers, the serial I/O section utilizes bit 3 (serial input) and bit 4 (serial output) or Port 2. Bit 2 of Port 2 is utilized if the internal-clock-out or external-clock-in options are selected.

Figure 21. Serial I/O Registers



Transmit/Receive Control and Status (TRCS) Register

The TRCS register consists of an 8-bit register of which all 8 bits may be read while only bits 0-4 may be written. The register is initialized to $20 on $\overline{\text{RESET}}$. The bits in the TRCS register are defined as follows:

7	6	5	4	3	2	1	0	
RDRE	ORFE	TDRE	RIE	RE	TIE	TE	WU	ADDR. $0011

Bit 0 WU — **"Wake-up on Next Message**—set by S6801 software cleared by hardware on receipt of ten consecutive 1's.

Bit 1 TE — **Transmit Enable**—set by S6801 to produce preamble of nine consecutive 1's and to enable gating of transmitter output to Port 2, bit 4 regardless of the DDR value corresponding to this bit; when clear, serial I/O has no effect on Port 2 bit 4.

Bit 2 TIE — **Transmit Interrupt Enable**—when set, will permit an $\overline{\text{IRQ2}}$ interrupt to occur when bit 5 (TDRE) is set; when clear, the TDRE value is masked from the bus.

Bit 3 RE — **Receiver Enable**—when set, gates Port 2 bit 3 to input of receiver regardless of DDR value for this bit; when clear, serial I/O has no effect on Port 2 bit 3.

Bit 4 RIE — **Receiver Interrupt Enable**—when set, will permit an $\overline{\text{IRQ2}}$ interrupt to occur when bit 7 (RDRF) or bit 6 (OR) is set; when clear, the interrupt is masked.

Bit 5 TDRE — **Transmit Data Register Empty**—set by hardware when a transfer is made from the transmit data register to the output shift register. The TDRE bit is cleared by reading the status register, then writing a new byte into the transmit data register, TDRE is initialized to 1 by $\overline{\text{RESET}}$.

Bit 6 ORFE — **Over-Run-Framing Error**—set by hardware when an overrun or framing error occurs (receive only). An overrun is defined as a new byte received with last byte still in Data Register/Buffer. A framing error has occured when the byte boundaries in bit stream are not synchronized to bit counter. The ORFE bit is cleared by reading the status register, then reading the Receive Data Register, or by $\overline{\text{RESET}}$.

Bit 7 RDRF — **Receiver Data Register Full**—set by hardware when a transfer from the input shift register to the receiver data register is made. The RDRF bit is cleared by reading the status register, then reading the Receive Data Register, or by $\overline{\text{RESET}}$.

Rate and Mode Control Register

The Rate and Mode Control register controls the following serial I/O variables:

- Baud rate
- format
- Clocking source, and
- Port 2 bit 2 configuration

The register consists of 4 bits all of which are write-only and cleared on $\overline{\text{RESET}}$. The 4 bits in the register may be considered as a pair of 2-bit fields. The two low order bits control the bit rate for internal clocking and the remaining two bits control the format and clock select logic. The register definition is as follows:

7	6	5	4	3	2	1	0	
X	X	X	X	CC1	CC0	S1	S0	ADDR. $0010

Bit 0 S0
Bit 1 S1 — **Speed Select**—These bits select the Baud rate for the internal clock. The four rates which may be selected are a function of the MPU $\phi 2$ clock frequency. Table 4 lists the available Baud rate.

Bit 2 CC0
Bit 3 CC1 — **Clock Control and Format Select**—This 2-bit field controls the format and clock select logic. Table 5 defines the bit field.

Table 4. SCI Internal Baud Rates

S1, S0	XTAL	4.0MHz	4.9152MHz	2.5476MHz
	$\phi 2$	1.0MHz	1.2288MHz	0.6144MHz
00	$\phi 2 \div 16$	62.5K BITS/S	76.8K BITS/S	38.4K BITS/S
01	$\phi 2 \div 128$	7,812.5 BITS/S	9,600 BITS/S	4,800 BITS/S
10	$\phi 2 \div 1024$	976.6 BITS/S	1,200 BITS/S	600 BITS/S
11	$\phi 2 \div 4096$	244.1 BITS/S	300 BITS/S	150 BITS/S

Table 5. Bit Field

CC1, CC0	FORMAT	CLOCK SOURCE	PORT 2 BIT 2	PORT 2 BIT 3	PORT 2 BIT 4
00	BI-PHASE	INTERNAL	NOT USED	**	**
01	NRZ	INTERNAL	NOT USED	**	**
10	NRZ	INTERNAL	OUTPUT*	SERIAL INPUT	SERIAL OUTPUT
11	NRZ	EXTERNAL	INPUT	SERIAL INPUT	SERIAL OUTPUT

*CLOCK OUTPUT IS AVAILABLE REGARDLESS OF VALUES FOR BITS RE AND TE.
**BIT 3 IS USED FOR SERIAL INPUT IF RE = "1" IN TRCS; BIT 4 IS USED FOR SERIAL OUTPUT IF TE = "1" IN TRCS.

Internally Generated Clock

If the user wishes for the serial I/O to furnish a clock, the following requirements are applicable:

- the values of RE and TE are immaterial
- CC1, CC0 must be set to 10
- the maximum clock rate will be $\phi \div 16$
- the clock will be at 1× the bit rate and will have a rising edge at mid-bit

Externally Generated Clock

If the user wishes to provide an external clock for the serial I/O, the following requirements are applicable:

- the CC1, CC0, field in the Rate and Mode Control Register must be set to 11.
- the external clock must be set to 8 times (×8) the desired baud rate and
- the maximum external clock frequency is 1.2MHz.

Serial Operations

The Serial I/O hardware should be initialized by the S6801 software prior to operation. This sequence will normally consist of:

- writing the desired operation control bits to the Rate and Mode Control Register and
- writing the desired operational control bits in the Transmit/Receive Control and Status Register.

The Transmitter Enable (TE) and Receiver Enable (RE) bits may be left set for dedicated operations.

Transmit Operations

The transmit operation is enabled by the TE bit in the Transmit/Receive Control and Status Register. This bit when set, gates the output of the serial transmit shift register to Port 2 Bit 4 and takes unconditional control

over the Data Direction Register value for Port 2, Bit 4.

Following a $\overline{\text{RESET}}$, the user should configure both the Rate and Mode Control Register and the Transmit/Receiver Control and Status Register for desired operation. Setting the TE bit during this procedure initiates the serial output by first transmitting a ten-bit preamble of 1's. Following the preamble, internal synchronization is established and the transmitter section is ready for operation.

At this point one of two situations exist:

a) if the Transmit Data Register is empty (TDRE = 1), a continuous string of ones will be sent indicating an idle line, or
b) if data has been loaded into the Transmit Data Register (TDRE = 0), the word is transferred to the output shift register and transmission of the data word will begin.

During the transfer itself, the 0 start bit is first transmitted. Then the 8 data bits (beginning with bit 0) followed by the stop bit, are transmitted. When the Transmitter Data Register has been emptied, the hardware sets the TDRE flag bit.

If the S6801 fails to respond to the flag within the proper time, (TDRE is still set when the next normal transfer from the parallel data register to the serial output register should occur) then a 1 will be sent (instead of a 0) at "Start" bit time, followed by more 1's until more data is supplied to the data register. No 0's will be sent while TDRE remains a 1.

The Bi-phase mode operates as described above except that the serial output toggles each bit time, and on 1/2 bit times when a 1 is sent.

Receive Operation

The receive operation is enabled by the RE bit which gates in the serial input through Port 2 Bit 3. The receiver section operation is conditioned by the contents of the Transmit/Receive Control and Status Register and the Rate and Mode Control Register.

The receiver bit interval is divided into 8 sub-intervals for internal synchronization. In the standard, non-Bi-phase mode, the received bit stream is synchronized by the first 0 (space) encountered.

The approximate center of each bit time is strobed during the next 10 bits. If the tenth bit is not a 1 (stop bit) a framing error is assumed, and bit ORFE is set. If the tenth bit is 1, the data is transferred to the Receiver Data Register, and interrupt flag RDRF is set. If RDRF is still set at the next tenth bit time, ORFE will be set, indicating an over-run has occurred. When the S6801 responds to either flag (RDRF or ORFE) by reading the status register followed by reading the Data Register RDRF (or ORFE) will be cleared.

Ram Control Register

This register, which is addressed at $0014, gives status information about the standby RAM. A 0 in the RAM enable bit (RAM E) will disable the standby RAM, thereby protecting it at power down if V_{CC} is held greater than V_{SBB} volts, as explained previously in the signal description for V_{CC} Standby.

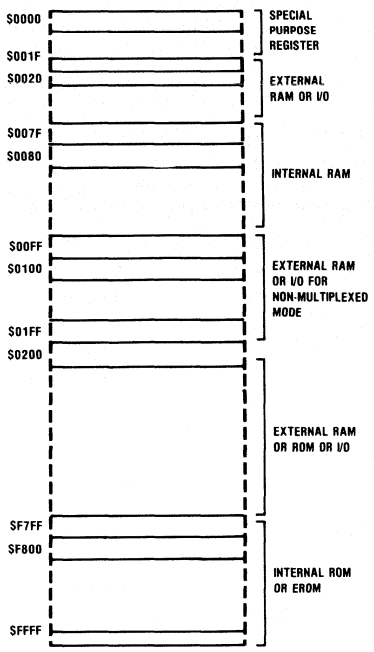
$0014	STAND-BY BIT	RAM E	X	X	X	X	X	X

Bit 1 Not used.
Bit 2 Not used.
Bit 3 Not used.
Bit 4 Not used.
Bit 5 Not used
Bit 6 The RAM ENABLE control bit allows the user the ability to disable the standby RAM. This bit is set to a logic "one" by reset which enables the standby RAM and can be written to or zero under program control. When the RAM is disabled, logic "zero", data is read from external memory.
Bit 7 The STANDBY BIT of the control register, $0014, is cleared when the standby voltage is removed. This bit is a read/write status flag that the user can read which indicates that the standby RAM voltage has been applied, and the data in the standby RAM is valid.

The S6801 provides up to 65K bytes of memory for program and/or data storage. The memory map is shown in Figure 22.

Locations $0020 through $007F access external RAM or I/O Internal RAM is accessed at $0080 through $00FF. The RAM may be alternately selected by mask programming at location $A000. However, if the user desires to access external RAM at those locations he may do so by clearing the RAM ENABLE control bit of the RAM Control Register. In this way an extra 126 bytes of external RAM are available. The first 64 bytes of the 128 bytes of on-chip RAM are provided with a separate power supply. This will maintain the 64 bytes of RAM in the power down mode as explained in the pin description for V_{CC} Standby.

Figure 22. Memory Map



Locations $0100 through $01FF are available in the Expanded Non-Multiplexed Mode. The eight address lines of Port 4 make this 256 word expandability possible. Those not needed for address lines can be used as input lines instead.

The full range of addresses available to the user is in the Expanded Multiplexed Mode. Locations $0200 through $F7FF can be used as external RAM, external ROM, or I/O. Any higher order bit not required for addressing can be used as I/O as in the Expanded Non-Multiplexed Mode.

The internal ROM is located at $F800 through $FFFF. The decoder for the ROM may be mask programmed on A12, and A13 as zeros or one's to provide for $C800, $D800, $E800 for the ROM address. A12 and A13 may also be don't care in this decoder. The primary address for the ROM will be $F800.

The first 32 bytes are for the special purpose registers as shown in Table 6.

Table 6. Special Registers

HEX ADDRESS	REGISTER
00	DATA DIRECTION 1
01	DATA DIRECTION 2
02	I/O PORT 1
03	I/O PORT 2
04	DATA DIRECTION 3
05	DATA DIRECTION 4
06	I/O PORT 3
07	I/O PORT 4
08	TCSR
09	COUNTER HIGH BYTE
0A	COUNTER LOW BYTE
0B	OUTPUT COMPARE HIGH BYTE
0C	OUTPUT COMPARE LOW BYTE
0D	INPUT CAPTURE HIGH BYTE
0E	INPUT CAPTURE LOW BYTE
0F	I/O PORT 3 C/S REGISTER
10	SERIAL RATE AND MODE REGISTER
11	SERIAL CONTROL AND STATUS REGISTER
12	SERIAL RECEIVER DATA REGISTER
13	SERIAL TRANSMIT DATA REGISTER
14	RAM/EROM CONTROL REGISTER
15-1F	RESERVED

Figure 23. Memory Map for Interrupt Vectors

	VECTOR MS	VECTOR LS	DESCRIPTION
Highest Priority	FFFE,	FFFF	Restart
	FFFC,	FFFD	Non-Maskable Interrupt
	FFFA,	FFFD	Software Interrupt
	FFF8,	FFF9	IRQ1/Interrupt Strobe S
	FFF6,	FFF7	IRQ2/Timer Input Capture
	FFF4,	FFF5	IRQ2/Timer Output Compare
	FFF2,	FFF3	IRQ2/Timer Overflow
Lowest Priority	FFF0,	FFF1	IRQ2/Serial I/O Interrupt

General Description of Instruction Set

The S6801 is upward object code compatible with the S6800 as it implements the full S6800 instruction set. The execution times of key instructions have been reduced to increase throughput. In addition, new instructions have been added; these include 16-bit operations and a hardware multiply.

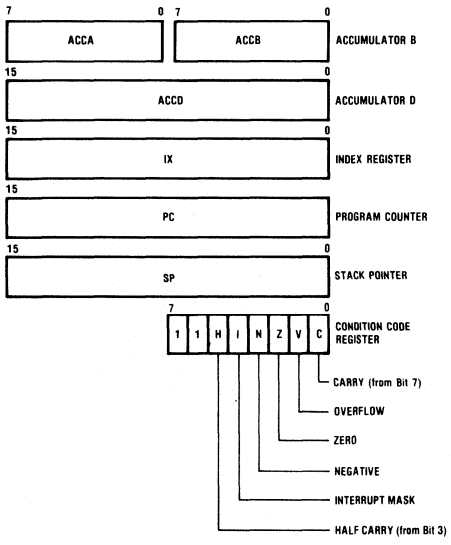
Included in the instruction set section are the following:

- MPU Programming Model (Figure 24)
- Addressing modes
- Accumulator and memory instructions—Table 7
- New instructions
- Index register and stack manipulations—Table 8
- Jump and branch instructions—Table 9
- Special operations—Figure 25
- Condition code register manipulation instructions—Table 10
- Instruction Execution times in machine cycles—Table 11
- Summary of cycle by cycle operation—Table 12

MPU Programming Model

The programming model for the S6801 is shown in Figure 24. The double (D) accumulator is physically the same as the A Accumulator concatenated with the B Accumulator so that any operation using accumulator D will destroy information in A and B.

Figure 24. MCU Programming Model



MPU Addressing Modes

The S6801 eight-bit microcomputer unit has seven address modes that can be used by a programmer, with the addressing mode a function of both the type of instruction and the coding within the instruction. A summary of the addressing modes for a particular instruction can be found in Table 11 along with the associated instruction execution time that is given in machine cycles. With a clock frequency of 4MHz, these times would be microseconds.

Accumulator (ACCX) Addressing—In accumulator only addressing, either accumulator A or accumulator B is specified. These are one-byte instructions.

Immediate Addressing—In immediate addressing, the operand is contained in the second byte of the instruction except LDS and LDX which have the operand in the second and third bytes of the instruction. The MCU addresses this location when it fetches the immediate instruction for execution. These are two or three-byte instructions.

Direct Addressing—In direct addressing, the address of the operand is contained in the second byte of the instruction. Direct addressing allows the user to directly address the lowest 256 bytes in the machine i.e., locations zero through 255. Enhanced execution times are achieved by storing data in these locations. In most configurations, it should be a random access memory. These are two-byte instructions.

Extended Addressing—In extended addressing, the address contained in the second byte of the instruction is used as the higher eight-bits of the address of the operand. The third byte of the instruction is used as the lower eight-bits of the address for the operand. This is an absolute address in memory. These are three-byte instructions.

Indexed Addressing—In indexed addressing, the address contained in the second byte of the instruction is added to the index register's lowest eight bits in the MCU. The carry is then added to the higher order eight bits of the index register. This result is then used to address memory. The modified address is held in a temporary address register so there is no change to the index register. These are two-byte instructions.

Implied Addressing—In the implied addressing mode the instruction gives the address (i.e., stack pointer, index register, etc.). These are one-byte instructions.

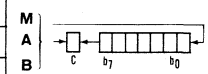
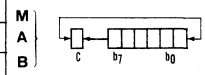
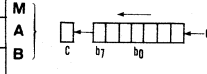
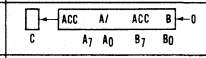
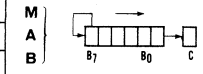
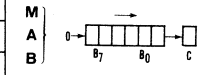
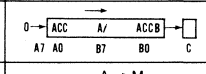
Relative Addressing—In relative addressing, the address contained in the second byte of the instruction is added to the program counter's lowest eight bits plus two. The carry or borrow is then added to the high eight bits. This allows the user to address data within a range of −125 to +120 bytes of the present instruction. These are two-byte instructions.

Table 7. Accumulator & Memory Instructions

ACCUMULATOR AND MEMORY		ADDRESSING MODES																5	4	3	2	1	0
		IMMED.			DIRECT			INDEX			EXTEND			INHERENT									
Operations	**MNEMONIC**	**OP**	~	#	**OP**	~	#	**OP**	~	#	**OP**	~	#	**OP**	~	#	**Boolean/Arithmetic Operation**	**H**	**I**	**N**	**Z**	**V**	**C**
ADD	ADDA	8B	2	2	9B	3	2	AB	4	2	BB	4	3				A + M→A	↕	•	↕	↕	↕	↕
	ADDB	CB	2	2	DB	3	2	EB	4	2	FB	4	3				B + M→B	↕	•	↕	↕	↕	↕
ADD DOUBLE	ADDD	C3	4	3	D3	5	2	E3	6	2	F3	6	3				A:B + M:M + 1→A:B	•	•	↕	↕	↕	↕
ADD ACCUMULATORS	ABA													1B	2	1	A + B→A	↕	•	↕	↕	↕	↕
ADD WITH CARRY	ADCA	89	2	2	99	3	2	A9	4	2	B9	4	3				A + M + C→A		•	↕	↕	↕	↕
	ADCB	C9	2	2	D9	3	2	E9	4	2	F9	4	3				B + M + C→B		•	↕	↕	↕	↕
AND	ANDA	84	2	2	94	3	2	A4	4	2	B4	4	3				A M→A	•	•	↕	↕	R	•
	ANDB	C4	2	2	D4	3	2	E4	4	2	F4	4	3				B M→B	•	•	↕	↕	R	•
BIT TEST	BIT A	85	2	2	95	3	2	A5	4	2	B5	4	3				A M	•	•	↕	↕	R	•
	BIT B	C5	2	2	D5	3	2	E5	4	2	F5	4	3				B M	•	•	↕	↕	R	•
CLEAR	CLR							6F	6	2	7F	6	3				00 →M	•	•	R	S	R	R
	CLRA													4F	2	1	00 →A	•	•	R	S	R	R
	CLRB													5F	2	1	00 →B	•	•	R	S	R	R
COMPARE	CMPA	81	2	2	91	3	2	A1	4	2	B1	4	3				A − M	•	•	↕	↕	↕	↕
	CMPB	C1	2	2	D1	3	2	E1	4	2	F1	4	3				B − M	•	•	↕	↕	↕	↕
COMPARE ACCUMULATORS	CBA													11	2	1	A − B	•	•	↕	↕	↕	↕
COMPLEMENT, 1'S	COM							63	6	2	73	6	3				M→M	•	•	↕	↕	R	S
	COMA													43	2	1	A→A	•	•	↕	↕	R	S
	COMB													53	2	1	B→B	•	•	↕	↕	R	S
COMPLEMENT, 2'S	NEG							60	6	2	70	6	3				0C − M→M	•	•	↕	↕	①	②
(NEGATE)	NEGA													40	2	1	00 − A→A	•	•	↕	↕	①	②
NEGB														50	2	1	00 − B→B	•	•	↕	↕	①	②
DECIMAL ADJUST, A	DAA													19	2	1	Converts binary add of BCD characters into BCD format	•	•	↕	↕	↕	③
DECREMENT	DEC							6A	6	2	7A	6	3				M − 1→M	•	•	↕	↕	④	•
	DECA													4A	2	1	A − 1→A	•	•	↕	↕	④	•
	DECB													5A	2	1	B − 1→B	•	•	↕	↕	④	•
EXCLUSIVE OR	EORA	88	2	2	98	3	2	A8	4	2	B8	4	3				A⊕M→A	•	•	↕	↕	R	•
	EORB	C8	2	2	D8	3	2	E8	4	2	F8	4	3				B⊕M→B	•	•	↕	↕	R	•
INCREMENT	INC							9C	6	2	7C	6	3				M + 1→M	•	•	↕	↕	⑤	•
	INCA													4C	2	1	A + 1→A	•	•	↕	↕	⑤	•
	INCB													5C	2	1	B + 1→B	•	•	↕	↕	⑤	•
LOAD ACCUMULATOR	LDAA	86	2	2	96	3	2	A6	4	2	B6	4	3				M→A	•	•	↕	↕	R	•
	LDAB	C6	2	2	D6	3	2	E6	4	2	F6	4	3				M→B	•	•	↕	↕	R	•
LOAD DOUBLE ACCUMULATOR	LDAD	CC	3	3	DC	4	2	EC	5	2	FC	5	3				M + A M + 1→B	•	•	↕	↕	R	•
MULTIPLY UNSIGNED	MUL													3D	10	1	A × B→AB	•	•	•	•	•	⑫
OR, INCLUSIVE	ORAA	8A	2	2	9A	3	2	AA	4	2	BA	4	3				A + M→A	•	•	↕	↕	R	•
	ORAB	CA	2	2	DA	3	2	EA	4	2	FA	4	3				B + M→B	•	•		↕	•	•

The Condition Code Register notes are listed after Table 10.

Table 7. Accumulator & Memory Instructions (Continued)

ACCUMULATOR AND MEMORY		ADDRESSING MODES																	
		IMMED.			DIRECT			INDEX			EXTEND			INHERENT			5	4	3	2	1	0
Operations	**MNEMONIC**	**OP**	~	#	**OP**	~	#	**OP**	~	#	**OP**	~	#	**OP**	~	#	**Boolean/Arithmetic Operation**	**H**	**I**	**N**	**Z**	**V**	**C**
PUSH DATA	PSHA													36	3	1	$A \rightarrow M_{SP}$ $SP-1 \rightarrow SP$	•	•	•	•	•	•
	PSHB													37	3	1	$B \rightarrow M_{SP}$ $SP-1 \rightarrow SP$	•	•	•	•	•	•
PULL DATA	PULA													33	4	1	$SP+1 \rightarrow SP$, $M_{SP} \rightarrow A$	•	•	•	•	•	•
	PULB													33	4	1	$SP+1 \rightarrow SP$, $M_{SP} \rightarrow B$	•	•	•	•	•	•
ROTATE LEFT	ROL							69	6	2	79	6	3				M A B 	•	•	↕	↕	⑥	↕
	ROLA													49	2	1		•	•	↕	↕	⑥	↕
	ROLB													59	2	1		•	•	↕	↕	⑥	↕
ROTATE RIGHT	ROR							66	6	2	76	6	3				M A B 	•	•	↕	↕	⑥	↕
	RORA													46	2	1		•	•	↕	↕	⑥	↕
	RORB													56	2	1		•	•	↕	↕	⑥	↕
SHIFT LEFT Arithmetic	ASL							66	6	2	78	6	3				M A B 	•	•	↕	↕	⑥	↕
	ASLA													48	2	1		•	•	↕	↕	⑥	↕
	ASLB													58	2	1		•	•	↕	↕	⑥	↕
DOUBLE SHIFT LEFT, Arithmetic	ASLD													05	3	1		•	•	↕	↕	⑥	•
SHIFT RIGHT Arithmetic	ASR							67	6	2	77	6	3				M A B 	•	•	↕	↕	⑥	↕
	ASRA													47	2	1		•	•	↕	↕	⑥	↕
	ASRB													57	2	1		•	•	↕	↕	⑥	↕
SHIFT RIGHT, LOGICAL	LSR							64	6	2	74	6	3				M A B 	•	•	↕	↕	⑥	↕
	LSRA													44	2	1		•	•	↕	↕	⑥	↕
	LSRB													54	2	1				↕	↕		↕
DOUBLE SHIFT RIGHT LOGICAL	LSRD													04	3	1		•	•	R	↕	⑥	↕
																		•	•	R	↕	6	↕
STORE ACCUMULATOR	STAA				97	3	2	A7	4	2	B7	4	3				A→M	•	•	↕	↕	R	•
	STAB				D7	3	2	E7	4	2	B7	4	3				B→M	•	•	↕	↕	R	•
STORE DOUBLE ACCUMULATOR	STAD				DD	4	2	ED	5	2	FD	5	3				A→M B→M+1	•	•	↕	↕	R	•
SUBTRACT	SUBA	80	2	2	90	3	2	A0	4	2	B0	4	3				A−M→A	•	•	↕	↕	↕	↕
	SUBB	C0	2	2	D0	3	2	E0	4	2	F0	4	3				B−M→B	•	•	↕	↕	↕	↕
DOUBLE SUBTRACT	SUBD	83	4	3	93	5	2	A3	6	2	B3	6	3				A:B−M:M+1→AB	•	•	↕	↕	↕	↕
SUBTRACT ACCUMULATORS	SBA													10	2	1	A−B→A	•	•	↕	↕	↕	↕
SUBTRACT WITH CARRY	SBCA	82	2	2	92	3	2	A2	4	2	B2	4	3				A−M−C→A	•	•	↕	↕	↕	↕
	SBCD	C2	2	2	D2	2	2	E2	4	2	F2	4	3				B−M−C→B	•	•	↕	↕	↕	↕
TRANSFER ACCUMULATORS	TAB													16	2	1	A→B	•	•	↕	↕	R	•
	TBA													16	2	1	A→B	•	•	↕	↕	R	•
TEST ZERO OR MINUS	TST							6D	6	2	7D	6	3				M−00	•	•	↕	↕	R	R
	TSTB													5D	2	1	B−00	•	•	↕	↕	R	R

The Condition Code Register notes are listed after Table 10.

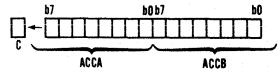
Added Instructions

In addition to the existing S6800 Instruction Set, the following new instructions are incorporated in the S6801 Microcomputer.

ABX Adds the 8-bit unsigned accumulator B to the 16-bit X-Register taking into account the possible carry out of the low order byte of the X-Register. IX←IX +ACCB

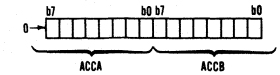
ADDD Adds the double precision ACCD* to the double precision value M:M+1 and places the results in ACCD. ACCD←(ACCD)+(M:M+1)

ASLD Shifts all bits of ACCAB one place to the left. Bit 0 is loaded with zero. The C bit is loaded from the most significant bit of ACCD.



LDD Loads the contents of double precision memory location into the double accumulator A:B. The condition codes are set according to the data. ACCD←(M:M+1)

LSRD Shifts all bits of ACCD one place to the right. Bit 15 is loaded with zero. The C bit is loaded from the least significant bit to ACCD.



MUL Multiplies the 8 bits in accumulator A with the 8 bits in accumulator B to obtain a 16-bit unsigned number in A:B. ACCA contains MSB of result. ACCD←ACCA *ACCB

PSHX The contents of the index register is pushed onto the stack at the address contained in the stack pointer. The stack pointer is decremented by 2. ↓(IXL), SP←(SP)−1 ↓(IXL), SP←(SP)−1

PULX The index register is pulled from the stack beginning at the current address contained in the stack pointer +1. The stack pointer is incremented by 2 in total. SP←(SP)+1; IXH SP←(SP)+1; IHL

STD Stores the contents of double accumulator A:B in memory. The contents of ACCD remain unchanged. M:M+1←(ACCD)

*ACCD is the 16-bit register (A:B) formed by concatenating the A and B accumulators. The A-accumulator is the most significant byte.

Table 8. Index Register and Stack Manipulation Instructions

POINTER OPERATIONS	MNEMONIC	IMMED. OP	IMMED. ~	IMMED. #	DIRECT OP	DIRECT ~	DIRECT #	INDEX OP	INDEX ~	INDEX #	EXTEND OP	EXTEND ~	EXTEND #	IMPLIED OP	IMPLIED ~	IMPLIED #	Boolean/Arithmetic Operation	COND. CODE REG. 5 H	4 I	3 N	2 Z	1 V	0 C
Compare Index Reg	CPX	8C	4	3	9C	5	2	AC	6	2	BC	6	3				$X_H - M$, $X_L - (M+1)$	•	•	⑦	‡	⑧	•
Decrement Index Reg	DEX													09	3	1	X − 1→X	•	•	•	‡	•	•
Decrement Stack Pointer	DES													34	3	1	SP − 1→SP	•	•	•	•	•	•
Increment Index Reg	INX													08	3	1	X + 1→X	•	•	•	‡	•	•
Increment Stack Pointer	INS													31	3	1	1SP + 1→SP	•	•	•	•	•	•
Load Index Reg	LDX	CE	3	3	DE	4	2	EE	5	2	FE	5	3				$M \rightarrow X_H$, $(M+1) \rightarrow X_L$	•	•	⑨	‡	R	•
Load Stack Pointer	LDS	8E	3	3	9E	4	2	AE	5	2	BE	5	3				$M \rightarrow SP_H$, $(M+1) \rightarrow SP_L$	•	•	⑨	‡	R	•
Store Index Reg	STX				DF	4	2	EF	5	2	FF	5	3				$X_H \rightarrow M$, $X_L \rightarrow (M+1)$	•	•	⑨	‡	R	•
Store Stack Pointer	STS				9F	5	2	AF	7	2	BF	6	3				$SP_H \rightarrow M$, $SP_L \rightarrow (M+1)$	•	•	⑨	‡	R	•
Index Reg→Stack Pointer	TXS													35	3	1	X − 1→SP	•	•	•	•	•	•
Stack Pointer→Index Reg	TSX													30	3	1	SP + 1→X	•	•	•	•	•	•
Add	ABX													3A	3	1	B + X→X	•	•	•	•	•	•
Push Data	PSHX													3C	3	1	$X_L \rightarrow M_{SP}$, SP − 1→SP $X_H \rightarrow H_{SP}$, SP − 1→SP	•	•	•	•	•	•
Pull Data	PULX													30	5	1	SP + 1→SP, $M_{SP} \rightarrow X_H$ SP + 1→SP, $M_{SP} \rightarrow X_L$	•	•	•	•	•	•

The Condition Code Register notes are listed after Table 10

Table 9. Jump and Branch Instructions

OPERATIONS	MNEMONIC	RELATIVE OP	RELATIVE ~	RELATIVE #	INDEX OP	INDEX ~	INDEX #	EXTND OP	EXTND ~	EXTND #	IMPLIED OP	IMPLIED ~	IMPLIED #	BRANCH TEST	COND. CODE REG. 5 H	4 I	3 N	2 Z	1 V	0 C
Branch Always	BRA	20	4	2										None	•	•	•	•	•	•
Branch If Carry Clear	BCC	24	4	2										C = 0	•	•	•	•	•	•
Branch If Carry Set	BCS	25	4	2										C = 1	•	•	•	•	•	•
Branch If = 0	BEO	27	4	2										Z = 1	•	•	•	•	•	•
Branch If ≥ Zero	BGE	2C	4	2										N⊕ V = 0	•	•	•	•	•	•
Branch If >Zero	BGT	2E	4	2										Z + (N⊕ V) = 0	•	•	•	•	•	•
Branch If Higher	BHI	22	4	2										C + Z = 0	•	•	•	•	•	•
Branch If≤Zero	BLE	2F	4	2										Z + (N ⊕ V) = 1	•	•	•	•	•	•
Branch If Lower Or Same	BLS	23	4	2										C + Z = 1	•	•	•	•	•	•
Branch If< Zero	BLT	2D	4	2										N ⊕ V = 1	•	•	•	•	•	•
Branch If Minus	BMI	28	4	2										N = 1	•	•	•	•	•	•
Branch If Not Equal Zero	BNE	20	4	2										Z = 0	•	•	•	•	•	•
Branch If Overflow Clear	BVC	28	4	2										V = 0	•	•	•	•	•	•
Branch If Overflow Set	BVS	29	4	2										V = 1	•	•	•	•	•	•
Branch If Plus	BPL	2A	4	2										N = 0	•	•	•	•	•	•
Branch To Subroutine	BSR	8D	8	2											•	•	•	•	•	•
Jump	JMP				6E	4	2	7E	3	3				See Special Operations	•	•	•	•	•	•
Jump To Subroutine	JSR				AD	8	2	8D	9	3					•	•	•	•	•	•
No Operation	NOP										01	2	1	Advances Prog. Cntr. Only	•	•	•	•	•	•
Return From Interrupt	RTI										3B	10	1		⑩					
Return From Subroutine	RTS										39	5	1		•	•	•	•	•	•
Software Interrupt	SWI										3F	12	1	See Special Operations	•	•	•	•	•	•
Wait For Interrupt*	WAI										3E	9	1		•	⑪	•	•	•	•

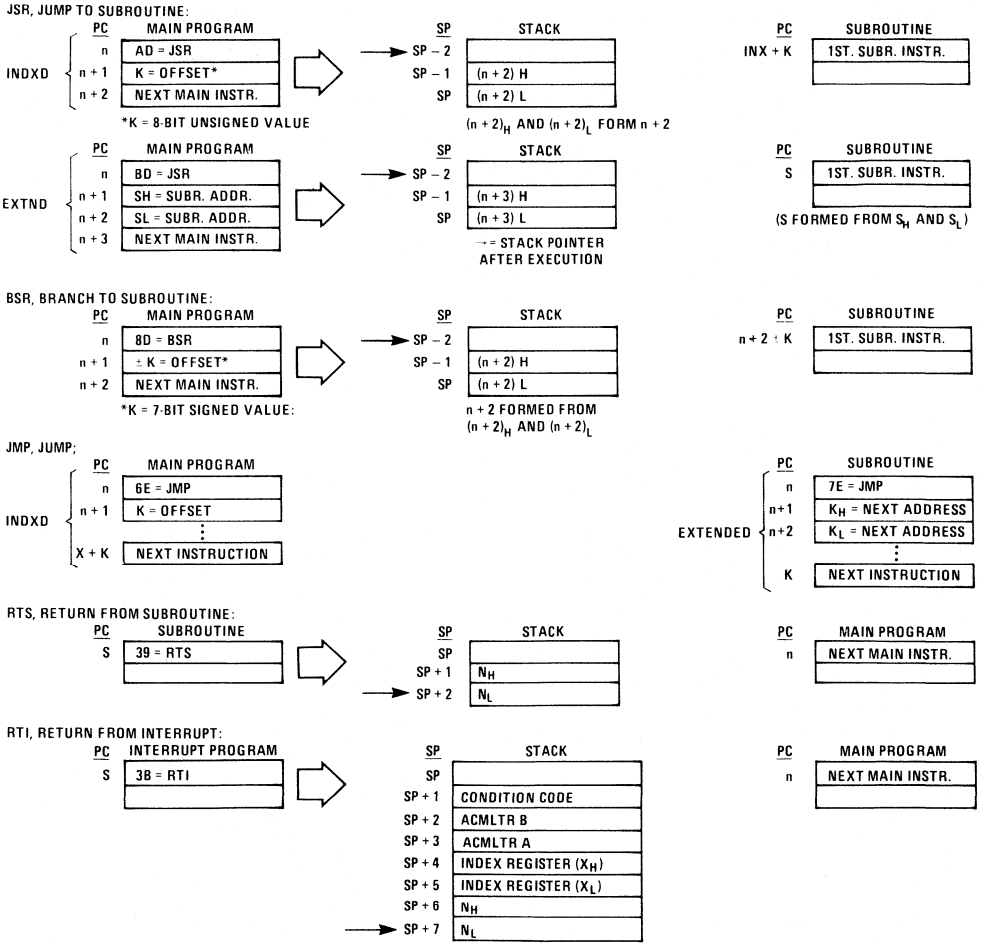
Table 10. Condition Code Register Manipulation Instructions

OPERATIONS	MNEMONIC	IMPLIED OP	IMPLIED ~	IMPLIED #	BOOLEAN OPERATION	COND. CODE REG. 5 H	4 I	3 N	2 Z	1 V	0 C
Clear Carry	CLC	0C	2	1	0→C	•	•	•	•	•	R
Clear Interrupt Mask	CLI	0E	2	1	0→1	•	R	•	•	•	•
Clear Overflow	CLV	0A	2	1	0→V	•	•	•	•	R	•
Set Carry	SEC	0D	2	1	1→C	•	•	•	•	•	S
Set Interrupt Mask	SEI	0F	2	1	1→1	•	S	•	•	•	•
Set Overflow	SEV	0B	2	1	1→V	•	•	•	•	S	•
Accumulator A→CCR	TAP	06	2	1	A→CCR	⑫					
CCR→Accumulator A	TPA	07	2	1	CCR→A	•	•	•	•	•	•

CONDITION CODE REGISTER NOTES: (Bit set if test is true and cleared otherwise).

1 (Bit V) Test Result = 10000000?
2 (Bit C) Test Result = 00000000?
3 (Bit C) Test: Decimal value of most significant BCD Character greater than nine? (Not cleared if previously set.)
4 (Bit V) Test: Operand = 10000000 prior to execution?
5 (Bit V) Test: Operand = 01111111 prior to execution?
6 (Bit V) Test: Set equal to result of N⊕C after shift has occurred.
7 (Bit N) Test: Sign Bit of most significant (MS) byte = 1?
8 (Bit V) Test: 2's complement overflow from subtraction of MS bytes?
9 (Bit N) Test: Result less than zero? (Bit 15 = 1)
10 (All) Load Condition Code Register from Stack. (See Special Operations)
11 (Bit I) Set when interrupt occurs. If previously set, a Non-Maskable Interrupt as required to exit the wait state.
12 (All) Set according to the contents of Accumulator A.

Figure 25. Special Operations



Customer Name _____

Address _____

City _____ State _____ Zip _____

Phone (_____)_____ Extension _____

Contact Ms/Mr _____

Customer Part # _____

ROM Start Address Option

- ☐ $C800
- ☐ $D800
- ☐ $E800
- ☐ $F800
- ☐ A12 and A13 don't care

RAM Start Address Option

- ☐ $0080

Pattern Media

- ☐ 2708 PROM
- ☐ 2716 PROM

Temperature Range

- ☐ 0°C to +70°C

Package Type

- ☐ Ceramic
- ☐ Plastic
- ☐ Cerdip

Marking

- ☐ Standard
- ☐ Special _____

Signature _____

Title _____

AMERICAN MICROSYSTEMS, INC.

S6802/A/B/S6808/A/B

MICROPROCESSOR WITH CLOCK AND RAM

Features

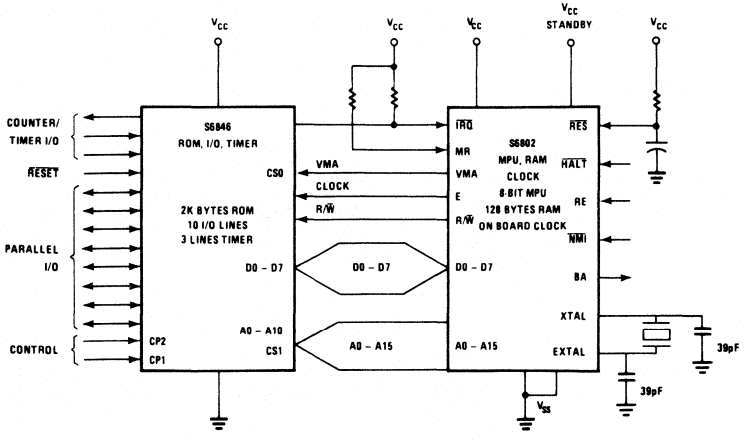
- ☐ On-Chip Clock Circuit
- ☐ 128x8-Bit On-Chip RAM (S6802)
- ☐ 32 Bytes of RAM Are Retainable (S6802)
- ☐ Software-Compatible With the S6800
- ☐ Expandable to 65K Words
- ☐ Standard TTL-Compatible Inputs and Outputs
- ☐ 8-Bit Word Size
- ☐ 16-Bit Memory Addressing
- ☐ Interrupt Capability
- ☐ Clock Rates:
  S6802/S6808—1.0MHz
  S68A02/S68A08—1.5MHz
  S68B02/S68B08—2.0MHz

General Description

The S6802/S6808 are monolithic 8-bit microprocessors that contain all the registers and accumulators of the present S6800 plus an internal clock oscillator and driver on the same chip. In addition, the S6802 has 128 bytes of RAM on board located at hex addresses 0000 to 007E. The first 32 bytes of RAM, at addresses 0000 to 001F, may be retained in a low power mode by utilizing V_{CC} standby, thus facilitating memory retention during a power-down situation. The S6808 is functionally identical to the S6802 except for the 128 bytes of RAM. The S6808 does not have any RAM.

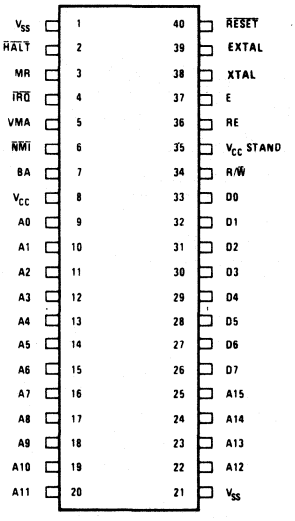
The S6802/S6808 are completely software compatible with the S6800 as well as the entire S6800 family of parts. Hence, the S6802/S6808 are expandable to 65K words. When the S6802 is interfaced with the S6846 ROM-I/O-Timer chip, as shown in the Block Diagram below, a basic 2-chip microcomputer system is realized.

Typical Microcomputer Block Diagram



BLOCK DIAGRAM OF A TYPICAL COST EFFECTIVE MICROCOMPUTER. THE MPU IS THE CENTER OF THE MICROCOMPUTER SYSTEM AND IS SHOWN IN A MINIMUM SYSTEM INTERFACING WITH A ROM COMBINATION CHIP. IT IS NOT INTENDED THAT THIS SYSTEM BE LIMITED TO THIS FUNCTION BUT THAT IT BE EXPANDABLE WITH OTHER PARTS IN THE S6800 MICROCOMPUTER FAMILY.

Pin Configuration



Absolute Maximum Ratings

Supply Voltage, V_{CC}	−0.3V to +7.0V
Input Voltage, V_{IN}	−0.3V to +7.0V
Operating Temperature Range, T_A	0° to +70°C
Storage Temperature Range, T_{stg}	−55°C to +150°C
Thermal Resistance, θ_{JA}	
Plastic	100°C/W
Ceramic	50°C/W

This device contains circuitry to protect the inputs against damage due to high static voltage or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

D.C. Electrical Characteristics (V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = 0°C to +70°C unless otherwise noted.)

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{IH}	Input High Voltage	Logic, EXtal	V_{SS} +2.0	—	V_{CC}	V
		$\overline{Reset}$	V_{SS} +4.0	—	V_{CC}	
V_{IL}	Input Leakage Voltage	Logic, EXtal, $\overline{Reset}$	V_{SS} - 0.3	—	V_{SS} + 0.8	V
I_{IN}	Input Leakage Current (V_{IN} = 0 to 5.25V, V_{CC} = Max)	Logic*	—	1.0	2.5	μA
V_{OH}	Output High Voltage					V
	(I_{LOAD} = - 205μA, V_{CC} = Min)	D0 — D7	V_{SS} +2.4	—	—	V
	(I_{LOAD} = - 145μA, V_{CC} = Min)	A0—A15, R/$\overline{W}$, VMA,E	V_{SS} +2.4	—	—	V
	(I_{LOAD} = - 100μA, V_{CC} = Min)	BA	V_{SS} +2.4	—	—	V
V_{OL}	Output Low Voltage (I_{LOAD} = 1.6mA, V_{CC} = Min)		—	—	V_{SS} + 0.4	V
P_D **	Power Dissipation		—	0.600	1.2	W
C_{IN} •	Capacitance # (V_{IN} = 0, T_A=25°C, f=1.0MHz	D0 — D7	—	10	12.5	pF
		Logic Inputs, EXtal	—	6.5	10	
C_{OUT}		A0 — A15, R/$\overline{W}$, VMA	—	—	12	pF
V_{CC} Standby	V_{CC} Standby		4.0	—	5.25	V
I_{DD} Standby	I_{DD} RAM Standby		—	—	8.0	mA

Clock Timing (V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = 0°C to +70°C unless otherwise noted)

Symbol	Parameter	S6802/S6808 Min.	S6802/S6808 Typ.	S6802/S6808 Max.	S68A02/S68A08 Min.	S68A02/S68A08 Typ.	S68A02/S68A08 Max.	S68B02/S68B08 Min.	S68B02/S68B08 Typ.	S68B02/S68B08 Max.	Unit
f	Frequency of Operation Input Clock ÷ 4	0.1	—	1.0	0.1	—	1.5	.1	—	2	MHz
f_{Xtal}	Crystal Frequency	1.0	—	4.0	1.0	—	6.0	1.0	—	8	
t_{CYC}	Cycle Time	1.0	—	10	1.0	—	6.6	1.0	—	5	μs
$PW_{\phi Hs}$ $PW_{\phi L}$	Clock Pulse Width Measured at 2.4V	450	—	4500	300	—	3000	220	—	2200	ns
t_ϕ	Fall Time Measured between V_{SS}+0.4V and V_{SS}−2.4V	—	—	25	—	—	25	—	—	25	ns

**Except $\overline{IRQ}$ and $\overline{NMI}$, which require 3KΩ pull-up load resistors for wire-OR capability at optimum operation. Does not include Extal and Xtal, which are crystal inputs.*

#Capacitance are periodically sampled rather than 100% tested.

Read/Write Timing (Figures 1 through 5; Load Circuit of Figure 3.)
($V_{CC}=5.0V\pm5\%$, $V_{SS}=0$, $T_A=0°C$ to $+70°C$ unless otherwise noted)

Symbol	Parameter	S6802/S6808			S68A02/S68A08			S68B02/S68B08			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{AD}	Address Delay C=90pF C=30pF		100	270			180 165			150 135	ns
t_{ACC}	Peripheral Read Access Time $t_{ACC}=t_{UT}-(t_{AD}+t_{DSR})$			575			360			250	ns
t_{DSR}	Data Setup Time (Read)	100			60			40			ns
t_H	Input Data Hold Time	10	30		10			10			ns
t_{AH}	Address Hold Time (Address, R/W, VMA)	20			10	75		25			ns
t_{DDW}	Data Delay Time (Write) Processor Controls		165	225		165	200			160	ns
t_{PCS}	Processor Control Setup Time			200	200			200			ns
t_{PCr},t_{PCf}	Processor Control Rise and Fall Time						100			100	ns

Figure 1. Read Data From Memory or Peripherals

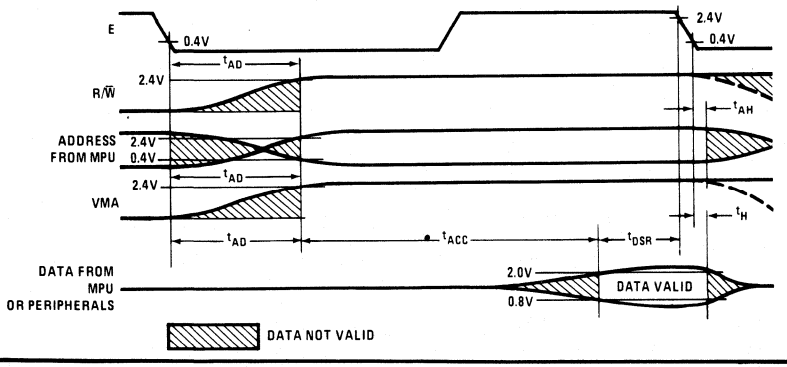


Figure 2. Write Data In Memory or Peripherals

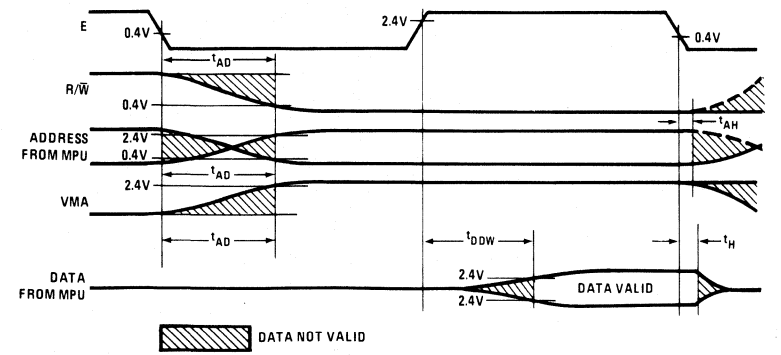
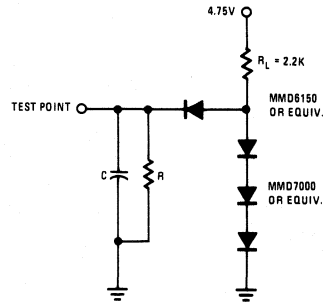


Figure 3. Bus Timing Test Load



C = 130pF FOR D0 – D7, E
= 90pF FOR A0 – A15, R/W, AND VMA
= 30pF FOR BA
R = 11.7 KΩ FOR D0 – D7, E
= 16.5KΩ FOR A0 – A15, R/W, AND VMA
= 24KΩ FOR BA

Figure 4. Typical Data Bus Output Delay Versus Capacitive Loading

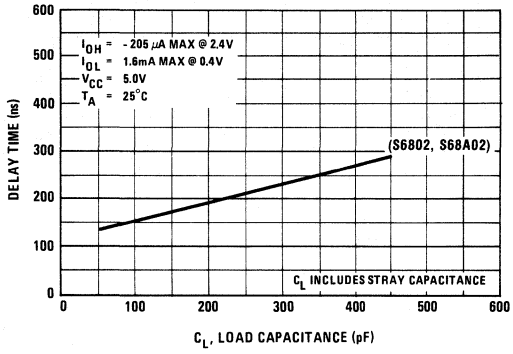


Figure 5. Typical Read/Write, VMA, and Address Output Delay Versus Capacitive Loading

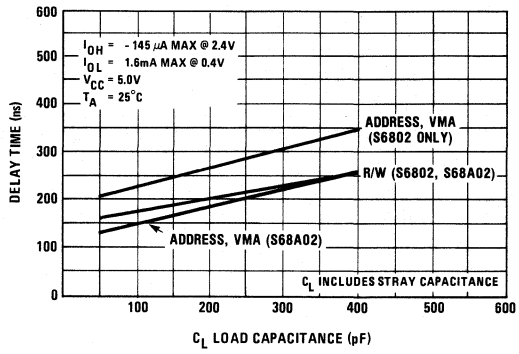
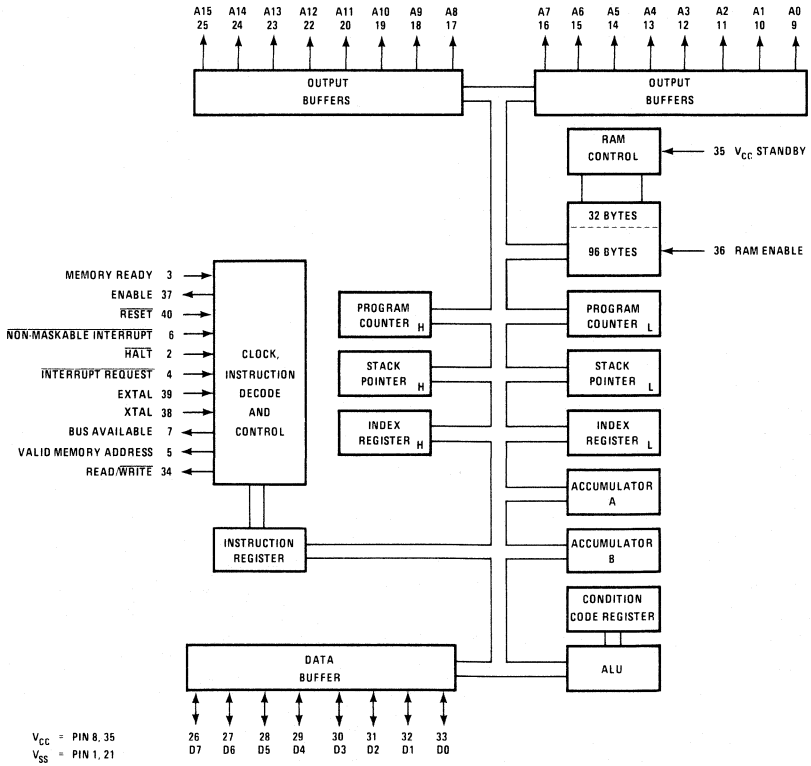


Figure 6. S6802 Expanded Block Diagram



S6802/S6808 MPU Description

Proper operation of the MPU requires that certain control and timing signals be provided to accomplish specific functions and that other signal lines be monitored to determine the state of the processor. These control and timing signals for the S6802/S6808 are identical to those of the S6800 except that TSC, DBE, $\phi 1$, $\phi 2$ input, and two unused pins have been eliminated, and the following signal and timing lines have been added:

RAM Enable (RE)
Crystal Connections EXtal and Xtal
Memory Ready (MR)
V_{CC} Standby
Enable $\phi 2$ Output (E)

The following is a summary of the S6802/S6808 MPU signals:

Address Bus (A0-A15)—Sixteen pins are used for the address bus. The outputs are capable of driving one standard TTL load and 130pF.

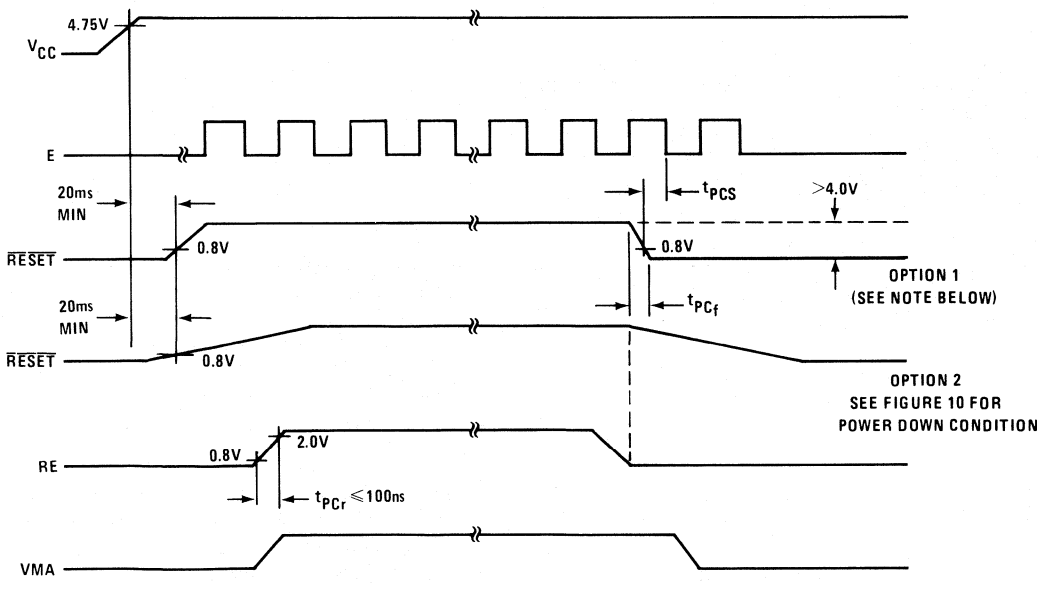
Data Bus (D0-D7)—Eight pins are used for the data bus. It is bi-directional, transferring data to and from the memory and peripheral devices. It also has three-state-output buffers capable of driving one standard TTL load and 130pF.

$\overline{\text{Halt}}$—When this input is in the low state, all activity in the machine will be halted. This input is level sensitive. In the halt mode, the machine will stop at the end of an instruction, Bus Available will be at a high state, Valid Memory Address will be at a low state, and all other three-state lines will be in the three-state mode. The address bus will display the address of the next instruction.

To insure single instruction operation, transition of the $\overline{\text{Halt}}$ line must not occur during the last 200ns of E and the Halt line must go high for one Clock cycle.

Read/$\overline{\text{Write}}$ (R/$\overline{\text{W}}$)—This TTL compatible output signals the peripherals and memory devices whether the MPU is in a Read (high) or Write (low) state. The normal standby state of this signal is Read (high).

Figure 9. Power-up and Reset Timing



NOTE: IF OPTION 1 IS CHOSEN, $\overline{\text{RESET}}$ AND RE PINS CAN BE TIED TOGETHER.

When the processor is halted, it will be in the logical one state. This output is capable of driving one standard TTL load and 90pF.

Valid Memory Address (VMA)—This output indicates to peripheral devices that there is a valid address on the address bus. In normal operation, this signal should be utilized for enabling peripheral interfaces such as the PIA and ACIA. This signal is not three-state. One standard TTL load and 90pF may be directly driven by this active high signal.

Bus Available (BA)—The Bus Available signal will normally be in the low state; when activated, it will go to the high state indicating that the microprocessor has stopped and that the address bus is available. This will occur if the $\overline{\text{Halt}}$ line is in the low state or the processor is in the WAIT state as a result of the execution of a WAIT instruction. At such time, all three-state output drivers will go to their off state and other outputs to their normally inactive level. The processor is removed from the WAIT state by the occurrence of a maskable (mask bit I = 0) or non-maskable interrupt. This output is capable of driving one standard TTL load and 30pF.

$\overline{\text{Interrupt Request}}$ ($\overline{\text{IRQ}}$)—This level sensitive input requests that an interrupt sequence be generated within the machine. The processor will wait until it completes the current instruction that is being executed before it recognizes the request. At that time, if the interrupt mask bit in the Condition Code Register is not set, the machine will begin an interrupt sequence. The Index Register, Program Counter, Accumulators, and Condition Code Register are stored away on the stack. Next the MPU will respond to the interrupt request by setting the interrupt mask bit high so that no further interrupts may occur. At the end of the cycle, a 16-bit address will be loaded that points to a vectoring address which is located in memory locations FFF8 and FFF9. An address loaded at these locations causes the MPU to branch to an interrupt routine in memory.

The $\overline{\text{Halt}}$ line must be in the high state for interrupts to be serviced. Interrupts will be latched internally while $\overline{\text{Halt}}$ is low.

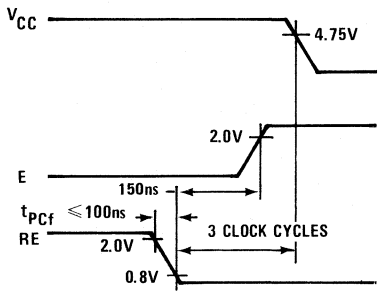
The $\overline{\text{IRQ}}$ has a high impedance pull-up device internal to the chip; however a 3kΩ external resistor to V_{CC} should be used for wire-OR and optimum control of interrupts.

$\overline{\text{Reset}}$—This input is used to reset and start the MPU from a power down condition, resulting from a power failure or an initial start-up of the processor. When this line is low, the MPU is inactive and the information in the registers will be lost. If a high level is detected on the input, this will signal the MPU to begin the restart sequence. This will start execution of a routine to initialize the processor from its reset condition. All the higher order address lines will be forced high. For the restart, the last two (FFFE, FFFF) locations in memory will be used to load the program that is addressed by the program counter. During the restart routine, the interrupt mask bit is set and must be reset before the MPU can be interrupted by $\overline{\text{IRQ}}$. Power-up and reset timing and power-down sequences are shown in Figures 9 and 10, respectively.

When $\overline{\text{RESET}}$ is released it must go through the low to high threshhold without bouncing, oscillating, or otherwise causing an erroneous $\overline{\text{RESET}}$ (less than 3 clock cycles). This may cause improper MPU operation.

$\overline{\text{Reset}}$, when brought low, must be held low at least 3 clock cycles. This allows the S6802/S6808 adequate time to respond internally to reset. This function is independent of the 20ms power up reset that is required.

Figure 10. Power-Down Sequence



Non-Maskable Interrupt (NMI)—A low-going edge on this input requests that a non-mask-interrupt sequence be generated within the processor. As with the $\overline{\text{Interrupt Request}}$ signal, the processor will complete the current instruction that is being executed before it recognizes the $\overline{\text{NMI}}$ signal. The interrupt mask bit in the Condition Code Register has no effect on $\overline{\text{NMI}}$.

The Index Register, Program Counter, Accumulators, and Condition Code Register are stored away on the stack. At the end of the cycle, a 16-bit address will be loaded that points to a vectoring address which is located in memory locations FFFC and FFFD. An address loaded at these locations caused the MPU to branch to a non-maskable interrupt routine in memory.

$\overline{NMI}$ has a high impedance pull-up resistor internal to the chip; however a 3kΩ external resistor to V_{CC} should be used for wire-OR and optimum control of interrupts.

Inputs $\overline{IRQ}$ and $\overline{NMI}$ are hardware interrupt lines that are sampled when E is high and will start the interrupt routine on a low E following the completion of an instruction.

Figure 12 is a flow chart describing the major decision paths and interrupt vectors of the microprocessor. Table 2 gives the memory map for interrupt vectors.

RAM Enable (RE)—A TTL-compatible RAM enable input controls the on-chip RAM of the S6802. When placed in the high state, the on-chip memory is enabled to respond to the MPU controls. In the low state, RAM is disabled. This pin may also be utilized to disable reading and writing the on-chip RAM during power-down situation. RAM enable must be low three clock cycles before V_{CC} goes below 4.75V during power-down to retain the on board RAM contents during V_{CC} standby.

The Data Bus will be in the output mode when the internal RAM is accessed, which prohibits external data from entering the MPU. Note that the internal RAM is fully decoded from $0000 to $007F and these locations must be disabled when internal RAM is accessed.

Extal and Xtal—The S6802/S6808 has an internal oscillator that may be crystal controlled. These connections are for a parallel resonant fundamental crystal. (AT cut) A divide-by-four circuit has been added to the S6802 so that a 4MHz crystal may be used in lieu of a 1MHz crystal for a more cost effective system. Pin 39 of the S6802/S6808 may be driven externally by a TTL input signal if a separate clock is required. Pin 38 is to be left open in this mode. If the external clock is used it may not be halted for more than 4.5μs. The S6802/S6808 is a dynamic part except for internal RAM, and requires the external clock to retain information. Figure 11a shows the crystal parameters. In applications where other than a 4.0MHz crystal is used, Table 1 gives the designer the crystal parameters to be specified. The table contains the entire spectrum of usable crystals for the S6802/S6808. Crystal frequencies not shown (that lie between 1.0MHz and 4.0MHz) may be interpolated from the table. Figure 11b shows the crystal connection.

Table 1. Crystal Parameters

Y1 CRYSTAL FREQUENCY	C1 & C2	C LOAD	R1 (MAX)	C_0 (MAX)
4.0MHz	27pF	24pF	50 ohms	7.0pF
3.58MHz	27pF	20pF	50 ohms	7.0pF
3.0MHz	27pF	18pF	75 ohms	6.7pF
2.5MHz	27pF	18pF	74 ohms	6.0pF
2.0MHz	33pF	24pF	100 ohms	5.5pF
1.5MHz	39pF	27pF	200 ohms	4.5pF
1.0MHz	39pF	30pF	250 ohms	4.0pF

Memory Ready (MR)—MR is a TTL compatible input control signal which allows stretching of E. When MR is high, E will be in normal operation. When MR is low, it may be stretched integral multiples of half periods, thus allowing interface to slow memories. Memory Ready timing is shown in Figure 13.

Enable (E)—This pin supplies the clock for the MPU and the rest of the system. This is a single phase, TTL compatible clock. This clock may be conditioned by a Memory Ready Signal. This is equivalent to ϕ2 on the S6800.

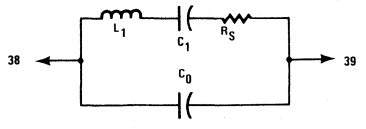
V_{CC} Standby—This pin supplies the dc voltage to the first 32 bytes of RAM as well as the RAM Enable (RE) control logic. Thus retention of data in this portion of the RAM on a power-up, power-down, or standby condition is guaranteed. Maximum current drain at 5.25V is 8mA.

Table 2. Memory Map for Interrupt Vectors

VECTOR MS	VECTOR LS	DESCRIPTION
FFFE	FFFF	RESTART
FFFC	FFFD	NON-MASKABLE INTERRUPT
FFFA	FFFB	SOFTWARE INTERRUPT
FFF8	FFF9	INTERRUPT REQUEST

Note: Memory Read (MR), Halt, RAM Enable (RE) and Non-Maskable interrupt should always be tied to the correct high or low state if not used.

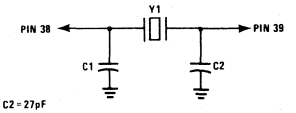
Figure 11a. Crystal Parameters



AT – Cut Parallel Resonance Crystal
C_0 = 7pF Max.
FREQ = 4.0MHz @ C_L = 24pF
R_S = 50 ohms Max.
Frequency Tolerance – ±5% to ±0.02%
The best E output "Worst Case Design" tolerance is ± 0.05% (500ppM) using A ±0.02 crystal.

Tolerance Note:
Critical timing loops may require a better tolerance than ±5%. Because of production deviations and the Temperature Coefficient of the S6802, the best "worst case design" tolerance is ±0.05%. (500 ppm) using a ±0.02% crystal. If the S6802 is not going to be used over its entire temperature range of 0°C to 70°C, a much tighter overall tolerance can be achieved.

Figure 11b. Crystal Connection



AMERICAN MICROSYSTEMS, INC.

PRELIMINARY DATA SHEET

S6805

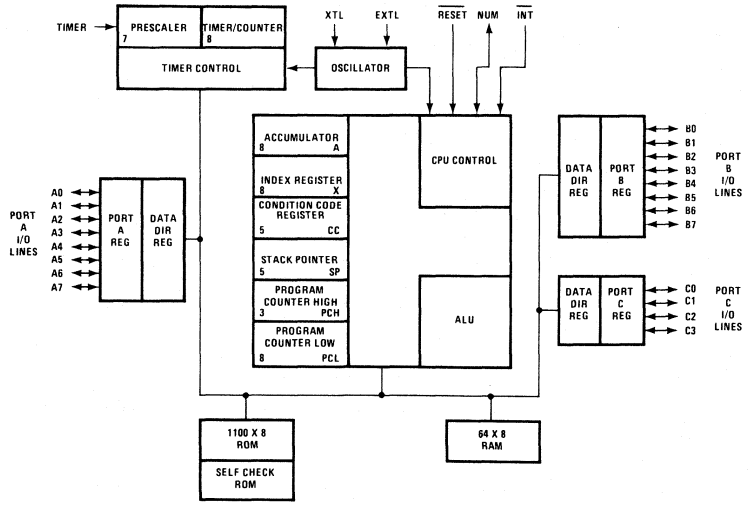
MICROCOMPUTER

Features

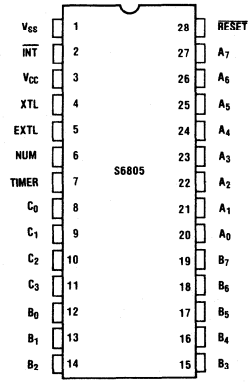
☐ **Hardware**
- 8-Bit Architecture
- 64 Bytes RAM
- 1100 Bytes ROM
- 116 Bytes of Self Check ROM
- 28 Pin Package
- Memory Mapped I/O
- Internal 8-Bit Timer with 7-Bit Prescaler
- Vectored Interrupts — External, Timer, Software, Reset
- 20 TTL/CMOS Compatible I/O Line 8 Lines LED Compatible
- On-Chip Clock Circuit
- Self-Check Capability
- Low Voltage Inhibit
- 5 Vdc Single Supply

☐ **Software**
- Similar to 6800
- Byte Efficient Instruction Set
- Versatile Interrupt Handling
- True Bit Manipulation
- Bit Test and Branch Instruction
- Indexed Addressing for Tables
- Memory Usable as Registers/Flags
- 10 Addressing Modes
- Powerful Instruction Set
  - — All 6800 Arithmetic Instructions
  - — All 6800 Logical Instructions
  - — All 6800 Shift Instructions
  - — Single Instruction Memory Examine/Change
  - — Full Set of Conditional Branches

Block Diagram



Pin Configuration



General Description

The S6805 is an 8-bit single chip microcomputer. It is the first member of the growing microcomputer family that contains a CPU, on-chip clock, ROM, RAM, I/O and timer. A basic feature of the 6805 is an instruction set very similar to the S6800 family of microprocessors. Although the 6805 is not strictly source nor object code compatible, an experienced 6800 user can easily write 6805 code. Also a 6805 user will have no trouble moving up to the 6801 or 6809 for more complex tasks.

Absolute Maximum Ratings

Supply Voltage, V_{CC}	−0.3V to +7.0V
Input Voltage, V_{IN}	−0.3V to +7.0V
Operating Temperature Range, T_A	0° to +70°C
Storage Temperature Range, T_{stg}	−55°C to +150°C
Thermal Resistance, θ_{JA}	
Plastic	85°C/W
Ceramic	50°C/W
CerDIP	51°C/W

This device contains circuitry to protect the inputs against damage due to high static voltage or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{IN} and V_{OUT} be constrained to the range $V_{SS} \le (V_{IN}$ or $V_{OUT}) \le V_{CC}$

Electrical Characteristics: $V_{CC} = +5.25$ Vdc ± Vdc, V_{SS} = GND, $T_A = 0° - 70°C$ unless otherwise noted

Symbol	Characteristic		Min.	Typ.	Max.	Unit
V_{IH}	Input High Voltage	$\overline{RESET}$	4.0	—	V_{CC}	Vdc
V_{IH}		$\overline{INT}$	—	2.2	—	Vdc
V_{IH}		All Other	$V_{SS}+2.0$	—	V_{CC}	Vdc
V_{IH}	Input High	Timer Mode	$V_{SS}+2.0$	—	V_{CC}	Vdc
V_{IH}	Voltage Timer	Self-Check Mode	—	9.0	15.0	Vdc
V_{IL}	Input Low Voltage	$\overline{RESET}$	$V_{SS}-0.3$	—	0.8	Vdc
V_{IL}		$\overline{INT}$	—	2.0	—	Vdc
V_{IL}		All Other	$V_{SS}-0.3$	—	$V_{SS}+0.8$	Vdc
V_H	$\overline{INT}$ Hysteresis		—	100	—	mV_{CC}
P_D	Power Dissipation		—	350	—	mW
C_{IN}	Input Capacitance	EXTL	—	20	—	pF
C_{IN}		All Other	—	10	—	pF
LVR	Low Voltage Recover		—	—	4.75	Vdc
LVI	Low Voltage Inhibit		—	4.5	—	

Switching Characteristics: $V_{CC} = +5.25$ V ± 0.5 Vdc, V_{SS} = GND, $T_A = 0° - 70°C$ unless otherwise noted

Symbol	Characteristic	Min.	Typ.	Max.	Unit
f_{cl}	Clock Frequency	0.4	—	4.0	MHz
t_{CYC}	Cycle Time	1.0	—	10	μs
t_{IWL}	$\overline{INT}$ Pulse Width	$t_{CYC}+250$	—	—	ns
t_{RWL}	$\overline{RESET}$ Pulse Width	$t_{CYC}+250$	—	—	ns
t_{RHL}	Delay Time Reset (External Cap. = 0.47μF)	20	50	—	ms

Port Electrical Characteristics: V_{CC} = +5.25 Vdc ± 0.5 Vdc, V_{SS} = GND, T_A = 0° – 70°C unless otherwise noted

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Condition
			Port A			
V_{OL}	Output Low Voltage	–	–	0.4	Vdc	I_{LOAD} = 1.6mAdc
V_{OH}	Output High Voltage	2.4	–	–	Vdc	I_{LOAD} = 100μAdc
V_{OH}	Output High Voltage	3.5	–	–	Vdc	I_{LOAD} = −10μAdc
V_{IH}	Input High Voltage	V_{SS} + 2.0	–	V_{CC}	Vdc	I_{LOAD} = −300μAdc (max)
V_{IL}	Input Low Voltage	V_{SS} − 0.3	–	V_{SS} + 0.8	Vdc	I_{LOAD} = −500μAdc (max)
			Port B			
V_{OL}	Output Low Voltage	–	–	0.4	Vdc	I_{LOAD} = 3.2mAdc
V_{OL}	Output Low Voltage	–	–	1.0	Vdc	I_{LOAD} = 10mAdc(sink)
V_{OH}	Output High Voltage	2.4	–	–	Vdc	I_{LOAD} = −200μAdc
I_{OH}	Darlington Current Drive (Source)	−1.0	–	−10	mAdc	V_O = 1.5Vdc
V_{IH}	Input High Voltage	V_{SS} + 2.0	–	V_{CC}	Vdc	
V_{IL}	Input Low Voltage	V_{SS} − 0.3	–	V_{SS} + 0.8	Vdc	
			Port C			
V_{OL}	Output Low Voltage	–	–	0.4	Vdc	I_{LOAD} = 1.6mAdc
V_{OH}	Output High Voltage	2.4	–	–	Vdc	I_{LOAD} = −100 μAdc
V_{IH}	Input High Voltage	V_{SS} + 2.0	–	V_{CC}	Vdc	
V_{IL}	Input Low Voltage	V_{SS} − 0.3	–	V_{SS} + 0.8	Vdc	
			Off-State Input Current			
I_{TSI}	Three-State Ports B & C	–	2	20	μAdc	
			Input Current			
I_{IN}	Timer at V_{IN} = (0.4 to 2.4 Vdc)	–	–	20	μAdc	

Figure 1. TTL Equiv. Test Load (Port B)

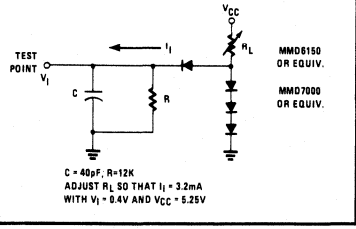


Figure 2. CMOS Equiv. Test Load (Port A)

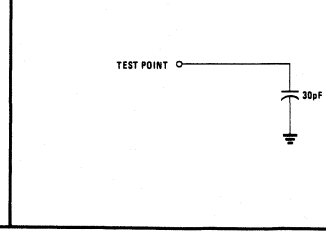
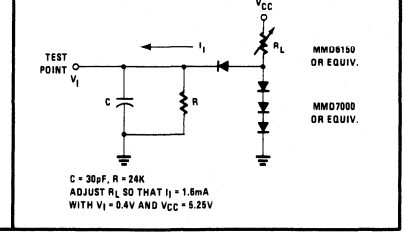


Figure 3. TTL Equiv. Test Load (Ports A and C)



Pin Description

Pin	Symbol	Description
1 and 3	V_{CC} and V_{SS}	Power is supplied to the MCU using these two pins. V_{CC} is 5.25V ± .5V, and V_{SS} is the ground connection.
2	$\overline{INT}$	External Interrupt provides capability to apply an external interrupt to the MCU.
4 and 5	XTL and EXTL	Provide control input for the on-chip clock circuit. The use of crystal (at cut 4MHz maximum), a resistor or a wire jumper is sufficient to drive the internal oscillator with varying degrees of stability. (See Internal Oscillator Options for recommendations) An internal divide by 4 prescaler scales the frequency down to the appropriate $\phi 2$ clock rate (1MHz maximum).
6	NUM	This pin is not for user application and should be connected to ground.
7	TIMER	Allows an external input to be used to decrement the internal timer circuitry. See TIMER for detailed information about the timer circuitry.
8-11 12-19 20-27	C0-C3 B0-B7 A0-A7	Input/Output lines (A0-A7, B0-B7, C0-C3). The 20 lines are arranged into two 8-bit ports (A and B) and one 4-bit port (C). All lines are programmed as either inputs or outputs under software control of the data direction registers. See Inputs/Outputs for additional information.
28	$\overline{RESET}$	This pin allows resetting of the MCU. A low voltage detect feature responds to a dip in voltage by forcing a RESET condition to clear all Data Direction Registers, so that all I/O pins are set as inputs.

Memory

The MCU memory is configured as shown in Figure 4. During the processing of an interrupt, the contents of the MCU registers are pushed onto the stack in the order shown in Figure 5. Since the stack pointer decrements during pushes, the low order byte (PCL) of the program counter is stacked first, then the high order three bits (PCH) are stacked first, then the high order three bits (PCH) are stacked. This ensures that the program counter is loaded correctly as the stack pointer increments when it pulls data from the stack. A subroutine call will cause only the program counter (PCH, PCL) contents to be pushed onto the stack.

Figure 4. MCU Memory Configuration

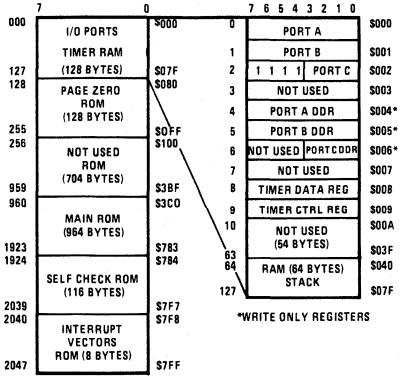
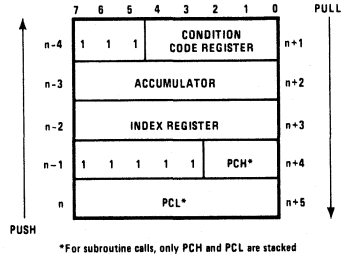


Figure 5. Interrupt Stacking Order



input pin allowing the user to easily perform pulse-width measurements. The source of the clock input is one of the options that has to be specified before manufacture of the MCU. A prescaler option can be applied to the clock input that extends the timing interval up to a maximum of 128 counts before being applied to the counter. This prescaling option must also be specified before manufacturing begins. The timer continues to count past zero and its present count can be monitored at any time by monitoring the timer data register. This allows a program to determine the length of time since a timer interrupt has occurred and not disturb the counting process.

At power up or reset the prescaler and counter are initialized with all logical ones; the timer interrupt request bit (bit 7) is cleared and the timer request mask bit (bit 6) is set.

Self Check Mode:

The MCU includes a non-user mode pin that replaces the normal operating mode with one in which the internal data and address buses are available at the I/O ports. The ports are configured as follows in the test mode (some multiplexing of the address and data lines is necessary):

- The internal ROM and RAM are disabled and Port A becomes the input data bus on the $\phi 2$ of the clock and can be used to supply instructions of data to the MCU.
- Port B is also multiplexed. When $\phi 2$ is high, Port B is the output data bus, and when $\phi 2$ is low Port B is the address lines. The output data bus can be used to monitor the internal ROM or RAM.
- Port C becomes the last three address lines and a read/write control line.

The MCU incorporates a self test program within a 116 byte non-user accessable test program and some control logic on-chip. These 116 bytes of ROM test every addressing mode and nearly every CPU instruction (95% of the total microprocessor capability) while only adding 1% to the total overall die size.

To perform the self test, the MCU output lines of Port A and B must be externally interconnected (Figure 7) and LED's are connected to Port C to provide both a pass/fail indication (3Hz square wave).

The flowchart for the self test program (Figure 8) runs four tests:

- **I/O TEST:** Tests for I/O lines that are stuck in high, low, shorted state, or are missing a connection. The I/O lines are all externally wired together so that the program can look for problems by testing for the correct operation of the lines as inputs and outputs and for shorts between two adjacent lines.
- **ROM ERROR:** (Checksum wrong). The checksum value of the user program must be masked into the self check ROM when the microcomputer is built. The self check program then tests the user ROM by computing the checksum value, which should be equal to the masked checksum if all the bits in the ROM are properly masked. Address and data lines that are stuck high, low or to each other are also detected by this test. An inoperable ROM will (in most cases) prevent the running of the self check program.

Figure 7. Timer Block Diagram

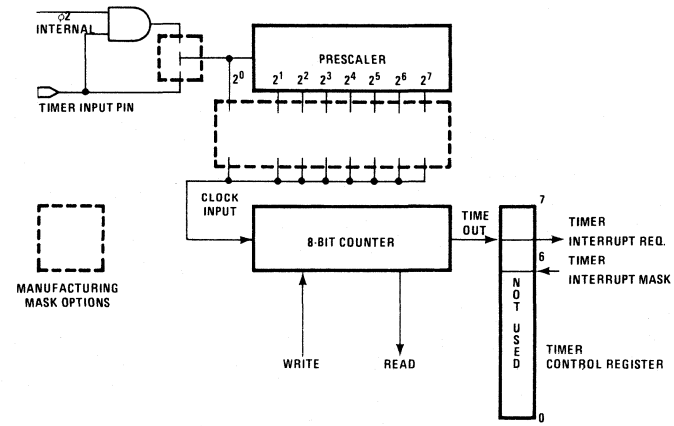
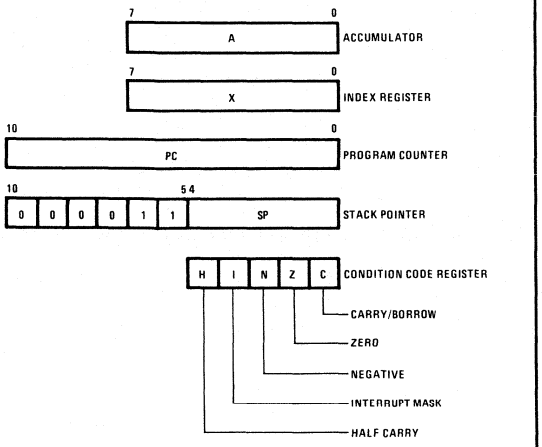


Figure 6. Programming Model



Registers

The S6805 MCU contains two 8-bit registers (A and X), one 11-bit register (PC), two 5-bit registers (SP and CC) that are visible to the programmer (see Figure 6).

Accumulator (A)

The A-register is an 8-bit general purpose accumulator used for arithmetic calculations and data manipulation.

Index Register (X)

This 8-bit register is used for the indexed addressing mode. It provides an 8-bit address that may be added to an offset to create an effective address. The index register can also be used for limited calculations and data manipulations when using the read/modify/write instructions. In code sequences not employing the index register it can be used as a temporary storage area.

Program Counter (PC)

This 11-bit register contains the address of the next instruction to be executed.

Stack Pointer (SP)

The stack pointer is an 11-bit register that contains the address of the next free location on the stack. Initially, the stack pointer is set to location $07F and is decremented as data is being pushed onto the stack and incremented as data is being pulled from the stack. The six most significant bits of the stack pointer are permanently set to 000011. During an MCU reset or the reset stack pointer (RSP) instruction, the stack pointer is set to location $07F. Subroutines and interrupts may be nested down to location $061 which allows the programmer to use up to 15 levels of subroutine calls. A 16th subroutine call would save the return address correctly, but the stack pointer would not remain pointing into the stack area and there would be no way to return from any of the subroutines.

Condition Code Register (CC)

The condition code register is a 5-bit register in which each bit is used to indicate or flag the results of the instruction just executed. These bits can be individually tested by a program and specific action taken as a result of their state. Each individual condition code register bit is explained in the following paragraphs.

HALF CARRY (H)—Used during arithmetic operations (ADD and ADC) to indicate that a carry occurred between bits 3 and 4.

INTERRUPT (I)—This bit is set to mask the timer and external interrupt ($\overline{\text{INT}}$). If an interrupt occurs while this bit is set it is latched and will be processed as soon as the interrupt bit is reset.

NEGATIVE (N)—USED TO INDICATE that the result of the last arithmetic, logical or data manipulation was negative (bit 7 in result equal to a logical one).

ZERO (Z)—Used to indicate that the result of the last arithetic, logical or data manipulation was zero.

CARRY/BORROW (C)—Used to indicate that a carry or borrow out of the arithmetic logic unit (ALU) occurred during the last arithmetic operation. This bit is also affected during bit test and branch instructions, shifts and rotates.

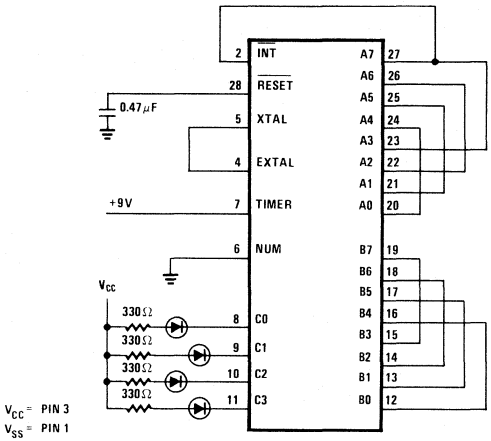
Timer

The MCU timer circuitry is shown in Figure 7. The 8-bit counter is loaded under program control and counts down toward zero as soon as the clock input is applied. When the timer reaches zero the timer interrupt request bit (bit 7) in the timer control register is set. The MCU redsponds to this interrupt by saving the present MCU state in the stack, fetching the timer interrupt vector from locations $7F8 and $7F9 and executing the interrupt routine. The timer interrupt can be masked by setting the timer interrupt mask bit (bit 6) in the timer control register. The interupt bit (bit 1) in the condition code register will also prevent a timer interrupt from being processed.

The clock input to the timer can be from an external source applied to the TIMER input pin or it can be the internal $\phi 2$ signal. Note that when $\phi 2$ signal is used as the source it can be gated by an input applied to the TIMER

• **RAM Bits Non-Functional**: The RAM is tested by the use of a walking bit pattern that is written into memory and then verified. Every in RAM is set to one and then to zero by using 9 different patterns as shown in Figure 9.

Figure 8. Interconnected Ports for Self Check Mode. Port C Gives Go/No Go and Diagnostic Information.



Self Test Routines

Program performs four main tests in the major loops and provides an output signal to indicate that the part is functional.

Interrupt Logic Failure: Using an I/O line the interrupt pin is toggled to create an interrupt. The main program runs long enough to allow the timer to underflow and causes the timer interrupt to be enabled.

If all of these tests are successful the program, then loops back to the beginning and starts testing again.

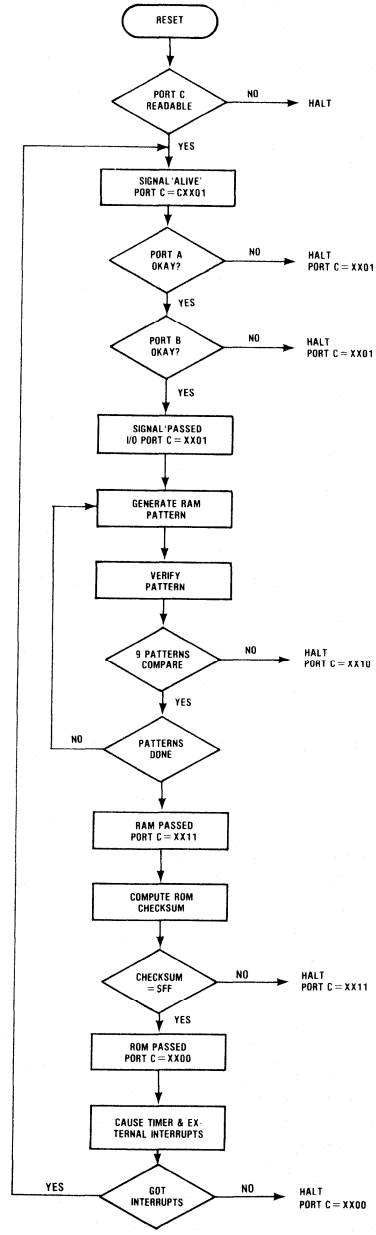
The self check program initially tries to get the MCU out of the reset state to indicate that the processor is at least working. The non-functional parts are thus immediately eliminated, and if the part fails at this first stage the program provides a means of determining the faulty section.

To place the MCU in the self check mode the voltage on the timer input (Figure 7) is raised to 8 volts which causes several operations to take place:

• The clocking source for the timer is shunted to the MCU internal clock to insure that the timer will run an underflow during the course of the program, no matter which clocking rate is masked.

• The address of the interrupt vectors (including the reset vector) are mapped into the self check ROM area. This allows the self check to test the interrupt structure.

Figure 9. Flowchart of Self Test Routines



The self check program is started by the reset signal instead of the normal program because the vectors (including the reset vector) have been overlaid. The self check program runs in an endless loop testing and retesting the processor as long as there are no errors. Signals on the I/O lines indicate that the test has passed, and if any test fails, the program stops by executing a branch to self instruction. The output lines then cease to toggle and two of the I/O lines will indicate the cause of failure.

RAM Test Pattern

"Walking bit" patterns test sequence sets and resets every bit in memory. (See Figure 10.)

Low Voltage Inhibit

As soon as the voltage at pin 3 (V_{CC}) falls to 4.5 volts, all I/O lines are put into a high impedance state. This prevents erroneous data from being given to an external device. When V_{CC} climbs back up to 4.6 volts a vectored reset is performed.

Table 1. Cause of Chip Failure as Shown in Bits 0 and 1 of I/O Port C

BIT 1	BIT 0	REASON FOR FAILURE
0	0	INTERRUPTS
0	1	I/O PORTS A OR B
1	0	RAM
1	1	ROM

Figure 10. RAM Test Pattern

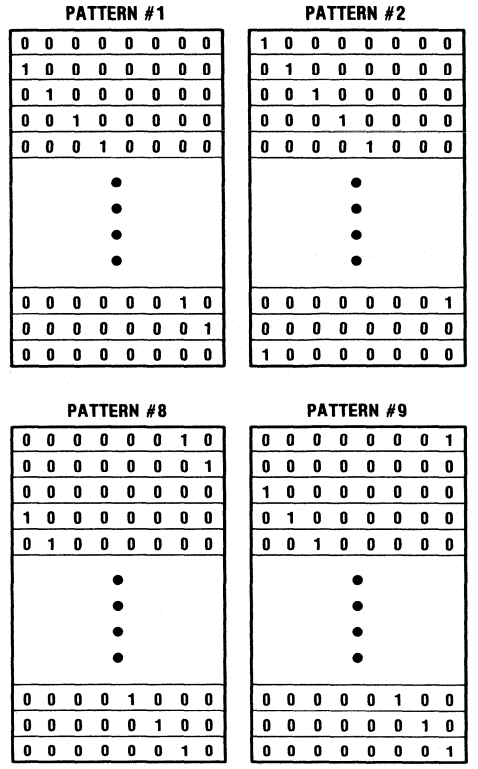
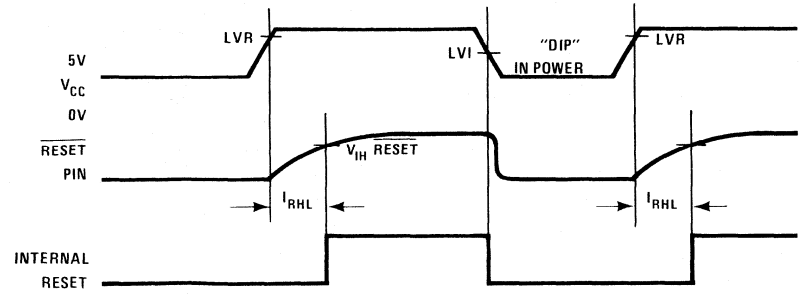


Figure 11. Power Up and Reset Timing

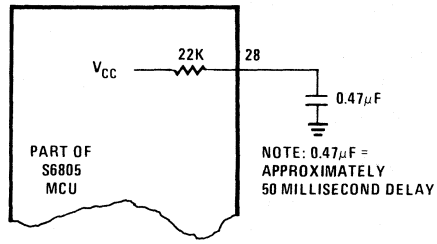


Resets

The MCU can be reset three ways; by the external reset input ($\overline{\text{RESET}}$), by the internal low voltage detect circuit already mentioned, and during the power up time. (See Figure 11.)

Upon power up, a minimum of 20 milliseconds is needed before allowing the reset input to go high. This time allows the internal oscillator to stabilize. Connecting a capacitor to the $\overline{\text{RESET}}$ input as shown in Figure 12 will provide sufficient delay.

Figure 12. Power Up Reset Delay Circuit



Internal Oscillator Options

The internal oscillator circuit has been designed to require a minimum of external components. The use of a crystal (AT cut, 4MHz max) or a resistor is sufficient to drive the internal oscillator with varying degrees of stability. A manufacturing mask option is available to provide better matching between the external components and the internal oscillator.

The different connection methods are shown in Figure 13. Crystal specifications are given in Figure 14. A resistor selection graph is given in Figure 15.

Figure 13. Internal Oscillator Options

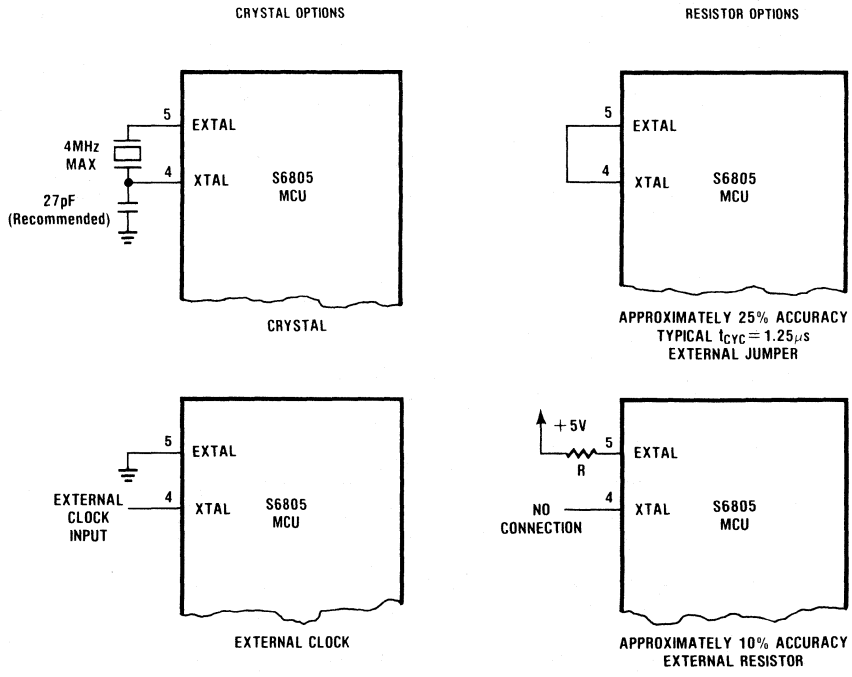
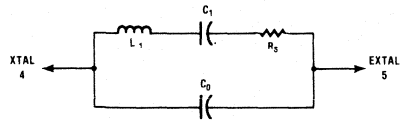
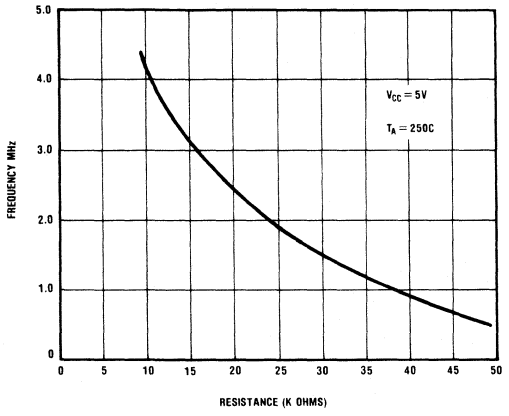


Figure 14. Crystal Parameters



AT–CUT PARALLEL RESONANCE CRYSTAL
C_0 = 7pF MAX
FREQ = 4.0MHz @ C_L = 24pF
R_S = 50 OHMS MAX

Figure 15. Typical Resistor Selection Graph



Interrupts

The MCU can be interrupted three different ways; through the external interrupt ($\overline{INT}$) input pin, the internal timer interrupt request, and a software interrupt instruction (SWI). When any interrupt occurs, processing is suspended, the present MCU state is pushed onto the stack, the interrupt bit (I) in the condition code register is set, the address of the interrupt routine is obtained from the appropriate interrupt vector address, and the interrupt routine is executed. The interrupt service routines normally end with a return from interrupt (RTI) instruction which allows the MCU to resume processing of the program prior to the interrupt. Table 1 provides a listing of the interrupts, their priority, and the vector address that contain the starting address of the appropriate interrupt routine.

A sinusodial signal (1kHz maximum) can be used to generate an external interrupt ($\overline{INT}$) as shown in Figure 16.

A flowchart of the interrupt processing sequence is given in Figure 17.

Table 1. Interrupt Priorities

Interrupt	Priority	Vector Address
$\overline{RESET}$	1	$7FE AND $7FF
SWI	2	$7FC AND $7FD
$\overline{INT}$	3	$7FA AND $7FB
TIMER	4	$7F8 AND $7F9

Input/Output

There are 20 input/output pins. All pins are programmable as either inputs or outputs under software control of the data direction registers. When programmed as outputs, all I/O pins read latched output data regardless of the logic level at the output pin due to output loading (see Figure 18). When port B is programmed for outputs, it is capable of sinking 10 milliamperes on each pin (one volt maximum). All input/output lines are TTL compatible as both inputs and outputs. Port A lines are CMOS compatible as outputs while Port B and C lines are CMOS compatible as inputs. Figure 19 provides some examples of port connections.

Figure 16. Typical Sinusodial Interrupt Circuits

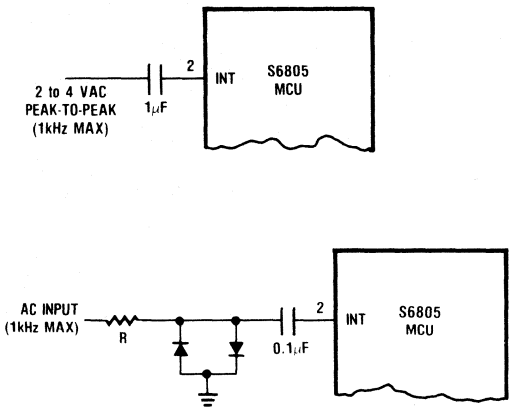


Figure 17. Interrupt Processing Flowchart

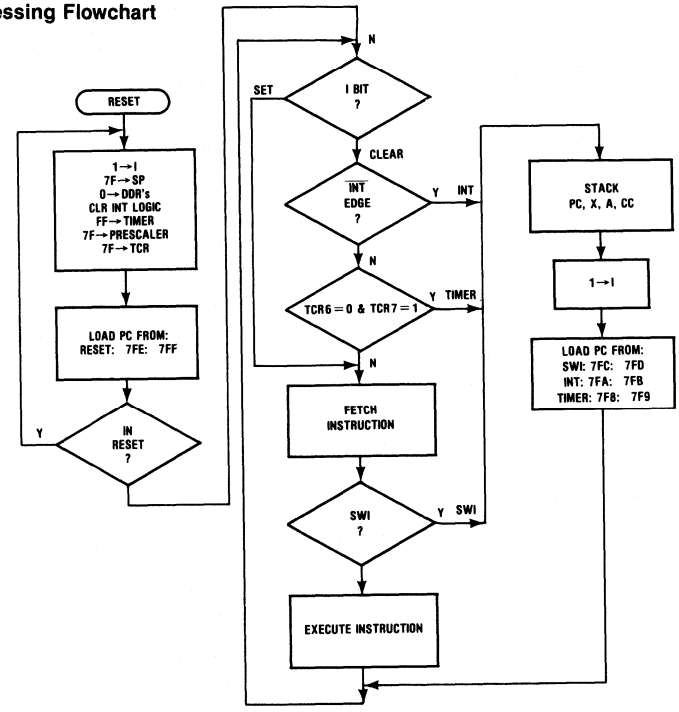
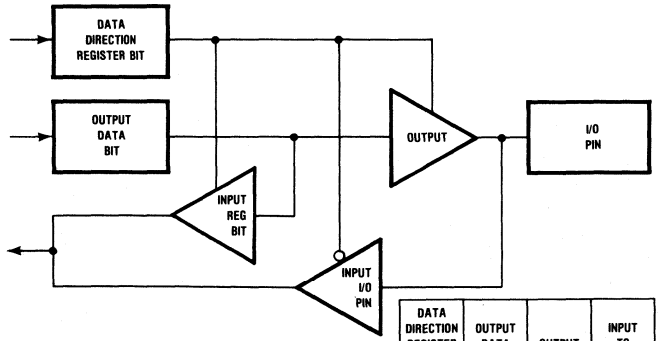
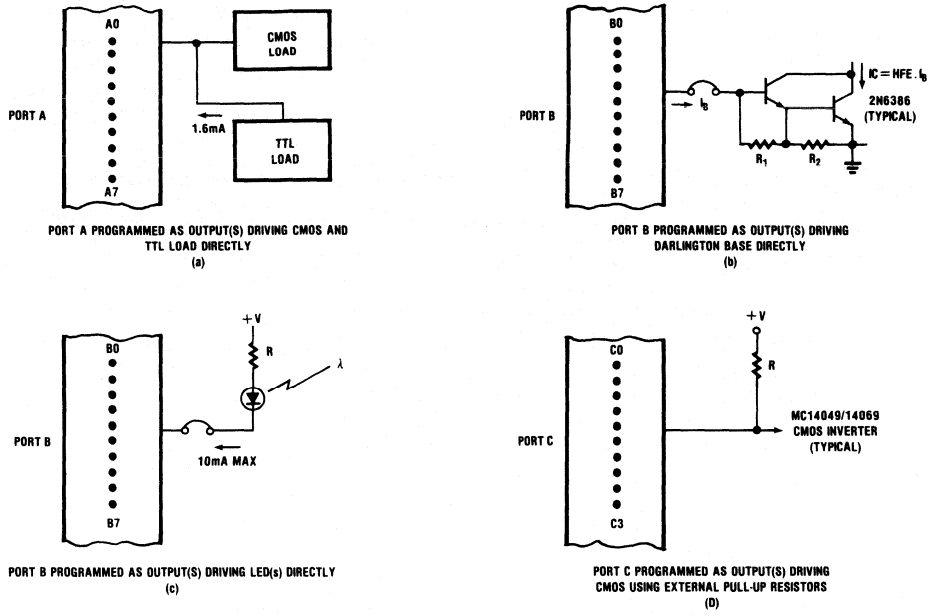


Figure 18. Typical Port I/O Circuitry



DATA DIRECTION REGISTER BIT	OUTPUT DATA BIT	OUTPUT STATE	INPUT TO MCU
1	0	0	0
1	1	1	1
0	X	3-STATE	PIN

Figure 19. Typical Port Connections



Bit Manipulation

The MCU has the ability to set or clear any single random access memory or input/output bit (except the data direction registers) with a single instruction (BSET, BCLR). Any bit in the page zero read only memory can be tested, using the BRSET and BRCLR instructions, and the program branches as a result of its state. This capability to work with any bit in RAM, ROM or I/O allows the user to have individual flags in RAM or to handle single I/O bits as control lines. The example in Figure 20 illustrates the usefulness of the bit manipulation and test instructions. Assume that bit 0 of port A is connected to a zero crossing detector circuit and that bit 1 of port A is connected to the trigger of a TRIAC which powers the controlled hardware.

This program, which uses only seven ROM locations, provides turn-on of the TRIAC within 14 microseconds of the zero crossing. The timer could also be incorporated to provide turn-on at some later time which would permit pulse-width modulation of the controlled power.

Addressing Modes

The MCU has ten addressing modes available for use by the programmer. They are explained and illustrated briefly in the following paragraphs.

Figure 20. Bit Manipulation Example

```
        •
        •
        •
        •
        •
SELF 1  BRCLR 0, PORTA, SELF 1
        BSET 1, PORTA
        BCLR 1, PORTA
        •
        •
        •
        •
        •
```

Immediate—Refer to Figure 21. The immediate addressing mode accesses constants which do not change during program execution. Such instructions are two bytes long. The effective address (EA) is the PC and the operand is fetched from the byte following the opcode.

Direct—Refer to Figure 22 in direct addressing, the address of the operand is contained in the second byte of the instruction. Direct addressing allows the user to directly address the lowest 256 bytes in memory. All RAM space, I/O registers and 128 bytes of ROM are located in page zero to take advantage of this efficient memory addressing mode.

Extended—Refer to Figure 23. Extended addressing is used to reference any location in memory space. The EA is the contents of the two bytes following the opcode. Extended addressing instructions are three bytes long.

Relative—Refer to Figure 24. The relative addressing mode applies only to the branch instructions. In this mode the contents of the byte following the opcode is added to the program counter when the branch is taken. EA=(PC)+2+Rel. Rel is the contents of the location following the instruction opcode with bit 7 being the sign bit. If the branch is not tken Rel=0, when a branch takes place, the program goes to somewhere within the range of +129 bytes to −127 of the present instruction. These instructions are two bytes long.

Indexed (No Offset)—Refer to Figure 25. This mode of addressing accesses the lowest 256 bytes of memory. These instructions are one byte long and their EA is the contents of the index register.

Indexed (8-Bit Offset)—Refer to Figure 26. The EA is calculated by adding the contents of the byte following the opcode to the contents of the index register. In this mode, 511 low memory locations are accessable. These instructions occupy two bytes.

Indexed (16-Bit Offset)—Refer to Figure 27. This addressing mode calculates the EA by adding the contents of the two bytes following the opcode to the index register. Thus, the entire memory space may be accessed. Instructions which use this addressing mode are three bytes long.

Bit Set/Clear—Refer to Figure 28. This mode of addressing applies to instructions which can set or clear any bit on page zero. The lower three bits in the opcode specify the bit to be set or cleared while the byte following the opcode specifies the address in page zero

Bit Test and Branch—Refer to Figure 29. This mode of addressing applies to instructions which can test any bit in the first 256 locations ($00-$FF) and branch to any location relative to the PC. The byte to be tested is addressed by the byte following the opcode. The individual bit within that byte to be tested is addressed by the lower three bits of the opcode. The third byte is the relative address to be added to the program counter if the branch condition is met. These instructions are three bytes long. The value of the bit tested is written to the carry bit in the condition code register.

Inherent—Refer to Figure 30. The inherent mode of addressing has no EA. All the information necessary to execute an instruction is contained in the opcode. Direct operations on the accumulator and the index register are included in this mode of addressing. In addition, control instructions such as SWI. RTI belong to this group. All inherent addressing instructions are one byte long.

Figure 21. Immediate Addressing Example

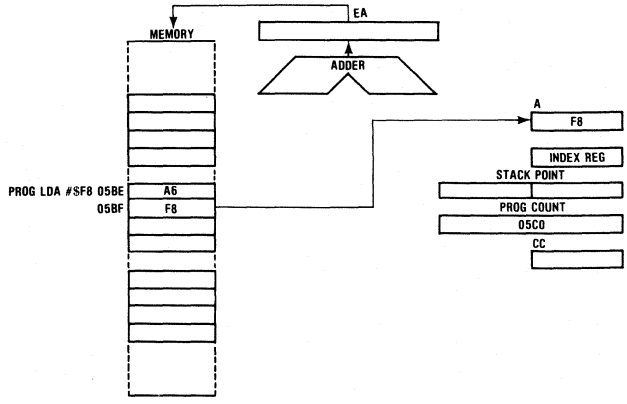


Figure 22. Direct Addressing Example

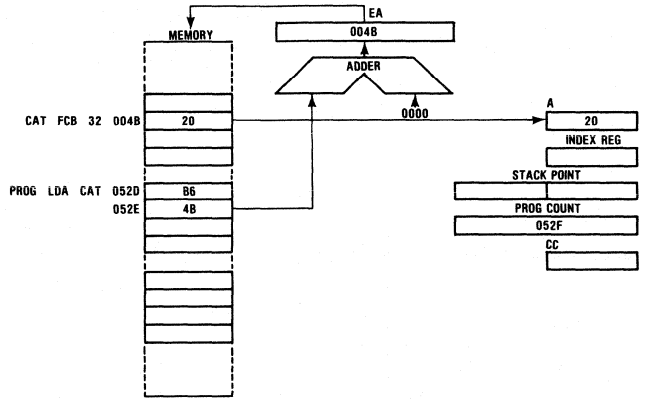


Figure 23. Extended Addressing Example

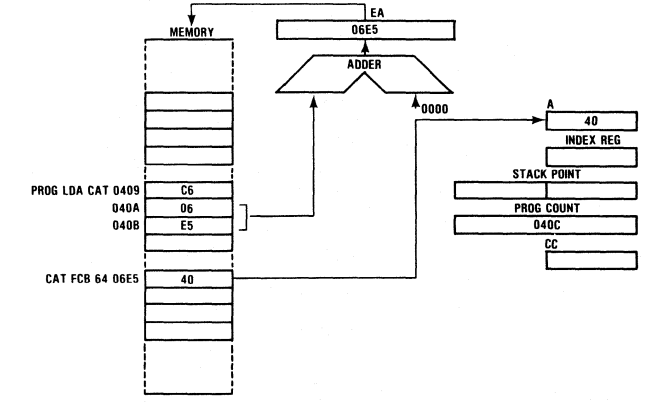


Figure 24. Relative Addressing Example

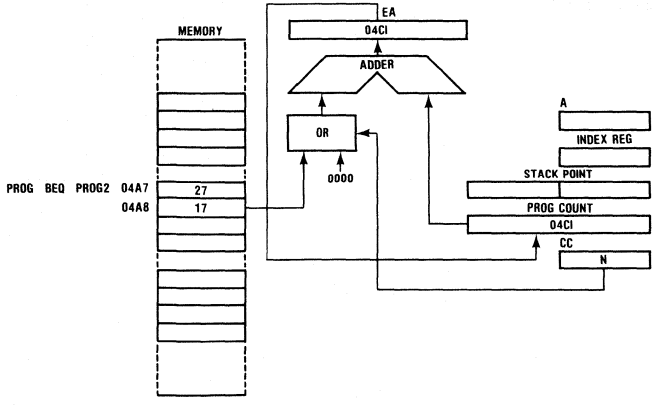


Figure 25. Indexed (No Offset) Addressing Example

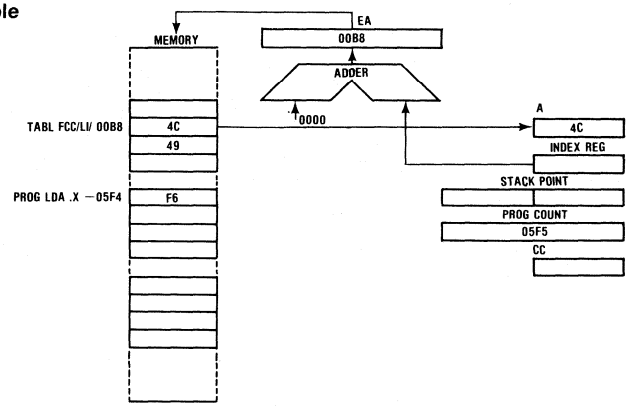


Figure 26. Indexed (8-Bit Offset) Addressing Example

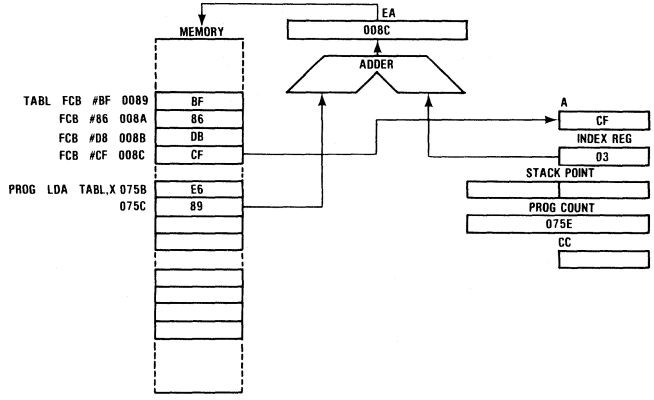


Figure 27. Indexed (16-Bit Offset) Addressing Example

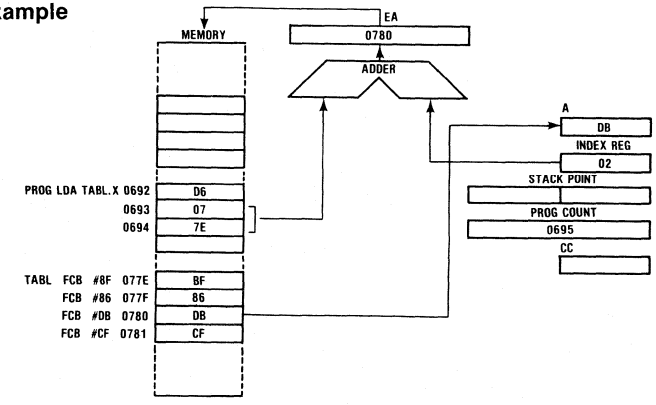


Figure 28. Bit Set/Clear Addressing Example

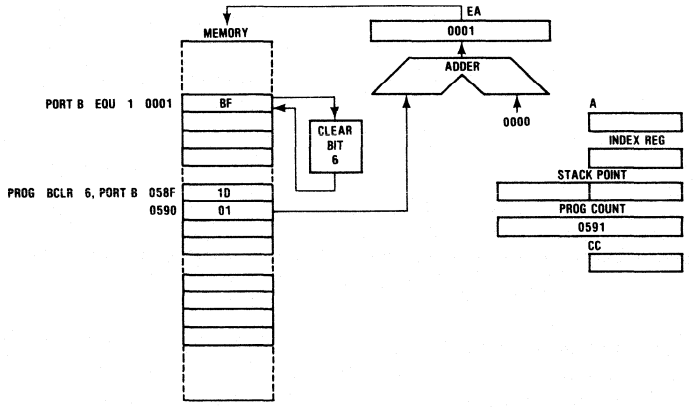


Figure 29. Bit Test and Branch Addressing Example

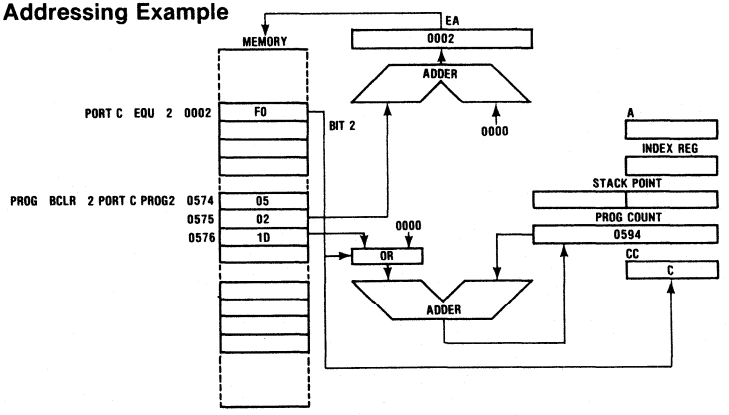
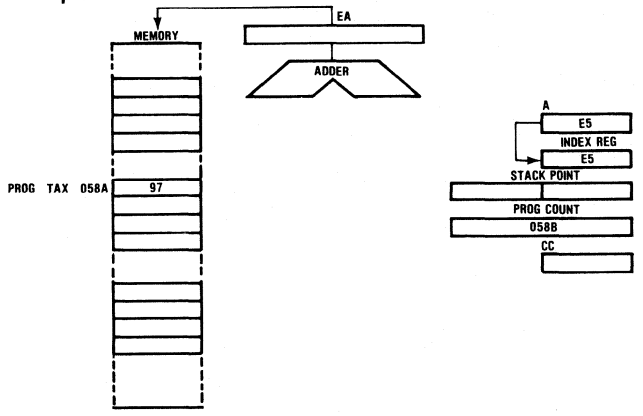


Figure 30. Inherent Addressing Example



Instruction Set

The MCU has a set of 59 basic instructions. They can be divided into five different types: register/memory, read/modify/write, branch, bit manipulation, and control. The following paragraphs briefly explain each type. All the instructions within a given type are presented in individual tables.

Register/Memory Instructions—Most of these instructions use two operands. One operand is either the accumulator or the index register. The other operand is obtained from memory using one of the addressing modes. The jump unconditional (JMP) and jump to subroutine (JSR) instructions have no register operand. Refer to Table 2.

Read/Modify/Write Instructions—These instructions read a memory location or a register, modify or test its contents, and write the modified value back to memory or to the register. The test for negative or zero (TST) instruction is an exception to the read/modify/write instructions since it does not perform the write. Refer to Table 3.

Branch Instructions—The branch instructions cause a branch from the program when a certain condition is met. Refer to Table 4.

Bit Manipulation Instructions—These instructions are used on any bit in the first 256 bytes of the memory. One group either sets or clears. The other group performs the bit test and branch operations. Refer to Table 5.

Control Instructions—The control instructions control the MCU operations during program execution. Refer to Table 6.

Alphabetical Listing—The complete instruction set is given in alphabetical order in Table 7.

Opcode Map—Table 8 is an opcode map for the instructions used on the MCU.

Table 2. Register/Memory Instructions

		ADDRESSING MODES																	
		IMMEDIATE			DIRECT			EXTENDED			INDEXED (No Offset)			INDEXED (8-Bit Offset)			INDEXED 16-Bit Offset)		
Function	Mnemonic	OP Code	# Bytes	# Cycles	OP Code	# Bytes	# Cycles	OP Code	# Bytes	# Cycles	OP Code	# Bytes	# Cycles	OP Code	# Bytes	# Cycles	OP Code	# Bytes	# Cycles
LOAD A FROM MEMORY	LDA	A6	2	2	B6	2	4	C6	3	5	F6	1	4	E6	2	5	D6	3	6
LOAD X FROM MEMORY	LDX	AE	2	2	BE	2	4	CE	3	5	FE	1	4	EE	2	5	DE	3	6
STORE A IN MEMORY	STA	—	—	—	B7	2	5	C7	3	6	F7	1	5	E7	2	6	D7	3	7
STORE X IN MEMORY	STX	—	—	—	BF	2	5	CF	3	6	FF	1	5	EF	2	6	DF	3	7
ADD MEMORY TO A	ADD	AE	2	2	BB	2	4	CB	3	5	FB	1	4	EB	2	5	DB	3	6
ADD MEMORY AND CARRY TO A	ADC	A9	2	2	B9	2	4	C9	3	5	F9	1	4	E9	2	5	D9	3	6
SUBTRACT MEMORY	SUB	A0	2	2	B0	2	4	C0	3	5	F0	1	4	E0	2	5	D0	3	6
SUBTRACT MEMORY FROM A WITH BORROW	SBC	A2	2	2	B2	2	4	C2	3	5	F2	1	4	E2	2	5	D2	3	6
AND MEMORY TO A	AND	A4	2	2	B4	2	4	C4	3	5	F4	1	4	E4	2	5	D4	3	6
OR MEMORY WITH A	ORA	AA	2	2	BA	2	4	CA	3	5	FA	1	4	EA	2	5	DA	3	6
EXCLUSIVE OR MEMORY WITH A	EOR	A8	2	2	B8	2	4	C8	3	5	F8	1	4	E8	2	5	D8	3	6
ARITHMETIC COMPARE A WITH MEMORY	CMP	A1	2	2	B1	2	4	C1	3	5	F1	1	4	E1	2	5	D1	3	6
ARITHMETIC COMPARE X WITH MEMORY	CPX	A3	2	2	B3	2	4	C3	3	5	F3	1	4	E3	2	5	D3	3	6
BIT TEST MEMORY WITH A (Logical Compare)	BIT	A5	2	2	B5	2	4	C5	3	5	F5	1	4	E5	2	5	D5	3	6
JUMP UNCONDITIONAL	JMP	—	—	—	BC	2	3	CC	3	4	FC	1	3	EC	2	4	DC	3	5
JUMP TO SUBROUTINE	JSR	—	—	—	BD	2	7	CD	3	8	FD	1	7	ED	2	8	DD	3	9

Table 3. Read/Modify/Write Instructions

		ADDRESSING MODES														
		INHERENT (A)			INHERENT (X)			DIRECT			INDEXED (No Offset)			INDEXED (8-Bit Offset)		
Function	Mnemonic	OP Code	# Bytes	# Cycles	OP Code	# Bytes	# Cycles	OP Code	# Bytes	# Cycles	OP Code	# Bytes	OP Cycles	# Code	# Bytes	Cycles
INCREMENT	INC	4C	1	4	5C	1	4	3C	2	6	7C	1	6	6C	2	7
DECREMENT	DEC	4A	1	4	5A	1	4	3A	2	6	7A	1	6	6A	2	7
CLEAR	CLR	4F	1	4	5F	1	4	3F	2	6	7F	1	6	6F	2	7
COMPLEMENT	COM	43	1	4	53	1	4	33	2	6	73	1	6	63	2	7
NEGATE (2's COMPLEMENT)	NEG	40	1	4	50	1	4	30	2	6	70	1	6	60	2	7
ROTATE LEFT THRU CARRY	ROL	49	1	4	59	1	4	39	2	6	79	1	6	69	2	7
ROTATE RIGHT THRU CARRY	ROR	46	1	4	56	1	4	36	2	6	76	1	6	66	2	7
LOGICAL SHIFT LEFT	LSL	48	1	4	58	1	4	38	2	6	78	1	6	68	2	7
LOGICAL SHIFT RIGHT	LSR	44	1	4	54	1	4	34	2	6	74	1	6	64	2	7
ARITHMETIC SHIFT RIGHT	ASR	47	1	4	57	1	4	37	2	6	77	1	6	67	2	7
TEST FOR NEGATIVE OR ZERO	TST	4D	1	4	5D	1	4	3D	2	6	7D	1	6	6D	2	7

Table 4. Branch Instructions

		RELATIVE ADDRESSING MODE		
Function	Mnemonic	OP Code	# Bytes	# Cycles
BRANCH ALWAYS	BRA	20	2	4
BRANCH NEVER	BRN	21	2	4
BRANCH IFF HIGHER	BHI	22	2	4
BRANCH IFF LOWER OR SAME	BLS	23	2	4
BRANCH IFF CARRY CLEAR	BCC	24	2	4
(BRANCH IFF HIGHER OR SAME)	(BHS)	24	2	4
BRANCH IFF CARRY SET	BCS	25	2	4
(BRANCH IFF LOWER)	(BLO)	25	2	4
BRANCH IFF NOT EQUAL	BNE	26	2	4
BRANCH IFF EQUAL	BEQ	27	2	4
BRANCH IFF HALF CARRY CLEAR	BHCC	28	2	4
BRANCH IFF HALF CARRY SET	BHCS	29	2	4
BRANCH IFF PLUS	BPL	2A	2	4
BRANCH IFF MINUS	BMI	2B	2	4
BRANCH IFF INTERRUPT MASK BIT IS CLEAR	BMC	2C	2	4
BRANCH IFF INTERRUPT MASK BIT IS SET	BMS	2D	2	4
BRANCH IFF INTERRUPT LINE IS LOW	BIL	2E	2	4
BRANCH IFF INTERRUPT LINE IS HIGH	BIH	2F	2	4
BRANCH TO SUBROUTINE	BSR	AD	2	8

Table 5. Bit Manipulation Instructions

Function	Mnemonic	ADDRESSING MODES					
		OP Code	# Bytes	# Cycles	OP Code	# Bytes	# Cycles
BRANCH IFF BIT n IS SET	BRSET n(n = 0 . . . . 7)	—	—	—	2•n	3	10
BRANCH IFF BIT n IS CLEAR	BRCLR n(n = 0 . . . . 7)	—	—	—	01 + 2•n	3	10
SET BIT n	BSET n(n = 0 . . . . 7)	10 + 2•n	2	7	—	—	—
CLEAR BIT n	BCLR n(n = 0 . . . . 7)	11 + 2•n	2	7	—	—	—

Table 6. Control Instructions

Function	Mnemonic	INHERENT		
		OP Code	# Bytes	# Cycles
TRANSFER A TO X	TAX	97	1	2
TRANSFER X TO A	TXA	9F	1	2
SET CARRY BIT	SEC	99	1	2
CLEAR CARRY BIT	CLC	98	1	2
SET INTERRUPT MASK BIT	SEI	9B	1	2
CLEAR INTERRUPT MASK BIT	CLI	9A	1	2
SOFTWARE INTERRUPT	SWI	83	1	11
RETURN FROM SUBROUTINE	RTS	81	1	6
RETURN FROM INTERRUPT	RTI	80	1	9
RESET STACK POINTER	RSP	9C	1	2
NO OPERATION	NOP	9D	1	2

AMERICAN MICROSYSTEMS, INC.

PRELIMINARY DATA SHEET

S6809/S68A09/S68B09

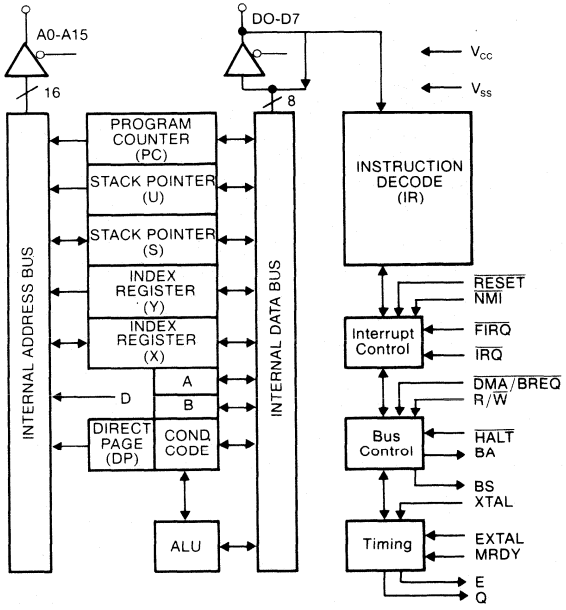
8-BIT MICROPROCESSING UNIT

Features

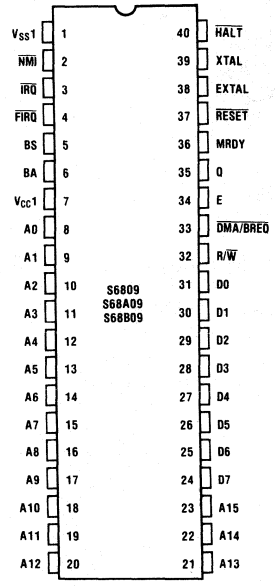
- ☐ **Interfaces with All S6800 Peripherals**
- ☐ **Upward Compatible Instruction Set and Addressing Modes**
- ☐ **Upward Source Compatible Instruction Set and Addressing Modes**
- ☐ **Two 8-Bit Accumulators Can Be Concatenated Into One 16-Bit Accumulator**
- ☐ **On-Chip Crystal Oscillator (4 Time XTAL)**

Because the S6809 generates *position-independent* code, software can be written in modular form for easy user expansion as system requirements increase. The S6809 is hardware compatible with all S6800 peripherals, and any assembly language code prepared for the S6800 can be passed through the S6809 assembler to produce code which will run on the S6809.

Block Diagram



Pin Configuration



S6809 Hardware Features

- ☐ **On-Chip Oscillator**
- ☐ **MRDY Input Extends Access Time**
- ☐ **$\overline{\text{DMA/BREQ}}$ for DMA and Memory Refresh**
- ☐ **Fast Interrupt Request Input: Stacks Only Program Counter and Condition Code**
- ☐ **Interrupt Acknowledge Output Allows Vectoring by Devices**
- ☐ **Three Vectored Priority Interrupt Levels**
- ☐ **SYNC Acknowledge Output Allows for Synchronization to External Event**
- ☐ **NMI Blocked after RESET until after First Load of Stack Pointer**
- ☐ **Early Address Valid Allows Use with Slow Memories**

S6809E Hardware Features

- ☐ **Last Instruction Cycle Output (LIC) for Identification Output Fetch**
- ☐ **Busy Output Eases Multiprocessor Design**

Instruction Set

- ☐ **Extended Range Branches**
- ☐ **Load Effective Address**
- ☐ **16-Bit Arithmetic**
- ☐ **8x8 Unsigned Multiply (Accumulator A*B)**
- ☐ **SYNC Instruction — Provides Software Sync with an External Hardware Process**
- ☐ **Push and Pull on 2 Stacks**
- ☐ **Push/Pull Any or All Registers**
- ☐ **Index Registers May Be Used as Stack Pointer**
- ☐ **Transfer/Exchange All Registers**

Addressing Modes

- ☐ **All 6800 Modes Plus PC Relative, Extended Indirect, Indexed Indirect, and PC Relative Indirect**
- ☐ **Direct Addressing Available Anywhere in Memory Map**
- ☐ **PC Relative Addressing: Byte Relative (± 32, 768 Bytes from PC)**
- ☐ **Complete Indexed Addressing Including Automatic Increment and Decrement, Register Offsets, and Four Indexable Registers (X, Y, U and S)**
- ☐ **Expanded Index Addressing**
  - **— 0, 5, 8, 16-Bit Constant Offset**
  - **— 8, 16-Bit Accumulator Offsets**

The S6809 gives the user 8 and 16-bit word capability with several hardware enhancements in the design such as the Fast Interrupt ($\overline{\text{FIRQ}}$), Memory Ready (MRDY), and Quadrature (Qout) and System Clock Outputs (Eout). With the Fast Interrupt Request ($\overline{\text{FIRQ}}$) the S6809 places *only* the Program Counter and Condition Code Register on the stack prior to accessing the $\overline{\text{FIRQ}}$ vector location. The Memory Ready ($\overline{\text{MRDY}}$) input allows extension of the data access time for use with slow memories. The System Clock (Eout) operates at the basic processor frequency and can be as the synchronization signal for the entire system. The Quadrature Output (Qout) provides additional system timing by signifying that address and data are stable.

The External Clock mode of the S6809E is particularly useful when synchronizing the processor to an externally generated signal. The Three-State Control input ($\overline{\text{TSC}}$) places the Address and R/$\overline{\text{W}}$ line in the high impedance state for DMA or Memory Refresh. The last Instruction Cycle (LIC) is activated during the last cycle of any instruction. This signifies that the next instruction cycle is the opcode fetch. The Processor Busy signal (BUSY) facilitates multiprocessor applications by allowing the designer to insure that flags being modified by one processor are not accessed by another simultaneously.

The S6809 features a family of addressing capabilities which can use any of the four index registers and stack pointers as a pointer to the operand (or the operand address). This pointer can have a fixed or variable signed offset that can be automatically incremented or decremented. The eight-bit direct page register permits a user to determine which page of memory is accessed by the instructions employing "page zero" addressing. This quick access to any page is especially useful in Multitasking Applications.

The S6809 has three vectored priority-interrupt levels, each of which automatically disables the lower priority interrupt while leaving the higher priority interrupt enabled.

The S6809 gives the system designer greater flexibility (through modular relocatable code) to enable the user to reduce system software costs while at the same time increasing software reliability and efficiency.

Absolute Maximum Ratings

Supply Voltage, V_{CC}	− 0.3V to + 7.0V
Input Voltage, V_{IN}	− 0.3V to + 7.0V
Operating Temperature Range, T_A	0°C to + 70°C
Storage Temperature Range, T_{stg}	− 55°C to + 150°C
Thermal Resistance, θ_{JA}	
Plastic	100°C/W
Ceramic	50°C/W

This device contains circuitry to protect the inputs against damage due to high static voltage or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Electrical Characteristics (V_{CC} = 5.0V ± 5%; V_{SS} = 0, T_A = 0°C to +70°C unless otherwise noted)

Symbol	Parameter		Min.	Typ.	Max.	Unit	Condition
V_{IH}	Input High Voltage	Logic, EXtal $\overline{RESET}$	V_{SS} + 2.0 V_{SS} + 4.0		V_{DD} V_{DD}	Vdc	
V_{IL}	Input Low Voltage	Logic EXtal, $\overline{RESET}$	V_{SS} – 0.3		V_{SS} + 0.8	Vdc	
I_{in}	Input Leakage Current	Logic		1.0	2.5	μAdc	V_{in} = 0 to 5.25V, V_{CC} = max
V_{OH}	Output High Voltage	D0-D7 A0-A15, R/$\overline{W}$, Q, E BA, BS	V_{SS} + 2.4 V_{SS} + 2.4 V_{SS} + 2.4			Vdc	I_{Load} = – 205μAdc, V_{CC} = min I_{Load} = – 145μAdc, V_{CC} = min I_{Load} = – 100μAdc, V_{CC} = min
V_{OL}	Output Low Voltage				V_{SS} + 0.5	Vdc	I_{Load} = 2.0mAdc, V_{CC} = min
P_D	Power Dissipation				1.0	W	
C_{in} C_{out}	Capacitance #	D_0-D_7 Logic Inputs, EXtal A_0-A_{15}, R/$\overline{W}$		10 7	15 10 12	pF	V_{in} = 0, T_A = 25°C, f = 1.0MHz
f f_{XTAL} f_{XTAL}	Frequency of Operation (Crystal or External Input)	S6809 S68A09 S68B09			4 6 8	MHz	
I_{TSI}	Three-State (Off State) Input Current	D_0-D_7 A_0-A_{15}, R/W		2.0	10 100	μAdc	V_{in} = 0.4 to 2.4V, V_{CC} = max

Read/Write Timing (Reference Figures 1 and 2)

		S6809			S68A09			S68B09				
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit	Condition
t_{CYC}	Cycle Time	1000			667			500			ns	
t_{UT}	Total Up Time	975			640			480			ns	$t_{acc} = t_{ut} - t_{AD} - t_{DSR}$
t_{ACC}	Peripheral Read Access Time	695			440			320			ns	$t_{ut} = t_{CYC} - t_{EF}$
t_{DSR}	Data Setup Time (Read)	80			60			40			ns	
t_{DHR}	Input Data Hold Time	10			10			10			ns	
t_{DHW}	Output Data Hold Time	30			30			30			ns	
t_{AH}	Address Hold Time (Address, R/$\overline{W}$)	30			30			30			ns	
t_{AD}	Address Delay			200			140			110	ns	
t_{DDW}	Data Delay Time (Write)			225			180			145	ns	
t_{AVS}	E_{low} to Q_{high} Time			250			165			125	ns	
t_{AQ}	Address Valid to Q_{high}	25			25			15			ns	
t_{PWEL}	Processor Clock Low	450			295			210			ns	
t_{PWEH}	Processor Clock High	450			280			220			ns	
t_{PCSR}	MRDY Set Up Time	60			60			60			ns	
t_{PCS}	Interrupts Set Up Time	200			140			110			ns	
t_{PCSH}	$\overline{HALT}$ Set Up Time	200			140			110			ns	
t_{PCSR}	$\overline{RESET}$ Set Up Time	200			140			110			ns	
t_{PCSD}	$\overline{DMA/BREQ}$ Set Up Time	125			125			125			ns	
t_{rc}	Crystal Osc Start Time	100			100			100			ms	
t_{ER}, t_{EF}	E Rise and Fall Time	5		25	5		25	5		20	ns	
t_{PCR}, t_{PLF}	Processor Control Rise/Fall			100			100			100	ns	
t_{QR}, t_{QF}	Q Rise and Fall Time	5		25	5		25	5		20	ns	
t_{PWQH}	Q Clock High	450			280			220			ns	

Figure 1. Read Data From Memory or Peripherals

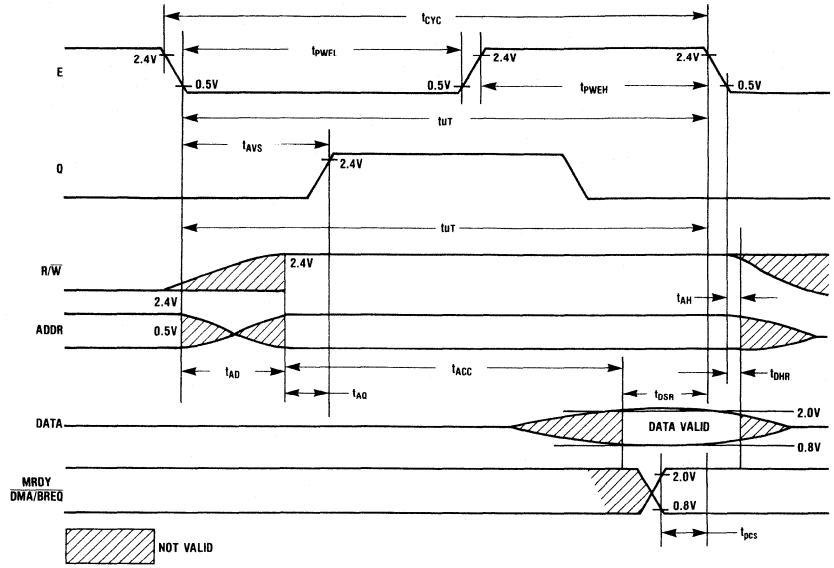


Figure 2. Write Data to Memory or Peripherals

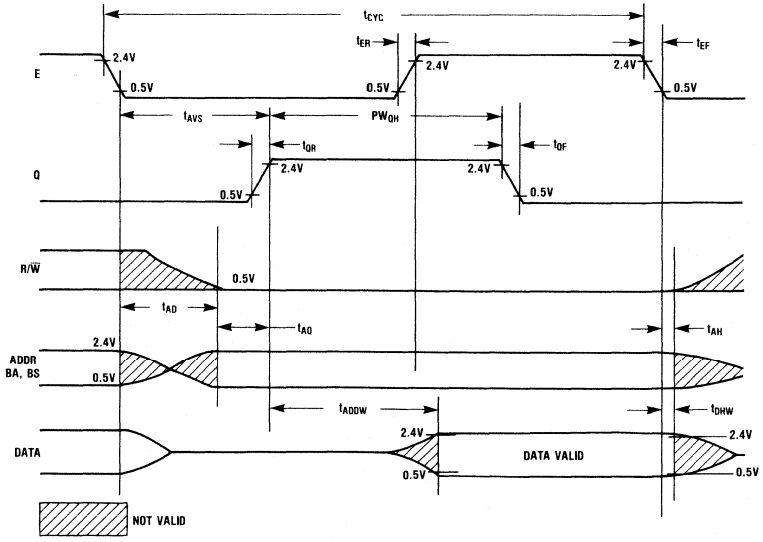
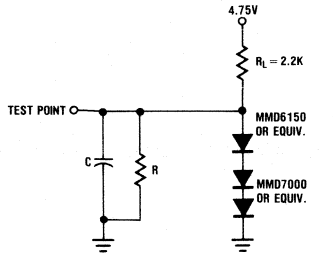


Figure 3. Bus Timing Test Load



C = 30pF FOR BA, BS
130pF FOR D0-D7, E, Q
90pF FOR A0-A15, R/W

R = 11.7kΩ FOR D0-D7
16.5kΩ FOR A0-A15, E, Q
24kΩ FOR BA, BS

Programming Model

As shown in Figure 4, the S6809 adds three registers to the set available in the S6800. The added registers include a direct page register, the User Stack pointer and a second Index Register.

Accumulators (A, B, D)

The A and B registers are general purpose accumulators which are used for arithmetic calculations and manipulation of data.

Certain instructions concatenate the A and B registers to form a single 16-bit accumulator. This is referred to as the D register, and is formed with the A register as the most significant byte.

Direct Page Register (DP)

The Direct Page Register of the S6809 serves to enhance the Direct Addressing Mode. The content of this register appears at the higher address outputs (A_8-A_{15}) during direct Addressing Instruction execution. This

S6800

Figure 4. Programming Model of the Microprocessing Unit

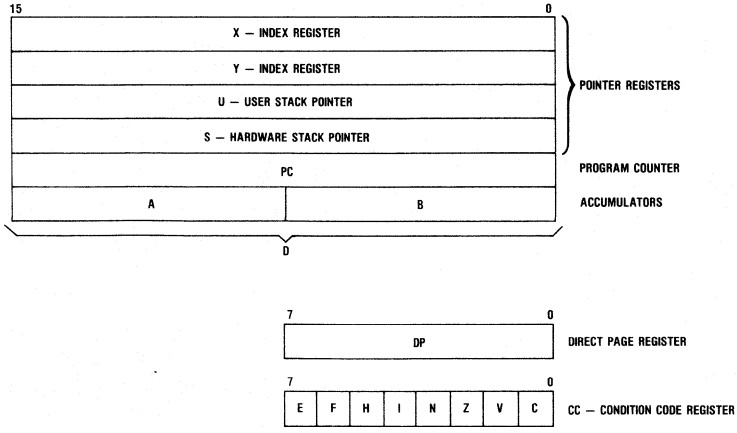
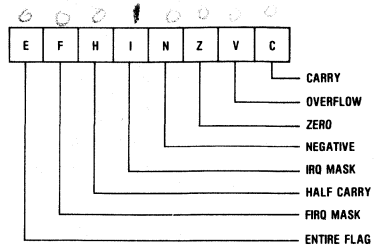


Figure 5. Condition Code Register Format



allows the direct mode to be used at any place in memory, under program control. To allow 6800 compatibility, all bits of this register are cleared during Processor Reset.

Index Registers (X, Y)

The Index Registers are used in indexed mode of addressing. The 16-bit address in this register takes part in the calculation of effective addresses. This address may be used to point to data directly or may be modified by an optional constant or register offset. During some indexed modes, the contents of the index register are incremented and decremented to point to the next item of tabular type data. All four pointer registers (X, Y, U, S) may be used as index registers.

Stack Pointers (U, S)

The Hardware Stack Pointer (S) is used automatically by the processor during subroutine calls and interrupts. The stack pointers of the S6809 point to the top of the stack, in contrast to the S6800 stack pointer which pointed to the next free location on the stack. The User Stack Pointer (U) is controlled exclusively by the programmer thus allowing arguments to be passed to and from subroutines with ease. Both Stack Pointers have the same indexed mode addressing capabilities as the X and Y registers, but also support **Push** and **Pull** instructions. This allows the S6809 to be used efficiently as a stack processor, greatly enhancing its ability to support higher level languages and modular programming.

Program Counter

The Program Counter is used by the processor to point to the address of the next instruction to be executed by the processor. Relative Addressing is provided allowing the Program Counter to be used like an index register in some situations.

Condition Code Register

The condition code register defines the State of the Processor at any given time, see Figure 5.

Bit 0 (C)

Bit 0 is the Carry Flag, and is usually the carry from the binary ALU. C is also used to represent a 'borrow' from subtract like instructions (CMP, NEG, SUB, SBC). Here the carry flag is the complement of the carry from the binary ALU.

Bit 1 (V)

Bit 1 is the overflow flag, and is set to a one by an operation which causes a signed two's complement arithmetic overflow. This overflow is detected in an operation in which the carry from the MSB in the ALU does not match the carry from the MSB-1.

Bit 2 (Z)

Bit 2 is the zero flag, and is set to a one if the result of the previous operation was identically zero.

Bit 3 (N)

Bit 3 is the negative flag, which contains exactly the value of the MSB of the result of the preceding operation. Thus, a negative two's-complement result will leave N set to a one.

Bit 4 (I)

Bit 4 is the $\overline{\text{IRQ}}$ mask bit. The processor will not recognize interrupts from the IRQ line if this bit is set to a one. $\overline{\text{NMI}}$, $\overline{\text{FIRQ}}$, $\overline{\text{IRQ}}$, $\overline{\text{RESET}}$, and SWI all set I to a one; SWI2 and SWI3 do not affect I.

Bit 5 (H)

Bit 5 is the half-carry bit, and is used to indicate a carry from bit 3 in the ALU as a result of an 8-bit addition only (ADC or ADD). This bit is used by the DAA instruction to perform a BCD decimal add adjust operation. The state of this flag is undefined in all subtract-like instructions.

Bit 6 (F)

Bit 6 is the $\overline{\text{FIRQ}}$ mask bit. The processor will not recognize interrupts from the FIRQ line if this bit is a one. $\overline{\text{NMI}}$, $\overline{\text{FIRQ}}$, SWI, and $\overline{\text{RESET}}$ all set F to a one. $\overline{\text{IRQ}}$, SWI2 and SWI3 do not affect F.

Bit 7 (E)

Bit 7 is the entire flag, and when set to a one indicates that the complete machine state (all the registers) was stacked, as opposed to the subset state (PC and CC). The E bit of the *stacked* CC is used on a return from interrupt (RTI) to determine the extent of the unstacking. Therefore, the current E left in the Condition Code Register represents past action.

S6809 MPU Signal Description

Power (V_{SS}, V_{CC})

Two pins are used to supply power to the part: V_{SS} is ground or 0 volts, while V_{CC} is $+5.0V \pm 5\%$.

Address Bus (A_0-A_{15})

Sixteen pins are used to output address information from the MPU onto the Address Bus. When the processor does not require the bus for a data transfer, it will output address $FFFF_{16}$, $R/\overline{W} = 1$, and $BS = 0$. Addresses are valid on the rising edge of Q (see Figures 1 and 2). All address bus drivers are made high-impedance when output Bus Available (BA) is high. Each pin will drive one Schottky TTL load and typically 90pF.

Data Bus (D_0-D_7)

These eight pins provide communication with the system bi-directional data bus. Each pin will drive one Schottky TTL load and typically 130pF.

Read/Write ($R/\overline{W}$)

This signal indicates the direction of the data transfer on the data bus. A low indicates that the MPU is writing data onto the data bus. $R/\overline{W}$ is made high impedance when BA is high. $R/\overline{W}$ is valid on the rising edge of Q, refer to Figures 1 and 2.

$\overline{\text{RESET}}$

A low level on this Schmitt-trigger input for greater than one bus cycle will reset the MPU as shown in Figure 6. The Reset vectors are fetched from locations $FFFE_{16}$ and $FFFF_{16}$ (Table 1) when Interrupt Acknowledge is true, ($BA \wedge BS = 1$). During initial power-on, the Reset line should be held low until the clock oscillator is fully operational; see Figure 7.

Because the S6809 Reset pin has a Schmitt-trigger input with a threshold voltage higher than that of standard peripherals, a simple R/C network may be used to reset the entire system. This higher threshold voltage insures that all peripherals are out of the reset state before the Processor.

$\overline{\text{HALT}}$

A low level on this input pin will cause the MPU to stop running at the end of the present instruction and remain halted indefinitely without loss of data. When Halted, the BA output is driven high indicating the buses are high-impedance. BS is also high which indicates the processor is in the Halt or Bus Grant state. While halted, the MPU will not respond to external real-time requests ($\overline{\text{FIRQ}}$, $\overline{\text{IRQ}}$) although $\overline{\text{DMA/BREQ}}$ will always be accepted, and $\overline{\text{NMI}}$ or $\overline{\text{RESET}}$ will be latched for later response. During the Halt state Q and E continue to run normally. If the MPU is not running ($\overline{\text{RESET}}$, $\overline{\text{DMA/BREQ}}$), a halted state (BA and BS = 1) can be achieved by pulling $\overline{\text{HALT}}$ low while $\overline{\text{RESET}}$ is still low. If $\overline{\text{DMA/BREQ}}$ and $\overline{\text{HALT}}$ are both pulled low, the processor will reach the last cycle of the instruction (by reverse cycle stealing) where the machine will then become halted. See Figure 8.

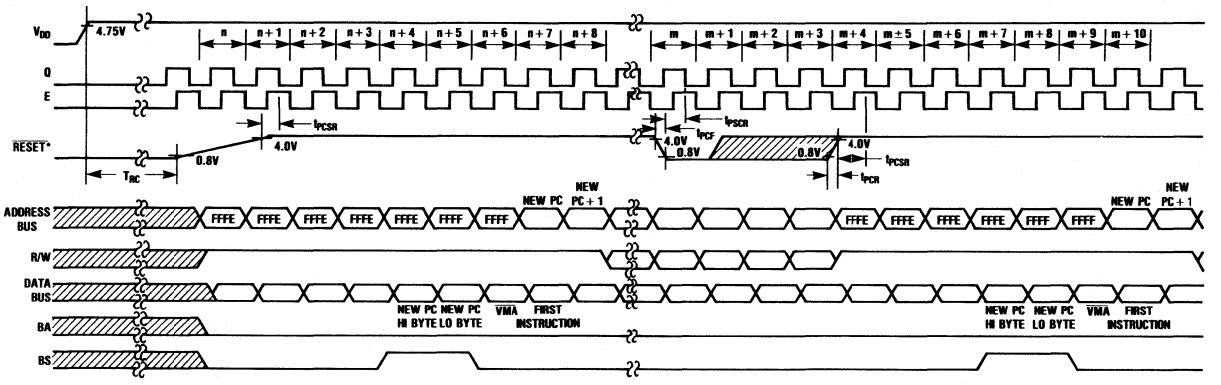
Bus Available, Bus Status (BA, BS)

The Bus Available output is an indication of an internal control signal which makes the MOS buses of the MPU high-impedance. This signal does not imply that the bus will be available for more than one cycle. When BA goes low, an additional dead cycle will elapse before the MPU acquires the bus.

The Bus Status output signal, when decoded with BA, represents the MPU state (valid with leading edge of Q):

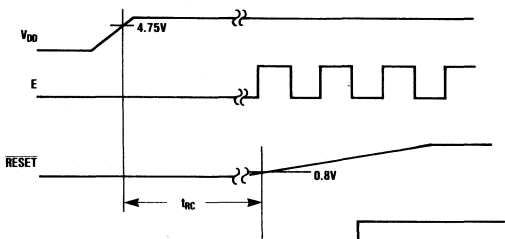
MPU State		
BA	BS	
0	0	Normal (Running)
0	1	Interrupt Acknowledge
1	0	SYNC Acknowledge
1	1	HALT or Bus Grant

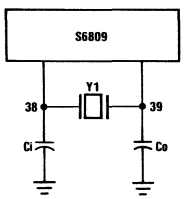
Figure 6. $\overline{\text{RESET}}$ Timing



*NOTE: PARTS WITH DATE CODES PREFIXED BY 7F WILL COME OUT OF RESET ONE CYCLE SOONER THAN SHOWN

Figure 7. Crystal Connections and Oscillator Start Up





Y1	C_{in}	C_{out}
8MHz	18pF	18pF
6MHz	20pF	20pF
4MHz	24pF	24pF

6809 Crystal Parameters*

	3.58MHz	4.00MHz	6.0MHz	8.0MHz
RS	60Ω	50Ω	30-50Ω	20-40Ω
C_0	3.5pF	6.5pF	4-6pF	4-6pF
C_1	.015pF	.025pF	.01-.02pF	.01-.02pF
C_{in}-C_{out}	25pF	25pF	25pF	25pF
Q	40K	≅ 30K	≅ 20K	≅ 20K

All Parameters Are ± 10%.
*Note: These are representative AT-cut crystal parameters only. Crystals of other types of cut that work may also be used.

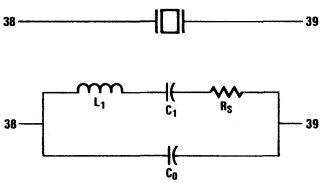
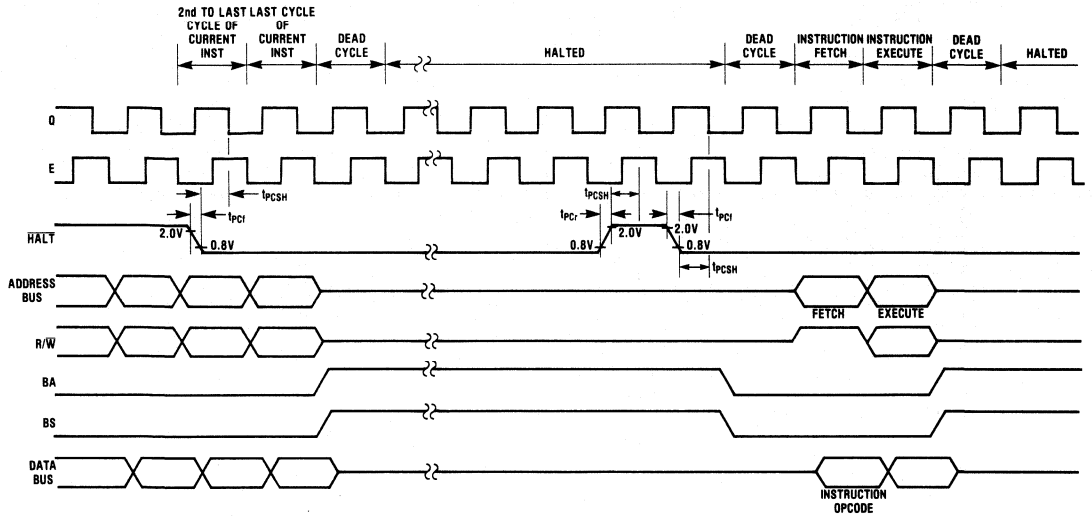


Figure 8. $\overline{\text{HALT}}$ and Single Instruction Execution for System Debug



Interrupt Acknowledge is indicated during both cycles of a hardware-vector-fetch ($\overline{\text{RESET}}$, $\overline{\text{NMI}}$, $\overline{\text{FIRQ}}$, $\overline{\text{IRQ}}$, SWI, SWI2, SWI3). This signal, plus decoding of the lower 4 address lines can provide the user with an indication of which interrupt level is being serviced and allow vectoring by device (see Table 1).

Sync Acknowledge is indicated while the MPU is waiting for external synchronization on an interrupt line.

Halt/Bus Grant is true when the S6809 is in a Halt or Bus Grant condition.

Table 1. Memory Map for Interrupt Vectors

Memory Map for Vector Location		Interrupt Vector Description
MS	LS	
FFFE	FFFF	$\overline{\text{RESET}}$
FFFC	FFFD	$\overline{\text{NMI}}$
FFFA	FFFB	SWI
FFF8	FFF9	$\overline{\text{IRQ}}$
FFF6	FFF7	$\overline{\text{FIRQ}}$
FFF4	FFF5	SWI2
FFF2	FFF3	SWI3
FFF0	FFF1	Reserved

***NOTE:** $\overline{\text{NMI}}$, $\overline{\text{FIRQ}}$ and $\overline{\text{IRQ}}$ requests are latched by the falling edge of every Q except during cycle stealing operations (e.g., DMA) where only $\overline{\text{NMI}}$ is latched. From this point, a delay of at least one bus cycle will occur before the interrupt is serviced by the MPU.

Non-Maskable Interrupt ($\overline{\text{NMI}}$)

A negative edge on this input requests that a non-maskable interrupt sequence be generated. A non-maskable interrupt cannot be inhibited by the program, and also has a higher priority than $\overline{\text{FIRQ}}$, $\overline{\text{IRQ}}$ or software interrupts. During recognition of an $\overline{\text{NMI}}$, the entire machine state is saved on the hardware stack. After reset, an $\overline{\text{NMI}}$ will not be recognized until the first program load of the Hardware Stack Pointer (S). The pulse width of $\overline{\text{NMI}}$ low must be at least one E cycle. If the $\overline{\text{NMI}}$ input does not meet the minimum set up with respect to Q, the interrupt will not be recognized until the next cycle. See Figure 9.

Fast-Interrupt Request ($\overline{\text{FIRQ}}$)

A low level on this input pin will initiate a fast interrupt sequence, provided its mask bit (F) in the CC is clear. This sequence has priority over the standard Interrupt Request ($\overline{\text{IRQ}}$), and is fast in the sense that it stacks only the contents of the condition code register and the program counter. The interrupt service routine should clear the source of the interrupt before doing an RTI. See Figure 10.

Figure 9. $\overline{IRQ}$ and $\overline{NMI}$ Interrupt Timing

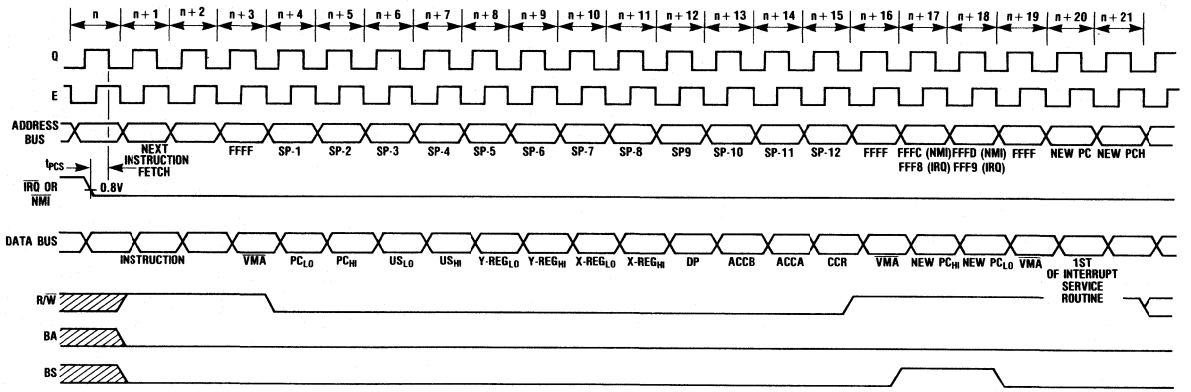
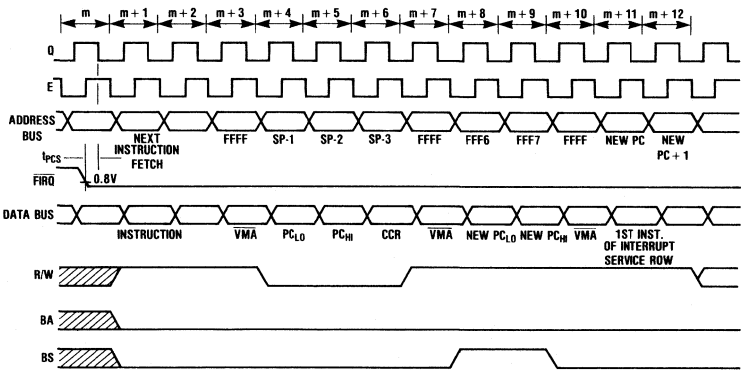


Figure 10. $\overline{FIRQ}$ Interrupt Timing



Interrupt Request ($\overline{IRQ}$)

A low level input on this pin will initiate an Interrupt Request sequence provided the mask bit (I) in the CC is clear. Since $\overline{IRQ}$ stacks the entire machine state it provides a slower response to interrupts than $\overline{FIRQ}$. $\overline{IRQ}$ also has a lower priority than $\overline{FIRQ}$. Again, the interrupt service routine should clear the source of the interrupt before doing an RTI. See Figure 9.

XTAL, EXTAL

These input pins are used to connect the on-chip oscillator to an external parallel-resonant crystal. Alternately, the pin EXTAL may be used as a TTL level input for external timing by grounding XTAL. The crystal or external frequency is 4 times the bus frequency, see Figure 7. Proper RF layout techniques should be observed in the layout of printed circuit boards.

E, Q

E is similar to the S6800 bus timing signal $\phi 2$; Q is a quadrature clock signal which leads E. Q has no parallel on the S6800. Addresses from the MPU will be valid with the leading edge of Q. Data is latched on the falling edge of E. Timing for E and Q is shown in Figure 11.

MRDY

This input control signal allows stretching of E to extend data-access time. When MRDY is high, E will be in normal operation. When MRDY is low, E may be stretched integral multiples of quarter (¼) bus cycles, thus allowing interface to slow memories as shown in Figure 12. A maximum stretch is 10 microseconds. During non-valid memory accesses ($\overline{VMA}$ cycles). MRDY has no effect on stretching E. This inhibits slowing the processor speed during "don't care" bus accesses.

$\overline{DMA/BREQ}$

The $\overline{DMA/BREQ}$ input provides a method of suspending execution and acquiring the MPU bus for another use as shown in Figure 13. Typical uses include DMA and dynamic memory refresh.

Transition of $\overline{DMA/BREQ}$ should occur during Q. A low level on this pin will stop instruction execution at the end of the current cycle. The MPU will acknowledge $\overline{DMA/BREQ}$ by setting BA and BS to a one. The requesting device will now have up to 15 bus cycles before the MPU retrieves the bus for self-refresh. Self-refresh requires one bus cycle with a leading and trailing dead cycle, see Figure 14.

Typically, the DMA controller will request to use the bus by asserting the $\overline{DMA/BREQ}$ pin low on the leading edge of E. When the MPU replies with BA = BS = 1, that cycle will be a dead cycle used to transfer control to the DMA controller.

False memory accesses should be prevented during any dead cycles. When BA is cleared (either as a result of

Figure 11. E/Q Relationship

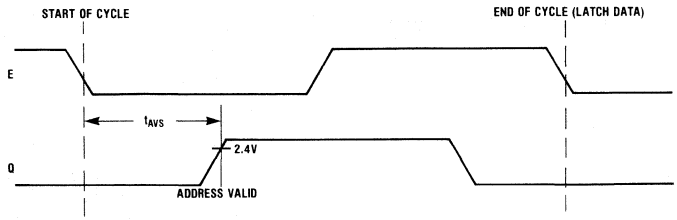


Figure 12. MRDY Timing

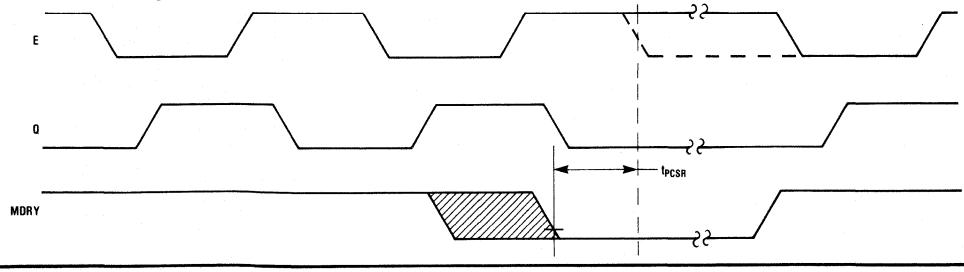


Figure 13. Typical DMA Timing (<14 Cycles)

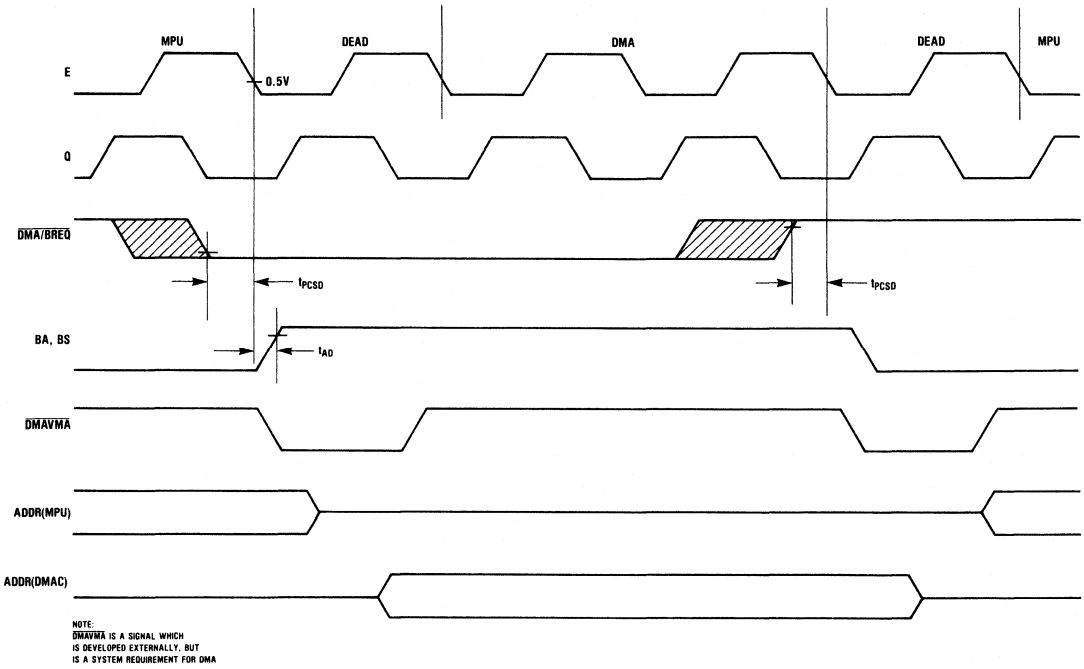
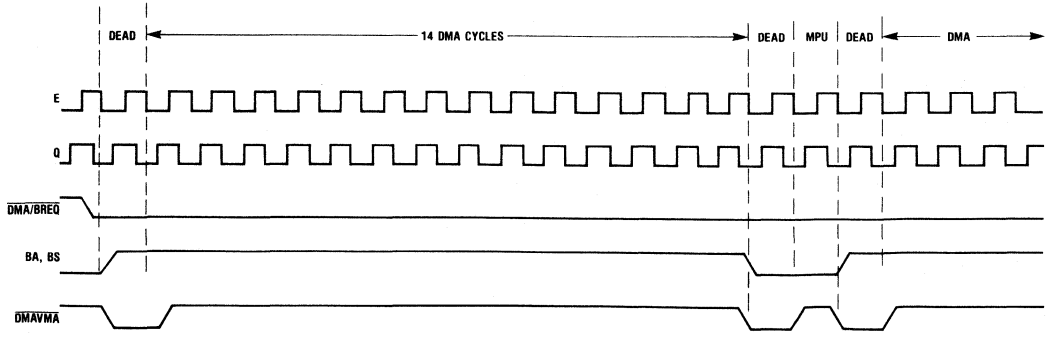


Figure 14. Auto-Refresh DMA Timing (<14 Cycles)



$\overline{DMA/BREQ}$ = HIGH or MPU self-refresh), the DMA device should be taken off the bus.

Another dead cycle will elapse before the MPU is allowed a memory access to transfer control without contention.

MPU Operation

During normal operation, the MPU fetches an instruction from memory and then executes the requested function. This sequence begins at $\overline{RESET}$ and is repeated indefinitely unless altered by a special instruction or hardware occurrence. Software instructions that alter normal MPU operation are: SWI, SWI2, SWI3, CWAI, RTI and SYNC. An interrupt, $\overline{HALT}$ or $\overline{DMA}$/$\overline{BREQ}$ can also alter the normal execution of instructions. Figure 15 illustrates the flowchart for the S6809. The left-half of the flowchart represents normal operation; the right-half represents the flow when an interrupt when an interrupt or special instruction occurs.

Addressing Modes

The basic instructions of any computer are greatly enhanced by the presence of powerful addressing modes. The S6809 has the most complete set of addressing modes available on any microcomputer today. For example, the S6809 has 59 basic instructions, however it recognizes 1464 different variations of instructions and addressing modes. The new addressing modes support modern programming techniques. The following addressing modes are available on the S6809:

- Inherent (Includes Accumulator)
- Immediate
- Extended
  - Extended Indirect
- Direct
- Register
- Indexed
  - Zero-Offset
  - Constant Offset
  - Accumulator Offset
  - Auto Increment/Decrement
  - Indexed Indirect
- Relative
  - Short/Long Relative Branching
  - Program Counter Relative Addressing

Inherent (Includes Accumulator)

In this addressing mode, the opcode of the instruction contains all the address information necessary. Examples of Inherent Addressing are: ABX, DAA, SWI, ASRA, and CLRB.

Immediate Addressing

In Immediate Addressing, the effective addressing of the data is the location immediately following the opcode; the data to be used in the instruction immediately follows the opcode of the instruction. The S6809 uses both 8 and 16-bit immediate values depending on the size of argument specified by the opcode. Examples of instructions with Immediate Addressing are:

```
LDA #$20
LDX #$F000
LDY #CAT
```

Note: # signifies Immediate addressing, $ signifies hexadecimal value.

Extended Addressing

In Extended Addressing the contents of the two bytes immediately following the opcode fully specify the 16-bit effective address used by the instruction. Note that the address generated by an extended instruction defines an absolute address and is not position independent. Examples of Extended Addressing include:

```
LDA CAT
STX MOUSE
LDD $2000
```

Extended Indirect

As a special case of indexed addressing (discussed below), one level of indirection may be added to Extended Addressing. In Extended Indirect, the two bytes following the postbyte of an Indexed instruction contains the address of the address of the data.

```
LDA [CAT]
LDX [$FFFE]
STU [DOG]
```

Direct Addressing

Direct addressing is similar to extended addressing except that only one byte of address follows the opcode. This byte specifies the lower 8 bits of the address to be used. The upper 8 bits of the address are supplied by the direct page register. Since only one byte of address is required in direct addressing, this mode requires less memory and executes faster than extended addressing. Of course, only 256 locations (one page) can be accessed without redefining the contents of the DP register. Since the DP register is set to $00 on Reset, direct addressing on the S6809 is compatible with direct addressing on the S6800. Indirection is not allowed in direct addressing. Some examples of direct addressing are:

```
LDA     $30
SETDP   $10 (Assembler directive)
LDB     $1030
LDD     <CAT
```

Note: < is an assembler directive which forces direct addressing.

Register Addressing

Some opcodes are followed by a byte that defines a register or set of registers to be used by the instruction, this is called a POSTBYTE. Some examples of register addressing are:

TFR	X,Y	Transfers X into Y
EXG	A,B	Exchanges A with B
PSHS	A,B,X,Y	Push onto S Y,X,B, then A
PULU	X,Y,D	Pull from U D,X, then Y

Indexed Addressing

In all indexed addressing one of the pointer registers (X, Y, U, S, and sometimes PC) is used in a calculation of the effective address of the operand to be used by the instruction. Five basic types of indexing are available and are discussed below. The postbyte of an indexed instruction specifies the basic type and variation of the addressing mode as well as the pointer register to be used. Figure 16 lists the legal formats for the postbyte. Table 2 gives the assembler form and the number of cycles and bytes added to the basic values for indexed addressing for each variation.

Zero-Offset Indexed — In this mode, the selected pointer register contains the effective address of the data to be used by the instruction. This is the fastest indexing mode.

Examples are:

LDD 0,X
LDA 0,S

Constant Offset Indexed — In this mode a two's-complement offset and the contents of one of the pointer registers are added to form the effective address of the operand. The pointer register's initial content is unchanged by the addition.

Three sizes of offsets are available:

± 4-bit (– 16 to + 15)
± 7-bit (– 128 to + 127)
± 15-bit (– 32768 to + 32767)

The two's complement 5-bit offset is included in the postbyte and therefore is most efficient in use of bytes and cycles. The two's complement 8-bit offset is contained in a single byte following the postbyte. The two's complement 16-bit offset is in the two bytes following the postbyte. In most cases the programmer need not be concerned with the size of this offset since the assembler will select the optional size automatically.

Examples of constant-offset indexing are:

LDA 23,X
LDX -2,S
LDY 300,X
LDU CAT,Y

Figure 16. Indexed Addressing Postbyte Register Bit Assignments

POST—BYTE REGISTER BIT								INDEXED ADDRESSING MODE
7	6	5	4	3	2	1	0	
0	R	R	X	X	X	X	X	EA = ,R ± 4-BIT OFFSET
1	R	R	0	0	0	0	0	,R+
1	R	R	I	0	0	0	1	,R+ +
1	R	R	0	0	0	1	0	,–R
1	R	R	I	0	0	1	1	,– –R
1	R	R	I	0	1	0	0	EA = ,R ± 0 OFFSET
1	R	R	I	0	1	0	1	EA = ,R ± ACCB OFFSET
1	R	R	I	0	1	1	0	EA = ,R ± ACCA OFFSET
1	R	R	I	1	0	0	0	EA = ,R ± 7-BIT OFFSET
1	R	R	I	1	0	0	1	EA = ,R ± 15-BIT OFFSET
1	R	R	I	1	0	1	1	EA = ,R ± D OFFSET
1	X	X	I	1	1	0	0	EA = ,PC ± 7-BIT OFFSET
1	X	X	I	1	1	0	1	EA = ,PC ± 15-BIT OFFSET
1	R	R	1	1	1	1	1	EA = ,ADDRESS

ADDRESSING MODE FIELD
INDIRECT FIELD
SIGN BIT WHEN B7 = 0
REGISTER FIELD
00:R = X
01:R = Y
10:R = U
11:R = S
X = DON'T CARE

Accumulator-Offset Indexed — This mode is similar to constant offset indexed except that the two's complement value in one of the accumulators (A, B or D) and the content of one of the pointer registers are added to form the effective address of the operand. The contents of both the accumulator and the pointer register are unchanged by the addition. The postbyte specifies which accumulator to use as an offset and no additional bytes are required. The advantage of an accumulator offset is that the value of the offset can be calculated by a program at run-time.

Some examples are:

LDA B,Y
LDX D,Y
LEAX B,X

Auto Increment/Decrement Indexed — In the auto increment addressing mode, the pointer register contains the address of the operand. Then, after the pointer register is used it is incremented by one or two. This addressing mode is useful in stepping through tables, moving data, or for the creation of software stacks. In auto

Table 2. Indexed Addressing Modes

Type	Forms	Non Indirect				Indirect			
		Assembler Form	Postbyte OP Code	+ ~	+ #	Assembler Form	Postbyte OP Code	+ ~	+ #
Constant Offset From R (Signed Offsets)	No Offset	,R	1RR00100	0	0	[,R]	1RR10100	3	0
	5-Bit Offset	n, R	0RRnnnnn	1	0	defaults to 8-bit			
	8-Bit Offset	n, R	1RR01000	1	1	[n, R]	1RR11000	4	1
	16-Bit Offset	n, R	1RR01001	4	2	[n, R]	1RR11001	7	2
Accumulator Offset From R (Signed Offsets)	A — Register Offset	A, R	1RR00110	1	0	[A, R]	1RR10110	4	0
	B — Register Offset	B, R	1RR00101	1	0	[B, R]	1RR10101	4	0
	D — Register Offset	D, R	1RR01011	4	0	D, R]	1RR11011	7	0
Auto Increment/Decrement R	Increment By 1	,R+	1RR00000	2	0	not allowed			
	Increment By 2	,R++	1RR00001	3	0	[,R++]	1RR10001	6	0
	Decrement By 1	,−R	1RR00010	2	0	not allowed			
	Decrement By 2	,−−R	1RR00011	3	0	[,−−R]	1RR10011	6	0
Constant Offset From PC	8-Bit Offset	n, PCR	1XX01100	1	1	[n, PCR]	1XX11100	4	1
	16-Bit Offset	n, PCR	1XX01101	5	2	[n, PCR]	1XX11101	8	2
Extended Indirect	16-Bit Address	—	—	—	—	[n]	10011111	5	2

$^{+}_{\sim}$ and $^{+}_{\#}$ indicate the number of additional cycles and bytes for the particular variation.

R = X, Y, U or S X = 00 Y = 01
X = Don't Care U = 10 S = 11

decrement, the pointer register is decremented prior to use as the address of the data. The use of auto decrement is similar to that of auto increment but the tables, etc. are scanned from the high to low addresses. The size of the increment/decrement can be either one or two to allow for tables of either 8 or 16-bit data to be accessed and is selectable by the programmer. The predecrement, post-increment nature of these modes allow them to be used to create additional software stacks that behave identically to the U and S stacks.

Some examples of the auto increment/decrement addressing modes are:

```
LDA ,X+
STD ,Y++
LDBL ,-Y
LDX ,--S
```

Indexed Indirect

All of the indexing modes with the exception of auto increment/decrement by one, or a ± 4-bit offset may have an additional level of indirection specified. In Indirect addressing, the effective address is contained at the location specified by the content of the Index register plus any offset. In the example below, the A accumulator is loaded indirectly using an effective address calculated from the Index register and an offset.

```
                        Before Execution
                    A = XX (don't care)
                        X = $F000
$0100  LDA    [10,X]  EA is now $F010
$F010  $F1            F150 is now the new EA
$F011  $5Q
$F150  $AA
                        After Execution
                    A = $AA Actual Data Loaded
```

All modes of indexed indirect are included except those which are meaningless (e.g., auto increment/decrement by 1 indirect). Some examples of indexed indirect are:

```
LDA  [,X]
LDD  [10,S]
LDA  [B,Y]
LDD  [,X++]
```

Relative Addressing

The byte(s) following the branch opcode is (are) treated as a signed offset which is added to the program counter. If the branch condition is true then the calculated address (PC + signed offset) is loaded into the program counter. Program execution continues at the new location as indicated by the PC; Short (1 byte offset) and long (2 bytes offset) relative addressing modes are available. All of memory can be reached in long relative addressing as an effective address is interpreted modulo 2^{16}. Some examples of relative addressing are:

```
        BEQ   CAT      (short)
        BGT   DOG      (short
CAT     LBEQ  RAT      (long)
DOG     LBGT  RABBIT   (long)
        .
        .
        .
RAT     NOP
RABBIT  NOP
```

Program Counter Relative

The PC can be used as the pointer register with 8 or 16-bit signed offsets. As in relative addressing the offset is added to the current PC to create the effective address. The effective address is then used as the address of the operand or data. Program Counter Relative Addressing is used for writing position independent programs. Tables related to a particular routine will maintain the same relationship after the routine is moved, if referenced relative to the Program Counter. Examples are:

```
LDA     CAT,PCR
LEAX    TABLE, PCR
```

Since program counter relative is a type of indexing, an additional level of indirection is available.

```
LDA     [CAT,PCR]
LDU     (DOG,PCR]
```

S6809 Instruction Set

The instruction set of the S6809 is similar to that of the S6800 and is upward compatible at the source code level. The number of opcodes has been reduced from 72 to 59, but because of the expanded architecture and additional addressing modes, the number of available opcodes (with different addressing modes) has risen from 197 to 1464.

Some of the new instructions and addressing modes are described in detail below:

PSHU/PSHS

The push instructions have the capability of pushing onto either the hardware stack (S) or user stack (U) any or all of the MPU registers with a single instruction.

PULU/PULS

The pull instructions have the same capability of the push instruction, in reverse order. The byte immediately following the push or pull opcode determines which register or registers are to be pushed or pulled. The actual PUSH/PULL sequence is fixed; each bit defines a unique register to push or pull as shown in Figure 17.

TFR/EXG

Within the S6809, any register may be transferred to or exchanged with another of like-size, i.e., 8-bit to 8-bit or 16-bit to 16-bit. Bits 4-7 of postbyte define the source register, while bits 0-3 represent the destination register. These are denoted as follows:

```
0000 – D     0101 – PC
0001 – X     1000 – A
0010 – Y     1001 – B
0011 – U     1010 – CC
0100 – S     1011 – DP
```

Note: All other combinations are undefined and INVALID.

Load Effective Address

The LEA works by calculating the effective address used in an indexed instruction and stores that address value, rather than the data at that address, in a pointer register. This makes all the features of the internal addressing hardware available to the programmer. Some of the implications of this instruction are illustrated in the following table of examples:

The LEA Instruction also allows the user to access data in a position independent manner. For example:

```
        LEAX  MSG1, PCR
        LBSR  PDATA (Print message routine)

MSG1 FCC  'MESSAGE'
```

Figure 17. Push/Pull Postbyte

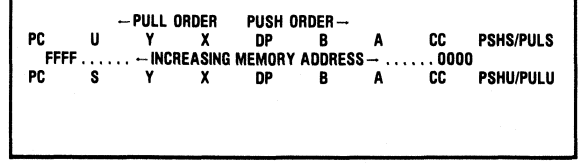


Table 3. LEA Examples

Instruction	Operation	Comment
LEAX 10, X	X+10 →X	Adds 5-bit constant 10 to X
LEAX 500, X	X+500 →X	Adds 6-bit constant 500 to X
LEAY A, Y	Y+A →Y	Adds 8-bit accumulator to Y
LEAY D, Y	Y+D →Y	Adds 16-bit D accumulator to Y
LEAU −10, U	U−10 →U	Subtracts 10 from U
LEAS −10, S	S−10 →S	Used to reserve area on stack
LEAS 10, S	S+10 →S	Used to 'clean up' stack
LEAX 5, S	S+5 →X	Transfers as well as adds

This sample program prints "message." By writing MSG1,PCR, the assembler computes the distance between the present address and MSG1. This result is placed as a constant into the LEAX instruction which will be indexed from the PC value at the time of execution. No matter where the code is located, when it is executed, the computed offset from the PC will put the absolute address of MSG1 into the X pointer register. This code is totally position independent.

MUL

Multiplies the unsigned binary numbers in the A and B accumulator and places the unsigned result into the 16-bit D accumulator. This unsigned multiply also allows multiple-precision multiplications.

Long and Short Relative Branches

The S6809 has the capability of program counter relative branching throughout the entire memory map. In this mode, if the branch is to be taken, the 8 or 16-bit signed offset is added to the value of the program counter to be used as the effective address. This allows the program to branch anywhere in the 64K memory map. Position independent code can be easily generated through the use of relative branching. Both short (8-bit) and long (16-bit) branches are available.

Sync

After encountering a Sync operation, the MPU enters a Sync state, stops processing instructions and waits for an interrupt. If the pending interrupt is non-maskable ($\overline{NMI}$) or maskable ($\overline{FIRQ}$, $\overline{IRQ}$) with its mask bit (F or I) clear, the processor will clear the Sync state and perform the normal interrupt stacking and service routine. Since $\overline{FIRQ}$ and $\overline{IRQ}$ are not edge-triggered, a low level with a minimum duration of three cycles is required to assure that the interrupt will be taken. If the pending interrupt is maskable ($\overline{FIRQ}$, $\overline{IRQ}$) with its mask bit (F or I) set, the processor will clear the Sync state and continue processing in sequence. Figure 18 depicts Sync timing.

Software Interrupts

A Software Interrupt is an instruction which will cause an interrupt, and its associated vector fetch. These Software Interrupts are useful in operating system calls, software debugging, trace operations, memory mapping, and software development systems. Three levels of SWI are available on this S6809, and are prioritized in the following order: SWI, SWI2, SWI3.

16-Bit Operations

The S6809 has the capability of processing 16-bit data. These instructions include loads, stores, compares, adds, subtracts, transfers, exchanges, pushes and pulls.

Cycle-by-Cycle Operation

The address bus cycle-by-cycle performance chart illustrates the memory-access sequence corresponding to each possible instruction and addressing mode in the S6809. Each instruction begins with an opcode fetch. While that opcode is being internally decoded, the next program byte is always fetched. (Most instructions will use the next byte, so this technique considerably speeds throughput). Next, the operation of each opcode will follow the flowchart. $\overline{VMA}$ is an indication of $FFFF_{16}$ on the address bus, R/$\overline{W}$ = 1 and BS = 0. The following examples illustrate the use of the chart; see Figure 19.

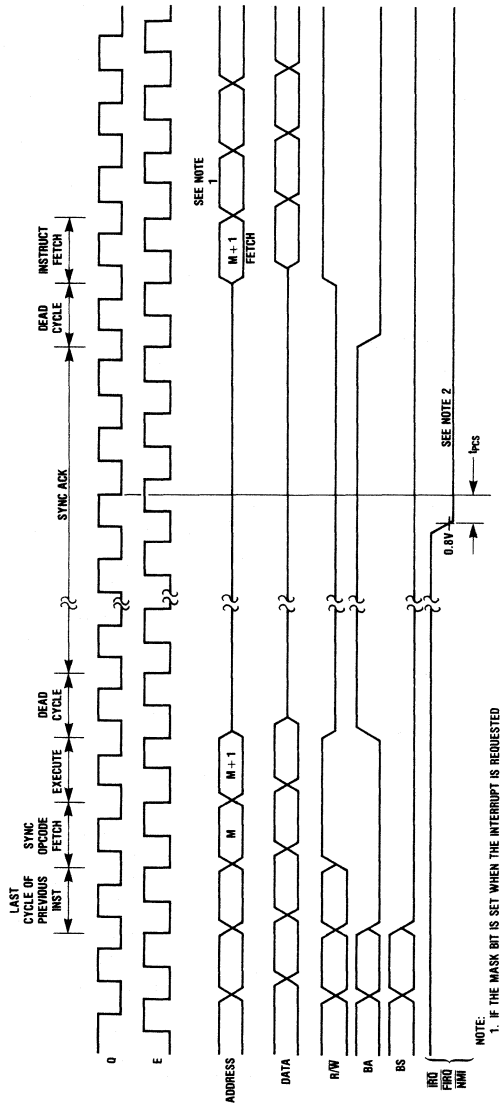
LBSR (Branch taken)

Cycle #	
1	opcode Fetch
2	opcode +
3	opcode +
4	$\overline{VMA}$
5	$\overline{VMA}$
6	ADDR
7	$\overline{VMA}$
8	STACK (write)
9	STACK (write)

DEC (Extended)

1	opcode Fetch
2	opcode +
3	opcode +
4	$\overline{VMA}$
5	ADDR (read)
6	$\overline{VMA}$
7	ADDR (write)

Figure 18. SYNC Timing



NOTE:
1. IF THE MASK BIT IS SET WHEN THE INTERRUPT IS REQUESTED PROCESSING WILL CONTINUE WITH INSTRUCTION EXECUTION FETCHED FROM PREVIOUS STEP. HOWEVER, IF AN NMI OR AN UNMASKED FIRQ OR IRQ CAUSED INTERRUPT, THE ADDRESS PLACED ON BUS FROM PREVIOUS CYCLE (M+1) REMAINS ON BUS AND PROCESSING CONTINUES WITH THIS CYCLE AS (m+1) OR (n+1) OF INTERRUPT TIMING.
2. IF MASK BITS ARE CLEAR IRQ & FIRQ MUST BE HELD LOW FOR THREE CYCLES TO GUARANTEE INTERRUPT TO BE TAKEN, ALTHOUGH ONLY ONE CYCLE IS NECESSARY TO BRING THE PROCESSOR OUT OF SYNC.

S6809 Instruction Set Tables

The instructions of the S6809 have been broken down into six different categories. They are as follows:

8-Bit Operation (Table 4)
16-Bit Operation (Table 5)
Index Register/Stack Pointer Instructions (Table 6)
Relative Branches (Long and Short) (Table 7)
Miscellaneous Instructions (Table 8)
Hexadecimal Value Instructions (Table 9)

Table 4. 8-Bit Accumulator and Memory Instructions

Mnemonic(s)	Operation
ADCA, ADCB	Add memory to accumulator with carry
ADDA, ADDB	Add memory to accumulator
ANDA, ANDB	And memory with accumulator
ASL, ASLA, ASLB	Arithmetic shift of accumulator or memory left
ASR, ASRA, ASRB	Arithmetic shift of accumulator or memory right
BITA, BITB	Bit test memory with accumulator
CLR, CLRA, CLRB	Clear accumulator or memory location
CMPA, CMPB	Compare memory from accumulator
COM, COMA, COMB	Complement accumulator or memory location
DAA	Decimal adjust A-accumulator
DEC, DECA, DECB	Decrement accumulator or memory location
EORA, EORB	Exclusive OR memory with accumulator
EXG R1, R2	Exchange R1 with R2 (R1, R2=A, B, CC, DP)
INC, INCA, INCB	Increment accumulator or memory location
LDA, LDB	Load accumulator from memory
LSL, LSLA, LSLB	Logical shift left accumulator or memory location
LSR, LSRA, LSRB	Logical shift right accumulator or memory location
MUL	Unsigned multiply (A x B→D)
NEG, NEGA, NEGB	Negate accumulator or memory
ORA, ORB	OR memory with accumulator
ROL, ROLA, ROLB	Rotate accumulator or memory left
ROR, RORA, RORB	Rotate accumulator or memory right
SBCA, SBCB	Subtract memory from accumulator with borrow
STA, STB	Store accumulator to memory
SUBA, SUBB	Subtract memory from accumulator
TST, TSTA, TSTB	Test accumulator or memory location
TFR, R1, R2	Transfer R1 to R2 (R1, R2=A, B, CC, DP)

NOTE: A, B, CC, or DP may be pushed to (pulled from) either stack with PSHS, PSHU, (PULS, PULU) instructions.

Table 5. 16-Bit Accumulator and Memory Instructions

Mnemonic(s)	Operation
ADDD	Add memory to D accumulator
CMPD	Compare memory from D accumulator
EXG D, R	Exchange D with X, Y, S, U or PC
LDD	Load D accumulator from memory
SEX	Sign Extend B accumulator into A accumulator
STD	Store D accumulator to memory
SUBD	Subtract memory from D accumulator
TFR D, R	Transfer D to X, Y, S, U or PC
TFR R, D	Transfer X, Y, S, U or PC to D

Table 6. Index Register/Stack Pointer Instructions

Mnemonic(s)	Operation
CMPS, CMPU	Compare memory from stack pointer
CMPX, CMPY	Compare memory from index register
EXG R1, R2	Exchange D, X, Y, S, U or PC with D, X, Y, S, U or PC
LEAS, LEAU	Load effective address into stack pointer
LEAX, LEAY	Load effective address into index register
LDS, LDU	Load stack pointer from memory
LDX, LDY	Load index register from memory
PSHS	Push any register(s) onto hardware stack (except S)
PSHU	Push any register(s) onto user stack (except U)
PULS	Pull any register(s) from hardware stack (except S)
PULU	Pull any register(s) from hardware stack (except U)
STS, STU	Store stack pointer to memory
STX, STY	Store index register to memory
TFR R1, R2	Transfer D, X, Y, S, U or PC to D, X, Y, S, U or PC
ABX	Add B accumulator to X (unsigned)

Table 7. Branch Instructions

Mnemonic(s)	Operation
BCC, LBCC	Branch if carry clear
BCS, LBCS	Branch if carry set
BEQ, LBEQ	Branch is equal
BGE, LBGE	Branch if greater than or equal (signed)
BGT, LBGT	Branch if greater (signed)
BHI, LBHI	Branch if higher (unsigned)
BHS, LBHS	Branch is higher or same (unsigned)
BLE, LBLE	Branch if less than or equal (signed)
BLO, LBLO	Branch if lower (unsigned)
BLS, LBLS	Branch if lower or same (unsigned)
BLT, LBLT	Branch if less than (signed)
BMI, LBMI	Branch if minus
BNE, LBNE	Branch if not equal
BPL, LBPL	Branch is plus
BRA, LBRA	Branch always
BRN, LBRN	Branch never
BSR, LBSR	Branch to subroutine
BVC, LBVC	Branch if overflow clear
BVS, LBVS	Branch if overflow set

Table 8. Miscellaneous Instructions

Mnemonic(s)	Operation
ANDCC	AND condition code register
CWAI	AND conditon code register, then wait for interrupt
NOP	No operation
ORCC	OR condition code register
JMP	Jump
JSR	Jump to subroutine
RTI	Return from interrupt
RTS	Return from subroutine
SWI, SWI2, SWI3	Software interrupt (absolute indirect)
SYNC	Synchronize with interrupt line

AMERICAN MICROSYSTEMS, INC.

PRELIMINARY DATA SHEET

S6809E/S68A09E/S68B09E

8-BIT MICROPROCESSING UNIT

Features

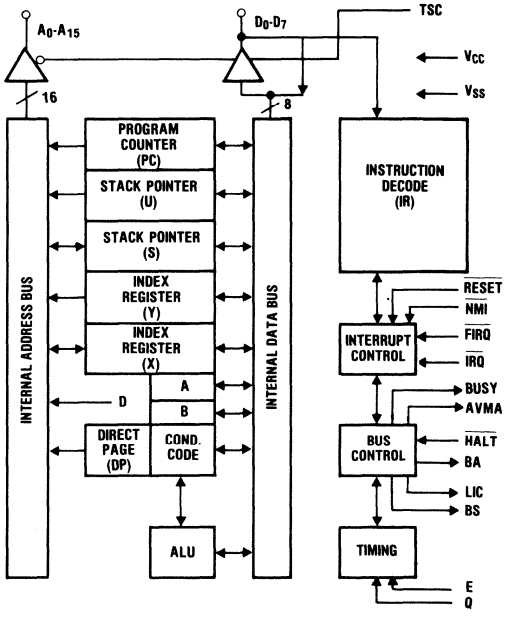
- ☐ Interfaces With All S6800 Peripherals
- ☐ Upward Compatible Instruction Set and Addressing Modes
- ☐ Upward Source Compatible Instruction Set and Addressing Modes
- ☐ Two 8-Bit Accumulators Can Be Concatenated Into One 16-Bit Accumulator
- ☐ External Clock Inputs, E and Q, Allow System Synchronization

General Description

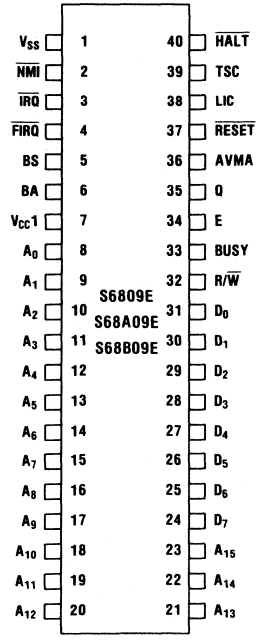
The S6809E is an advanced processor within the S6800 family offering greater throughput, improved byte efficiency, and increased adaptability to various software disciplines. These include position independence, reentrancy, recursion, block structuring, and high level language generation.

Because the S6809E supports *position-independent* code, software can be written in modular form for easy user expansion as system requirements increase. The S6809E is hardware compatible with all S6800 peripherals, and any assembly language code prepared for the S6800 can be passed through the S6809 assembler to produce code which will run on the S6809E.

Block Diagram



Pin Configuration



S6809E Hardware Features

- ☐ Fast Interrupt Request Input: Stacks Only Program Counter and Condition Code
- ☐ Interrupt Acknowledge Output Allows Vectoring by Devices
- ☐ Three Vectored Priority Interrupt Levels
- ☐ SYNC Acknowledge Output Allows for Synchronization to External Event
- ☐ NMI Blocked After RESET Until After First Load of Stack Pointer
- ☐ Early Address Valid Allows Use With Slow Memories
- ☐ Last Instruction Cycle Output (LIC) for Signalling Opcode Fetch
- ☐ Busy Output Eases Multiprocessor Design

Instruction Set

- ☐ Extended Range Branches
- ☐ Load Effective Address
- ☐ 16-Bit Arithmetic
- ☐ 8×8 Unsigned Multiply (AccumulatorA*B)
- ☐ SYNC Instruction—Provides Software Sync With an External Hardware Process
- ☐ Push and Pull on 2 Stacks
- ☐ Push/Pull Any or All Registers
- ☐ Index Registers May be Used as a Stack Pointer
- ☐ Transfer/Exchange all Registers

Addressing Modes

- ☐ All S6800 Modes Plus PC Relative Extended Indirect, Indexed Indirect, and PC Relative Indirect
- ☐ Direct Addressing Available Anywhere in Memory Map
- ☐ PC Relative Addressing: Byte Relative (±32,768 Bytes From PC)
- ☐ Complete Indexed Addressing Including Automatic Increment and Decrement, Register Offsets, and Four Indexable Register (X, Y, U and S)
- ☐ Expanded Index Addressing
  - ☐ 0, 5, 8, 16-Bit Constant Offset
  - ☐ 8, 16-Bit Accumulator Offsets

The S6809E gives the user 8- and 16-bit word capability with several hardware enhancements in the design such as the Fast Interrupt Request ($\overline{FIRQ}$), Memory Ready (MRDY), and Quadrature (Q_{OUT}) and System Clock Outputs (E_{OUT}). With the Fast Interrupt Request ($\overline{FIRQ}$) the S6809E places *only* the Program Counter and Condition Code Register on the stack prior to accessing the $\overline{FIRQ}$ vector location. The Memory Ready ($\overline{MRDY}$) input allows extension of the data access time for use with slow memories. The System Clock (E_{OUT}) operates at the basic processor frequency and can be as the synchronization signal for the entire system. The Quadrature Output (Q_{OUT}) provides additional system timing by signifying that address and data are stable.

The External Clock mode of the S6809E is particularly useful when synchronizing the processor to an externally generated signal. The Three-State Control input ($\overline{TSC}$) places the Address and R/$\overline{W}$ line in the high impedance state for DMA or Memory Refresh. The last Instruction Cycle (LIC) is activated during the last cycle of any instruction. This signifies that the next instruction cycle is the opcode fetch. The Processor Busy signal (BUSY) facilitates multiprocessor applications by allowing the designer to insure that flags being modified by one processor are not accessed by another simultaneously.

The S6809E features a family of addressing capabilities which can use any of the four index registers and stack pointers as a pointer to the operand (or the operand address). This pointer can have a fixed or variable signed offset that can be automatically incremented or decremented. The eight-bit direct page register permits a user to determine which page of memory is accessed by the instructions employing "page zero" addressing. This quick access to any page is especially useful in multitasking applications.

The S6809E has three vectored priority-interrupt levels, each of which automatically disables the lower priority interrupt while leaving the higher priority interrupt enabled.

The S6809E gives the system designer greater flexibility (through modular relocatable code) to enable the user to reduce system software costs while at the same time increasing software reliability and efficiency.

Electrical Characteristics (V_{CC}=5.0V ±5%; V_{SS}=0, T_A=0°C to +70°C unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max.	Units	Condition
V_{IH}	Input High Voltage — Logic, Q	V_{SS}+2.0	—	V_{CC}	V_{DC}	
V_{IHR}	$\overline{RESET}$	V_{SS}+4.0	—	V_{CC}	V_{DC}	
V_{IHC}	E	V_{CC}−0.75	—	V_{CC}+0.3		
V_{IL}	Input Low Voltage — Logic, Q, $\overline{RESET}$	V_{SS}−0.3	—	V_{SS}+0.8	V_{DC}	
V_{ILC}	E	V_{SS}−0.3	—	V_{SS}+0.4		
I_{IN}	Input Leakage Current — Logic, E, Q, $\overline{RESET}$	—	1.0	2.5	μAdc	V_{IN}=0 to 5.25 V_{CC}
V_{OL}	Output High Voltage — D_0-D_7	V_{SS}+2.0	—	—	V_{DC}	I_{LOAD}=−205μAdc
	A_0-A_{15}, R/$\overline{W}$	V_{SS}+2.0	—	—		I_{LOAD}=−145μAdc
						V_{CC}=Min.
	BA, BS, LIC, AVMA, BUSY	—	—	V_{SS}+0.8		I_{LOAD}=−100μAdc
V_{OL}	Output Low Voltage	—	—	V_{SS}+0.8	V_{DC}	I_{LOAD}=2.0mAdc V_{CC}=Min.
P_D	Output Low Voltage	—	—	1.0	W	
C_{IN}	Capacitance — D_0-D_7, Logic, Q, $\overline{RESET}$	—	10	15	pF	V_{IN}=0 T_A=25°C f=1Mhz
	E	—	30	50		
C_{OUT}	A_0-A_{15}, R/$\overline{W}$, BA, BS	—	10	15		
	LIC, AVMA, BUSY	—	10	15		
f	Frequency — S6809E	0.1	—	1.0	MHz	
f	S68A09E	0.1	—	1.5		
f	S68B09E	0.1	—	2.0		
I_{TSI}	Tri-State (Off) Input Current — D_0-D_7	—	2.0	10	μAdc	V_{IN}=0.4 to 2.4
	A_0-A_{15}, R/$\overline{W}$	—	—	100		V_{CC}=Max.

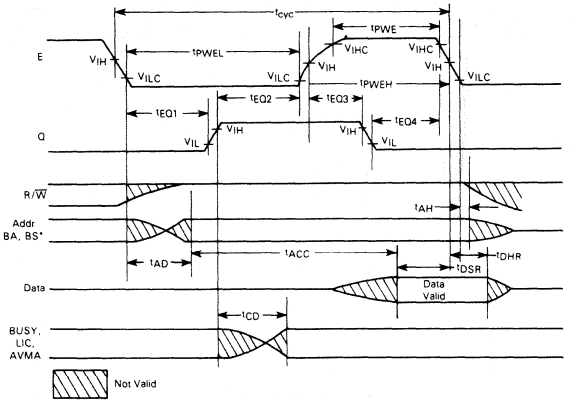
Read/Write Timing (Reference Figures 1 and 2)

Symbol	Characteristic	S6809E			S68A09E			S68B09E			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{CYC}	Cycle Time	1000	—	10000	667	—	10000	500	—	10000	ns
t_{ACC}	Peripheral Read Access Time $t_{CYC}-t_{EF}-t_{AD}-t_{DSR}=t_{ACC}$	695	—	—	440	—	—	320	—	—	ns
t_{DSR}	Data Setup Time (Read)	80	—	—	60	—	—	40	—	—	ns
t_{DHR}	Input Data Hold Time	10	—	—	10	—	—	10	—	—	ns
t_{DHW}	Output Data Hold Time	30	—	—	30	—	—	30	—	—	ns
t_{AH}	Address Hold Time (Address, R/$\overline{W}$)	20	—	—	20	—	—	20	—	—	ns
t_{AD}	Address Delay	—	—	200	—	—	140	—	—	110	ns
t_{DDW}	Data Delay Time (Write)	—	—	200	—	—	140	—	—	110	ns
t_{PWEL}	E Clock Low	450	—	9500	295	—	9500	210	—	9500	ns
t_{PWEH}	E Clock High (Measured at V_{IH})	450	—	9500	280	—	9500	220	—	9500	ns
t_{PWE}	E Clock High (Measured at V_{IHC})	370	—	9500	220	—	9500	180	—	9500	ns
t_{Er}, t_{Ef}	E Rise and Fall Time	5	—	25	5	—	25	5	—	20	ns
t_{PWQH}	Q Clock High	450	—	—	280	—	—	220	—	—	ns
t_{Qr}, t_{Qf}	Q Rise and Fall Time	5	—	25	5	—	25	5	—	20	ns
t_{EQ1}	E Low to Q Rising	200	—	—	133	—	—	100	—	—	ns
t_{EQ2}	Q High to E Rising	200	—	—	133	—	—	100	—	—	ns
t_{EQ3}	E High to Q Falling	200	—	—	133	—	—	100	—	—	ns
t_{EQ4}	Q Low to E Falling	200	—	—	133	—	—	100	—	—	ns

Read/Write Timing (Continued)

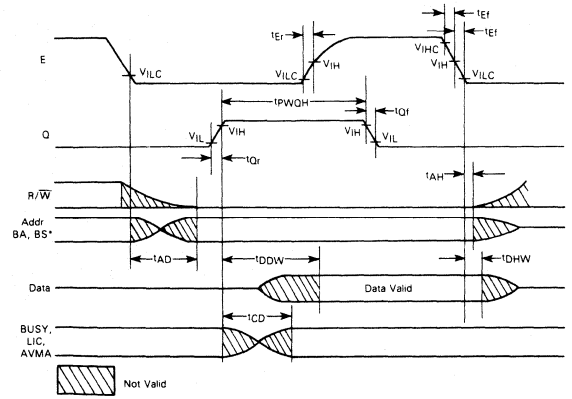
Symbol	Characteristic	S6809E			S68A09E			S68B09E			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{PCS}	Interrupts $\overline{HALT}$, $\overline{RESET}$ and TSC Setup Time	200	—	—	140	—	—	110	—	—	ns
t_{THT}	TSC Hold Time	500	—	—	333	—	—	250	—	—	ns
t_{TSA}	TSC Drive to Valid Logic Levels	—	—	210	—	—	150	—	—	120	ns
t_{TSR}	TSC Release MOS Buffers to High Impedance	—	—	200	—	—	140	—	—	110	ns
t_{TSD}	TSC Three-State Delay	—	—	120	—	—	85	—	—	80	ns
t_{CD}	Control Delay (BUSY, LIC, AVMA)	—	—	200	—	—	140	—	—	110	ns
t_{PCr}, t_{PCf}	Processor Control Rise/Fall	—	—	100	—	—	100	—	—	100	ns

Figure 1. Read Data From Memory of Peripherals



Note: Waveform measurements for all inputs and outputs are specified at logic high = V_{IHMIN} and logic low = V_{ILMAX} unless otherwise specified.

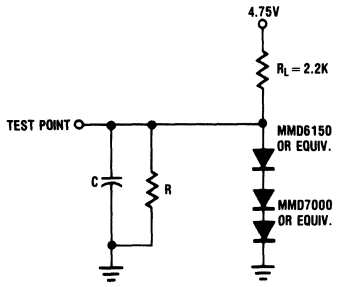
Figure 2. Write Data to Memory or Peripherals



*Hold time for BA, BS not specified

Note: Waveform measurements for all inputs and outputs are specified at logic high = V_{IHMIN} and logic low = V_{ILMAX} unless otherwise specified.

Figure 3. Bus Timing Test Load



C = 30pF FOR BA, BS
130pF FOR D0-D7, E, Q
90pF FOR A0-A15, R/W

R = 11.7kΩ FOR D0-D7
16.5kΩ FOR A0-A15, E, Q
24kΩ FOR BA, BS

Programming Model.

As shown in Figure 4, the S6809E adds three registers to the set available in the S6800. The added registers include a direct page register, the User Stack pointer and a second Index Register.

Accumulators (A, B, D). The A and B registers are general purpose accumulators which are used for arithmetic calculations and manipulation of data.

Certain instructions concatenate the A and B registers to form a single 16-bit accumulator. This is referred to as the D register, and is formed with the A register as the most significant byte.

Direct Page Register (DP). The Direct Page Register of the S6809E serves to enhance the Direct Addressing Mode. The content of this register appears at the higher address outputs (A_8-A_{15}) during direct Addressing Instruction execution. This allows the direct mode to be used at any place in memory, under program control. To allow 6800 compatibility, all bits of this register are cleared during Processor Reset.

Figure 4. Programming Model of the Microprocessing Unit

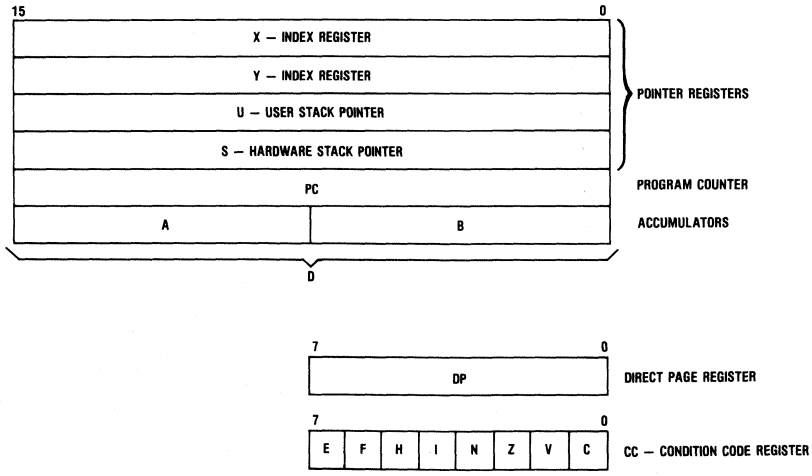
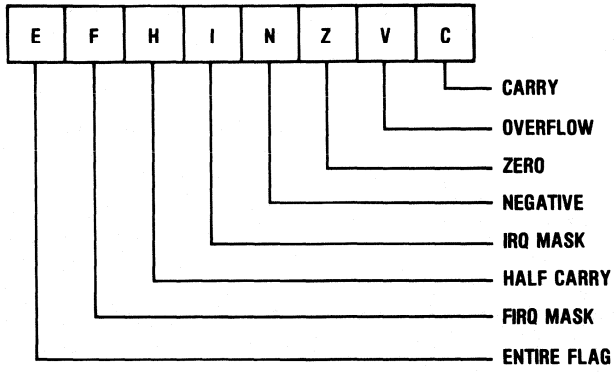


Figure 5. Condition Code Register Format



Index Registers. The Index Registers are used in indexed mode of addressing. The 16-bit address in this register takes part in the calculation of effective addresses. This address may be used to point to data directly or may be modified by an optional constant or register offset. During some indexed modes, the contents of the index register are incremented and decremented to point to the next item of tabular type data. All four pointer registers (X, Y, U, S) may be used as index registers.

Stack Pointers (U, S). The Hardware Stack Pointer (S) is used automatically by the processor during subroutine calls and interrupts. The stack pointers of the S6809E point to the top of the stack, in contrast to the S6800 stack pointer which pointed to the next free location on the stack. The User Stack Pointer (U) is controlled exclusively by the programmer thus allowing arguments to be passed to and from subroutines with ease. Both Stack Pointers have the same indexed mode addressing capabilities as the X and Y registers, but also support **Push** and **Pull** instructions. This allows the S6809E to be used efficiently as a stack processor, greatly enhancing its ability to support higher level languages and modular programming.

Program Counter. The Program Counter is used by the processor to point to the address of the next instruction to be executed by the processor. Relative Addressing is provided allowing the Program Counter to be used like an index register in some situations.

Condition Code Register.

The condition code register defines the State of the Processor at any given time, see Figure 5.

Bit 0 (C). Bit 0 is the Carry Flag, and is usually the carry from the binary ALU. C is also used to represent a 'borrow' from subtract like instructions (CMP, NEG, SUB, SBC). Here the carry flag is the complement of the carry from binary ALU.

Bit 1 (V). Bit 1 is the overflow flag, and is set to a one by an operation which causes a signed two's complement arithmetic overflow. This overflow is detected in an operation in which the carry from the MSB in the ALU does not match the carry from the MSB-1.

Bit 2 (Z). Bit 2 is the zero flag, and is set to a one if the result of the previous operation was identically zero.

Bit 3 (N). Bit 3 is the negative flag, which contains exactly the value of the MSB of the result of the preceding operation. Thus, a negative two's-complement result will leave N set to a one.

Bit 4 (I). Bit 4 is the $\overline{\text{IRQ}}$ mask bit. The processor will not recognize interrupts from the IRQ line if this bit is set to a one. $\overline{\text{NMI}}$, $\overline{\text{FIRQ}}$, $\overline{\text{IRQ}}$, $\overline{\text{RESET}}$, and SWI all set I to a one; SWI2 and SWI3 do not affect I.

Bit 5 (H). Bit 5 is the half-carry bit, and is used to indicate a carry from bit 3 in the ALU as a result of an 8-bit addition only (ABC or ADD). This bit is used by the DAA instruction to perform a BCD decimal add adjust operation. The state of this flag is undefined in all subtract-like instructions.

Bit 6 (F). Bit 6 is the $\overline{\text{FIRQ}}$ mask bit. The processor will not recognize interrupts from the FIRQ line if this bit is a one. $\overline{\text{NMI}}$, $\overline{\text{FIRQ}}$, SWI, and $\overline{\text{RESET}}$ all set F to a one. $\overline{\text{IRQ}}$, SWI2 and SWI3 do not affect F.

Bit 7 (E). Bit 7 is the entire flag, and when set to a one indicates that the complete machine state (all the registers) was stacked, as opposed to the subset state (PC and CC). The E bit of the *stacked* CC is used on a return from interrupt (RTI) to determine the extent of the unstacking. Therefore, the current E left in the Condition Code Register represents past action.

S6809E MPU Signal Description

Power (V_{SS}, V_{CC}). Two pins are used to supply power to the part: V_{SS} is ground or 0 volts, while V_{CC} is +5.0V ±5%.

Address Bus (A_0-A_{15}). Sixteen pins are used to output address information from the MPU onto the Address Bus. When the processor does not require the bus for a data transfer, it will output address $FFFF_{16}$, R/$\overline{W}$=1, and BS=0. Addresses are valid on the rising edge of Q (see Figures 1 and 2). All address bus drivers are made high-impedance when output Bus Available (BA) is high or when TSC is asserted. Each pin will drive on Schottky TTL load and typically 90pF.

Data Bus (D_0-D_7). These eight pins provide communication with the system bi-directional data bus. Each pin will drive one Schottky TTL load and typically 130pF.

Read/Write (R/$\overline{W}$). This signal indicates the direction This signal indicates the direction of the data transfer on the data bus. A low indicates that the MPU is writing data onto the data bus. R/$\overline{W}$ is made high impedance when BA is high or when TSC is asserted. R/$\overline{W}$ is valid on the rising edge of Q, refer to Figures 1 and 2.

$\overline{RESET}$. A low level on this Schmitt-trigger input for greater than one bus cycle will reset the MPU as shown in Figure 6. The Reset vectors are fetched from locations $FFFE_{16}$ and $FFFF_{16}$ (Table 1) when Interrupt Acknowledge is true, (BA∧BS=1). During intial power-on, the Reset line should be held low until the clock input signals are fully operational; see Figure 7.

Because the S6809E Reset pin has a Schmitt-trigger input with a threshold voltage higher than that of standard peripherals, a simple R/C network may be used to reset the entire system. This higher threshold voltage insures that all peripherals are out of the reset state before the Processor.

$\overline{HALT}$. A low level on this input pin will cause the MPU to stop running at the end of the present instruction and remain halted indefinitely without loss of data. When Halted, the BA output is driven high indicating the buses are high-impedance. BS is also high which indicates the processor is in the Halt or Bus Grant state. While halted, the MPU will not respond to external real-time requests ($\overline{FIRQ}$, $\overline{IRQ}$ and $\overline{NMI}$ or $\overline{RESET}$ will be latched for later response. During the Halt state Q and E continue to run normally. If the MPU is not running ($\overline{RESET}$), a halted state (BA and BS=1) can be achieved by pulling $\overline{HALT}$ low while $\overline{RESET}$ is still low.

Bus Available, Bus Status (BA, BS). The Bus Available output is an indication of an internal control signal which makes the MOS buses of the MPU high-impedance. The signal does not imply that the bus will be available for more than one cycle. When BA goes low, an additional dead cycle will elapse before the MPU acquires the bus. BA will not be asserted when TSC is active.

The Bus Status output signal, when decoded with BA, represents the MPU state (valid with leading edge of Q):

MPU State		
BA	**BS**	
0	0	Normal (Running)
0	1	Interrupt Acknowledge
1	0	SYNC Acknowledge
1	1	HALT or Bus Grant

Interrupt Acknowledge is indicated during both cycles of a hardware-vector-fetch ($\overline{RESET}$, $\overline{NMI}$, $\overline{FIRQ}$, $\overline{IRQ}$, SWI, SWI2, SWI3). This signal, plus decoding of the lower 4 address lines can provide the user with an indication of which interrupt level is being serviced and allow vectoring by device (see Table 1).

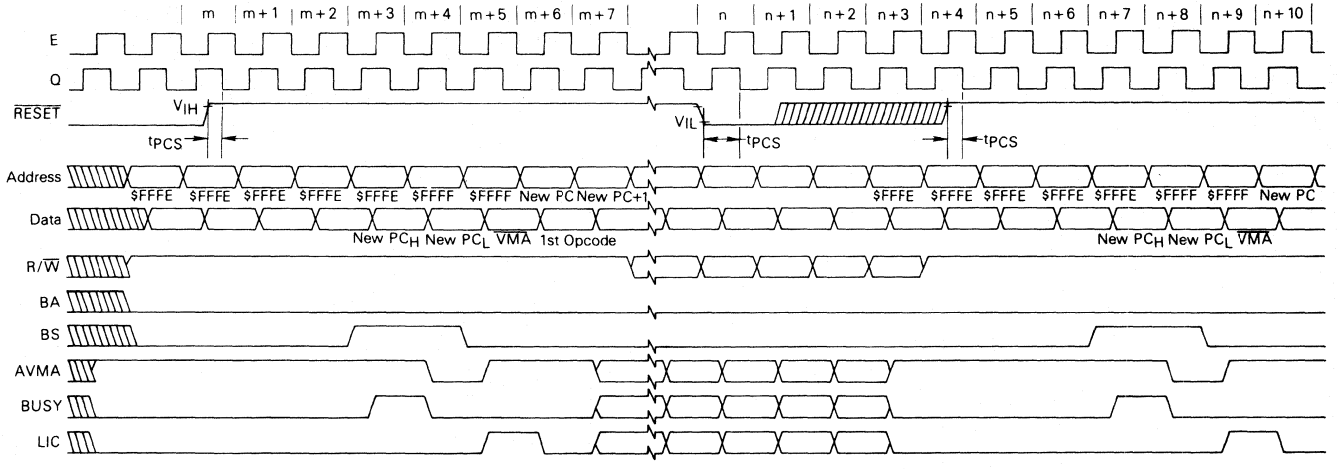
Table 1. Memory Map for Interrupt Vectors

Memory Map for Vector Location		Interrupt Vector Description
MS	**LS**	
FFFE	FFFF	$\overline{RESET}$
FFFC	FFFD	$\overline{NMI}$
FFFA	FFFB	SWI
FFF8	FFF9	$\overline{IRQ}$
FFF6	FFF7	$\overline{FIRQ}$
FFF4	FFF5	SWI2
FFF2	FFF3	SWI3
FFF0	FFF1	Reserved

Sync Acknowledge is indicated while the MPU is waiting for external synchronization on an interrupt line.

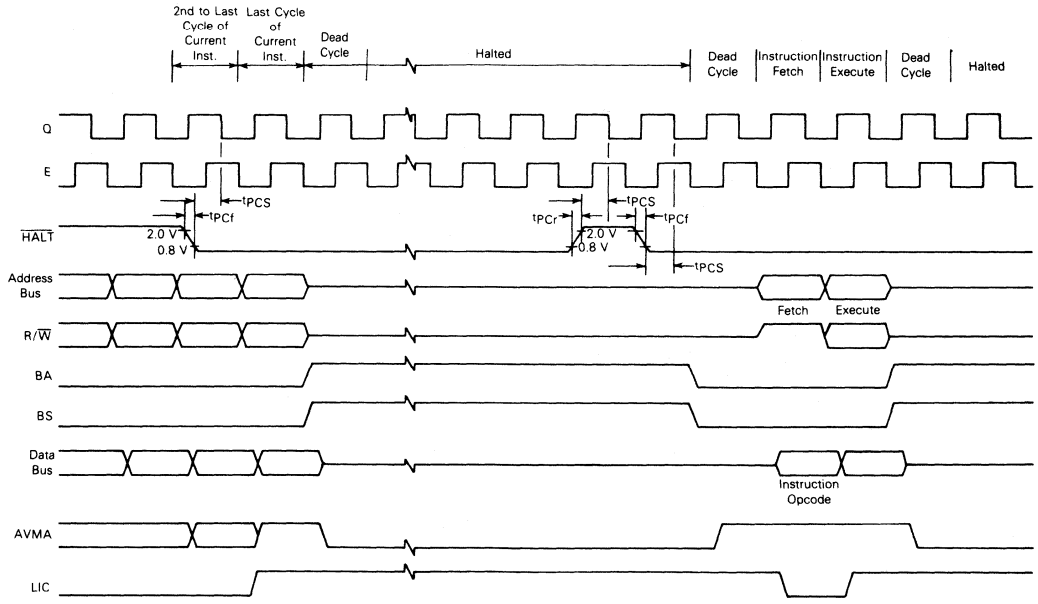
Halt is true when the S6809E is in a Halt condition.

Figure 6. $\overline{\text{RESET}}$ Timing



Note: Waveform measurements for all inputs and outputs are specified at logic high = V_{IHMIN} and logic low = V_{ILMAX} unless otherwise specified.

Figure 7 — $\overline{\text{HALT}}$ and Single Instruction Execution Timing for System Debug



Note: Waveform measurements for all inputs and outputs are specified at logic high = V_{IHMIN} and logic low = V_{ILMAX} unless otherwise specified.

*Note: $\overline{\text{NMI}}$, $\overline{\text{FIRQ}}$ and $\overline{\text{IRQ}}$ requests are latched by the falling edge of every Q. From this point, a delay of at least one bus cycle will occur before the interrupt is serviced by the MPU.

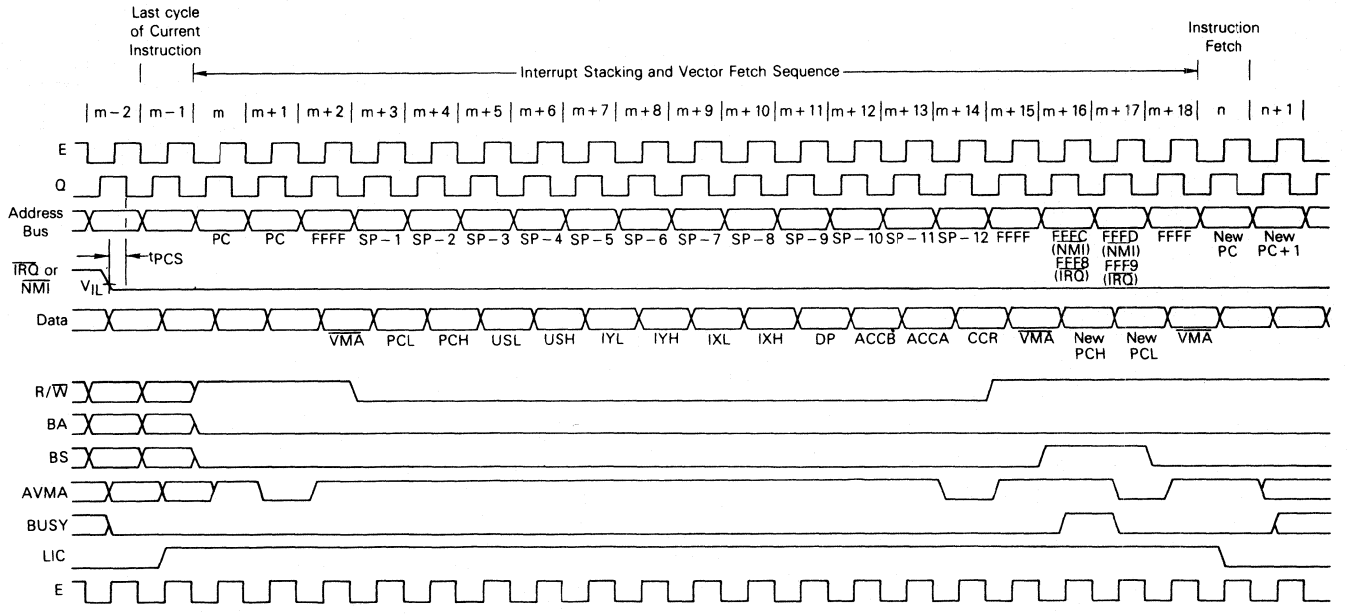
Non-Maskable Interrupt ($\overline{\text{NMI}}$). A negative edge on this input requests that a non-maskable interrupt sequence be generated. A non-maskable interrupt cannot be inhibited by the program, and also has a higher priority than $\overline{\text{FIRQ}}$, $\overline{\text{IRQ}}$ or software interrupts. During recognition of an $\overline{\text{NMI}}$, the entire machine state is saved on the hardware stack. After reset, an $\overline{\text{NMI}}$ will not be recognized until the first program load of the Hardware Stack Pointer (S). The pulse width of $\overline{\text{NMI}}$ low must be at least one E cycle. If the $\overline{\text{NMI}}$ input does not meet the minimum set up with respect to Q, the interrupt will not be recognized until the next cycle. See Figure 8.

Fast-Interrupt Request ($\overline{\text{FIRQ}}$). A low level on this input pin will initiate a fast interrupt sequence, provided its mask bit (F) in the CC is clear. This sequence has priority over the standard Interrupt Request ($\overline{\text{IRQ}}$), and is fast in the sense that it stacks only the contents of the condition code register and the program counter. The interrupt service routine should clear the source of the interrupt before doing an RTI. See Figure 9.

Interrupt Request ($\overline{\text{IRQ}}$). A low level input on this pin will initiate an Interrupt Request sequence provided the mask bit (I) in the CC is clear. Since $\overline{\text{IRQ}}$ stacks the entire machine state it provides a slower response to interrupts than $\overline{\text{FIRQ}}$. $\overline{\text{IRQ}}$ also has a lower priority than $\overline{\text{FIRQ}}$. Again, the interrupt service routine should clear the source of the interrupt before doing an RTI. See Figure 8.

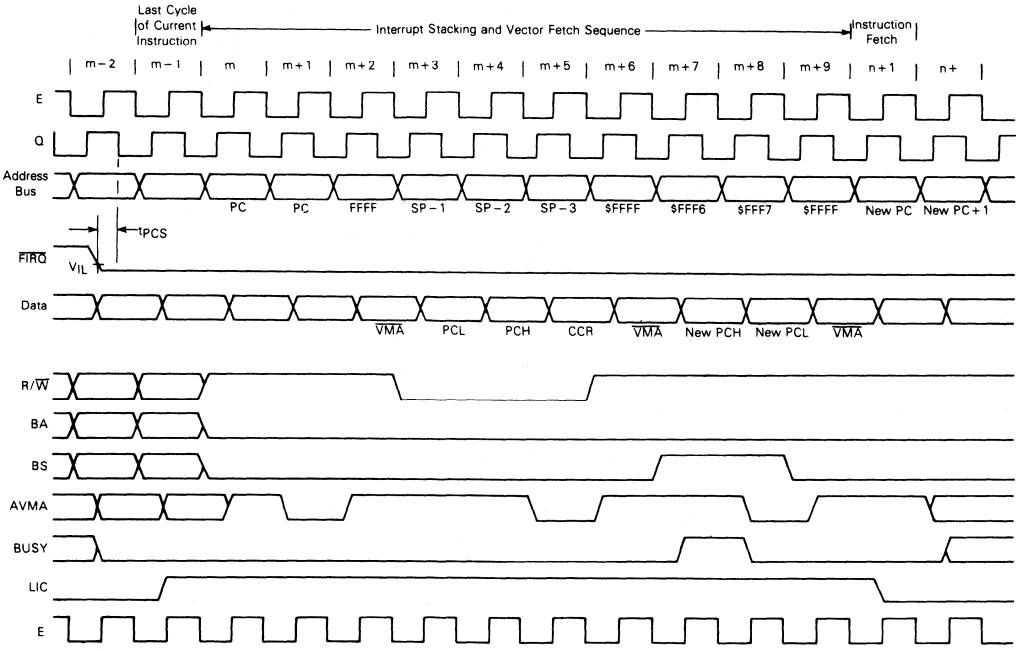
E and Q Clock Inputs The E and Q inputs are the clock signals required by the S6809E. The E signal is similar to the ϕ_2 signal of the S6800. Data is latched on the trailing edge of the E signal. The Q is a Quadrature clock, and is used to signal the validity of the addresses on the address bus. The Q input is TTL compatible, the E input however, directly drives the internal MOS circuitry. As a result, the E signal's levels must be higher than TTL levels, to minimize internal skew. The required signals are shown in Figures 1 and 2. Figure 11 shows the circuitry required to generate the proper signals. A 74LS73 is required, as the other 7473 series are level triggered rather than edge-triggered, and will not generate the proper waveforms.

Figure 8. $\overline{IRQ}$ and $\overline{NMI}$ Interrupt Timing



Note: Waveform measurements for all inputs and outputs are specified at logic high = V_{IHMIN} and logic low = V_{ILMAX} unless otherwise specified.
E clock shown for reference only.

Figure 9. $\overline{FIRQ}$ Interrupt Timing



Note: Waveform measurements for all inputs and outputs are specified at logic high = V_{INMIN} and logic low = V_{ILMAX} unless otherwise specified.
E clock shown for reference only.

Figure 10. E/Q Relationship

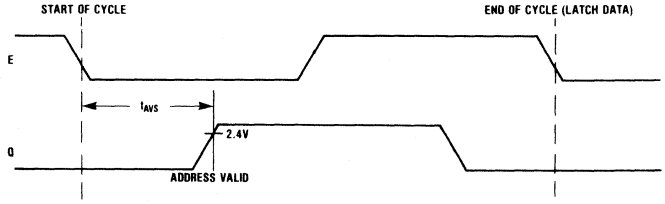


Figure 11. S6809E Clock Generator

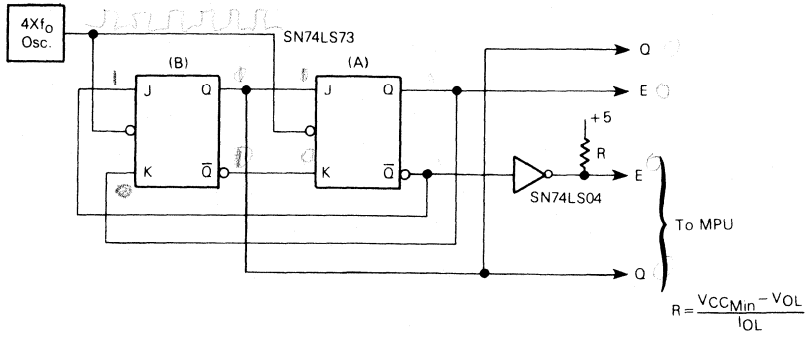
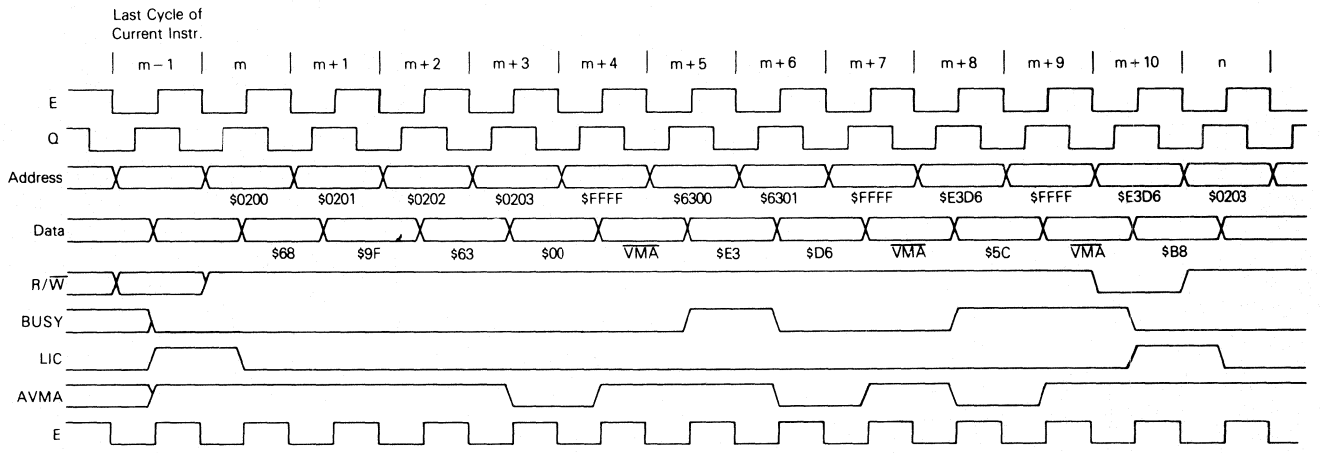


Figure 12a. Busy Timing



Note: Waveform measurements for all inputs and outputs are specified at logic high = V_{IHMIN} and logic low = V_{ILMAX} unless otherwise specified.

Figure 12b. Read-Modify-Write Instruction Example (ASL Extended Indirect)

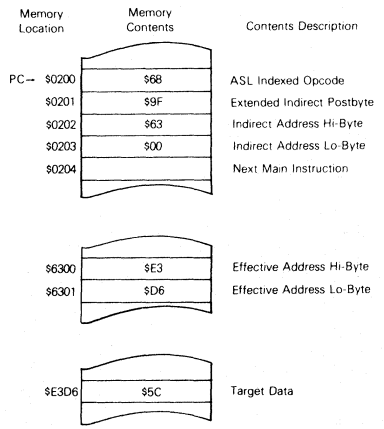
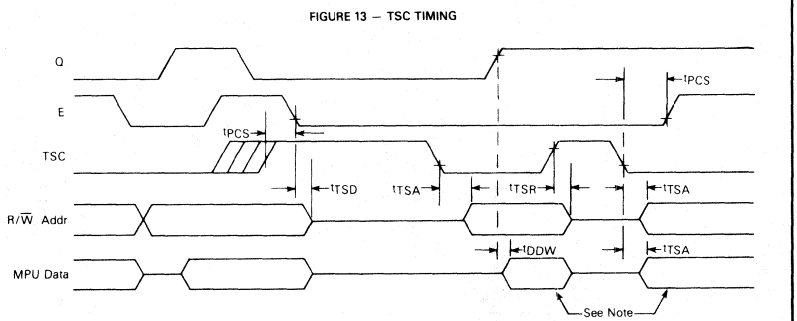


Figure 13. TSC Timing



Notes: Data will be asserted by the MPU only during the interval while R/W is low and E or Q is high.
Waveform measurements for all inputs and outputs are specified at logic high = V_{IHMIN} and logic low = V_{ILMAX} unless otherwise specified.

BUSY. The BUSY output is used for arbitration of the MPU bus. The BUSY signal signifies that the S6809E will need the bus for at least the next cycle, as it is in the middle of a multiple-byte data access. The BUSY signal will be high for the first two cycles of the operand fetch of any Read-Modify-Write instruction, high during the first operand fetch of any double-byte instructions (LDD, STD) and high during the first byte access of any indirect access or vector fetch operation. BUSY is not active during pushes or pulls from the stack (PUL, PSH). Figure 12 shows the timing for the BUSY signal for a Read-Modify-Write operation (ASL @6300).

AVMA. The AVMA output is an advanced Valid Memory Address signal. This output goes HIGH one cycle before the MPU performs a memory access. The advanced nature of this signal allows bus arbitration logic an advanced warning of potential bus conflict.

LIC. The LIC output is the Last Instruction Cycle signal. This signal's HIGH to LOW transition signals that the current MPU cycle is an opcode fetch. The LIC signal will be held HIGH when the MPU is Halted at the end of an instruction (i.e., not in CWAI or RESET), when the MPU is in the SYNC state or while it is stacking during interrupts.

TSC. The TSC input is a Tri-State-Control for the S6809E's Address, data and R/$\overline{W}$ buffers. To force the MPU into the High-impedance state, the TSC line should be brought HIGH t_{PCST} before the end of the current cycle. The clocks for the MPU are then stopped in the first quarter (E=0, Q=0) of the next cycle. To regain the bus, the TSC line should be brought low, and the clocks restarted.

The TSC HIGH state is latched on the trailing edge of E, and therefore should be timed accordingly.

MPU Operation. During normal operation, the MPU fetches an instruction from memory and then executes the requested function. This sequence begins at $\overline{RESET}$ and is repeated indefinitely unless altered by a special instruction or hardware occurrence. Software instructions that alter normal MPU operation are: SWI, SWI2, SWI3, CWAI, RTI and SYNC. An interrupt, $\overline{HALT}$ or $\overline{DMA/BREQ}$ can also alter the normal execution of instructions. Figure 15 illustrates the flowchart for the S6809E. The left-half of the flowchart represents normal operation; the right-half represents the flow when an interrupt or special instruction occurs.

Addressing Modes

The basic instructions of any computer are greatly enhanced by the presence of powerful addressing modes. The S6809E has the most complete set of addressing modes available on any microcomputer today. For example, the S6809E has 59 basic instructions, however it recognizes 1464 different variations of instructions and addressing modes. The new addressing modes support modern programming techniques. The following addressing modes are available on the S6809E.

- Inherent (Includes Accumulator)
- Immediate
- Extended
  - Extended Indirect
- Direct
- Register
- Indexed
  - Zero-Offset
  - Constant Offset
  - Auto Increment/Decrement
  - Indexed Indirect
- Relative
  - Short/Long Relative Branching
  - Program Counter Relative Addressing

Inherent (Includes Accumulator). In this addressing mode, the opcode of the instruction contains all the address information necessary. Examples of Inherent Addressing are: ABX, DAA, SWI, ASRA, CLRB.

Immediate Addressing. In Immediate Addressing, the effective addressing of the data is the location immed iately following the opcode; the data to be used in the instruction immediately follows the opcode of the instruction. The S6809E uses both 8 and 16-bit immediate values depending on the size of argument specified by the opcode. Examples of instructions with Immediate Addressing are:

```
LDA#$20
LDX#$F000
LDY#CAT
```

Note:# signifies Immediate addressing, $ signifies hexadecimal value.

Extended Addressing. In Extended Addressing the contents of the two bytes immediately following the opc ode fully specify the 16-bit effective address used by the instruction. Note that the address generated by an extended instruction defines an absolute address and is not position independent. Examples of Extended Addressing include:

```
LDA CAT
STX MOUSE
LDD $2000
```

Extended Indirect. As a special case of indexed addressing (discussed below), one level of indirection may be added to Extended Addressing. In Extended Indirect, the two bytes following the postbyte of an Indexed instruction contains the address of the address of the data.

```
LDA [CAT]
LDX [$FFFE]
STU [DOG]
```

Direct Addressing. Direct addressing is similar to extended addressing except that only one byte of address follows the opcode. This byte specifies the lower 8 bits of the address to be used. The upper 8 bits of the address are supplied by the direct page register. Since only one byte of address is required in direct addressing, this mode requires less memory and executes faster than extended addressing. Of course, only 256 locations (one page) can be accessed without redefining the contents of the DP register. Since the DP register is set to $00 on Reset, direct addressing on the S6809E is compatible with direct addressing on the S6800. Indirection is not allowed in direct addressing. Some examples of direct addressing are:

```
LDA    $30
SETDP  $10 (Assembler directive)
LDB    $1030
LDD    <CAT
```

Note: < is an assembler directive which forces direct addressing

Register Addressing. Some opcodes are followed by a byte that defines a register or set of registers to be used by the instruction, this is called a POSTBYTE. Some examples of register addressing are:

TFR	X,Y	Transfers X into Y
EXG	A,B	Exchanges A with B
PSHS	A,B,X,Y	Push onto SY,X,B, then A
PULU	X,Y,D	Pull from U D,X, then Y

Indexed Addressing. In all indexed addressing one of the pointer registers (X, Y, U, S, and sometimes PC) is used in a calculation of the effective address of the operand to be used by the instruction. Five basic types of indexing are available and are discussed below. The postbyte of an indexed instruction specifies the basic type and variation of the addressing mode as well as the pointer register to be used. Figure 16 lists the legal formats for the postbyte. Table 2 gives the assembler form and the number of cycles and bytes added to the basic values for indexed addressing for each variation.

Zero-Offset Indexed. In this mode, the selected pointer register contains the effective address of the data to be used by the instruction. This is the fastest indexing mode.

Examples are:

```
LDD 0,X
LDA 0,S
```

Constant Offset Indexed. In this mode a two's-complement offset and the contents of one of the pointer registers are added to form the effective address of the operand. The pointer register's initial content is unchanged by the addition.

Three sizes of offsets are available:

±4-bit (−16 to +15)
±7-bit (−128 to +127)
±15-bit (−32768 to +32767)

The two's complement 5-bit offset is included in the postbyte and therefore is most efficient in use of bytes and cycles. The two's complement 8-bit offset is contained in a single byte following the postbyte. The two's complement 16-bit offset is in the two bytes following the post-byte. In most cases the programmer need not be concerned with the size of this offset since the assembler will select the optional size automatically.

Examples of constant-offset indexing are:

```
LDA 23,X
LDX −2,S
LDY 300,X
LDU CAT,Y
```

Accumulator-Offset Indexed. This mode is similar to constant offset indexed except that the two's complement value in one of the accumulators (A, B or D) and the content of one of the pointer registers are added to form the effective address of the operand. The contents of both the accumulator and the pointer register are unchanged by the addition. The postbyte specifies which accumulator to use as an offset and no additional bytes are re-

Figure 15. Indexed Addressing Postbyte Register Bit Assignments

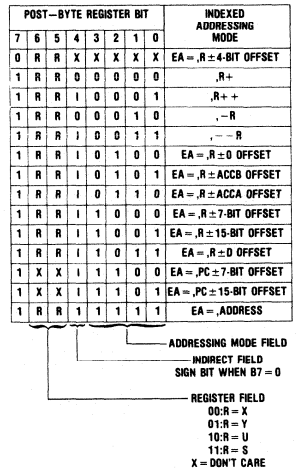


Table 2. Indexed Addressing Modes

Type	Forms	Non Indirect				Indirect			
		Assembler Form	Postbyte OP Code	+ ~	+ #	Assembler Form	Postbyte OP Code	+ ~	+ #
Constant Offset From R (Signed Offsets)	No Offset	,R	1RR00100	0	0	[,R]	1RR10100	3	0
	5-Bit Offset	n, R	0RRnnnnn	1	0	defaults to 8-bit			
	8-Bit Offset	n, R	1RR01000	1	1	[n, R]	1RR11000	4	1
	16-Bit Offset	n, R	1RR01001	4	2	[n, R]	1RR11001	7	2
Accumulator Offset From R (Signed Offsets)	A — Register Offset	A, R	1RR00110	1	0	[A, R]	1RR10110	4	0
	B — Register Offset	B, R	1RR00101	1	0	[B, R]	1RR10101	4	0
	D — Register Offset	D, R	1RR01011	4	0	D, R]	1RR11011	7	0
Auto Increment/Decrement R	Increment By 1	,R+	1RR00000	2	0	not allowed			
	Increment By 2	,R++	1RR00001	3	0	[,R++]	1RR10001	6	0
	Decrement By 1	,−R	1RR00010	2	0	not allowed			
	Decrement By 2	,−−R	1RR00011	3	0	[,−−R]	1RR10011	6	0
Constant Offset From PC	8-Bit Offset	n, PCR	1XX01100	1	1	[n, PCR]	1XX11100	4	1
	16-Bit Offset	n, PCR	1XX01101	5	2	[n, PCR]	1XX11101	8	2
Extended Indirect	16-Bit Address	—	—	—	—	[n]	10011111	5	2

$^{+}_{\sim}$ and $^{+}_{\#}$ indicate the number of additional cycles and bytes for the particular variation.

R = X, Y, U or S X = 00 Y = 01
X = Don't Care U = 10 S = 11

quired. The advantage of an accumulator offset is that the value of the offset can be calculated by a program at run-time.

Some examples are:

```
LDA B,Y
LDX D,Y
LEAX B,X
```

Auto Increment/Decrement Indexed. In the auto increment addressing mode, the pointer register contains the address of the operand. Then, after the pointer register is used it is incremented by one or two. This addressing mode is useful in stepping through tables, moving data, or for the creation of software stacks. In auto decrement, the pointer register is decremented prior to use as the address of the data. The use of auto decrement is similar to that of auto increment but the tables, etc. are scanned from the high to low addresses. The size of the increment/decrement can be either one or two to allow for tables of either 8 or 16-bit data to be accessed and is selectable by the programmer. The pre-decrement, post-increment nature of these modes allow them to be used to create additional software stacks that behave identically to the U and S stacks.

Some examples of the auto increment/decrement addressing modes are:

```
LDA ,X+
STD ,Y++
LDBL ,−Y
LDX ,−−S
```

Indexed Indirect. All of the indexing modes with the exception of auto increment/decrement by one, or a ±4-bit offset may have an additional level of indirection specified. In Indirect addressing, the effective address is contained at the location specified by the content of the Index register plus any offset. In the example below, the A accumulator is loaded indirectly using an effective address calculated from the Index register and an offset.

```
                                  Before Execution
                                  A=XX (don't care)
                                  X=$F000
$0100 LDA      [10,X]             EA is now $F010
$F011                             F150 is now the new EA
$F150
                                  After Execution
                                  A=$AA Actual Data Loaded
```

All modes of indexed indirect are included except those which are meaningless (e.g., auto increment/decrement by 1 indirect). Some examples of indexed indirect are:

```
LDA [,X]
LDD [10,S]
LDA [B,Y]
LDD [,X++]
```

Relative Addressing. The bytes(s) following the branch opcode is (are) treated as a signed offset which is added to the program counter. If the branch condition is true then the calculated address (PC + signed offset) is loaded into the program counter. Program execution continues at the new location as indicated by the PC; Short (1 byte offset) and long (2 bytes offset) relative addressing modes are available. All of memory can be reached in long relative addressing as an effective address is interpreted modulo 2^{16}. Some examples of relative addressing are:

```
        BEQ   CAT      (short)
        BGT   DOG      (short)
CAT     LBEQ  RAT      (long)
DOG     LBGT  RABBIT   (long)
        •
        •
        •
RAT     NOP
RABBIT  NOP
```

Program Counter Relative. The PC can be used as the pointer register with 8 or 16-bit signed offsets. As in relative addressing the offset is added to the current PC to create the effective address. The effective address is then used as the address of the operand or data. Program Counter Relative Addressing is used for writing position independent programs. Tables related to a particular routine will maintain the same relationship after the routine is moved, if referenced relative to the Program Counter. Examples are:

```
LDA     CAT,PCR
LEAX    TABLE, PCR
```

Since program counter relative is a type of indexing, an additional level of indirection is available.

```
LDA     [CAT,PCR]
LDU     [DOG,PCR]
```

S6809E Instruction Set

The instruction set of the S6809E is similar to that of the S6800 and is upward compatible at the source code level. The number of opcodes has been reduced from 72 to 59, but because of the expanded architecture and additional addressing modes, the number of available opcodes (with different addressing modes) has risen from 197 to 1464.

Some of the new instructions and addressing modes are described in detail below:

PSHU/PSHS. The push instructions have the capability of pushing onto either the hardware stack (S) or user stack (U) any or all of the MPU registers with a single instruction.

PULU/PULS. The pull instructions have the same capability of the push instruction, in reverse order. The byte immediately following the push or pull opcode determines which register or registers are to be pushed or pulled. The actual PUSH/PULL sequence is fixed; each bit defines a unique register to push or pull as shown in Figure 17.

TFR/EXG. Within the S6809E, any register may be transferred to or exchanged with another of like-size, i.e., 8-bit to 8-bit or 16-bit to 16-bit. Bits 4-7 of postbyte define the source register, while bits 0-3 represent the destination register. These are denoted as follows:

0000 — D	0101 — PC
0001 — X	1000 — A
0010 — Y	1001 — B
0011 — U	1010 — CC
0100 — S	1011 — DP

Note: All other combinations are undefined and INVALID.

Load Effective Address. The LEA works by calculating the effective address used in an indexed instruction and stores that address value, rather than the data at that address, in a pointer register. This makes all the features of the internal addressing hardware available to the programmer. Some of the implications of this instruction are illustrated in the following table of examples:

The LEA Instruction also allows the user to access data in a position independent manner. For example:

```
        LEAX  MSG1, PCR
        LBSR  PDATA (Print message routine)
MSG1    FCC   'MESSAGE'
```

Figure 16. Push/Pull Postbyte

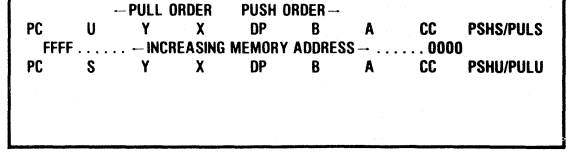


Table 3. LEA Examples

Instruction	Operation	Comment
LEAX 10, X	X+10 →X	Adds 5-bit constant 10 to X
LEAX 500, X	X+500 →X	Adds 6-bit constant 500 to X
LEAY A, Y	Y+A →Y	Adds 8-bit accumulator to Y
LEAY D, Y	Y+D →Y	Adds 16-bit D accumulator to Y
LEAU −10, U	U−10 →U	Subtracts 10 from U
LEAS −10, S	S−10 →S	Used to reserve area on stack
LEAS 10, S	S+10 →S	Used to 'clean up' stack
LEAX 5, S	S+5 →X	Transfers as well as adds

This sample program prints "message." By writing MSG1,PCR, the assembler computes the distance between the present address and MSG1. This result is placed as a constant into the LEAX instruction which will be indexed from the PC value at the time of execution. No matter where the code is located, when it is executed, the computed offset from the PC will put the absolute address of MSG1 into the X pointer register. This code is totally position independent.

MUL. Multiplies the unsigned binary numbers in the A and B accumulator and places the unsigned result into the 16-bit D accumulator. This unsigned multiply also allows multiple-precision multiplications.

Long and Short Relative Branches. The S6809E has the capability of program counter relative branching throughout the entire memory map. In this mode, if the branch is to be taken, the 8 or 16-bit signed offset is added to the value of the program counter to be used as the effective address. This allows the program to branch anywhere in the 64K memory map. Position independent code can be easily generated through the use of relative branching. Both short (8-bit) and long (16-bit) branches are available.

Sync. After encountering a Sync operation, the MPU enters a Sync State, stops processing instructions and waits for an interrupt. If the pending interrupt is nonmaskable ($\overline{NMI}$) or maskable ($\overline{FIRQ}$, $\overline{IRQ}$) with its mask bit (F or I) clear, the processor will clear the Sync state and perform the normal interrupt stacking and service routine. Since $\overline{FIRQ}$ and $\overline{IRQ}$ are not edge-triggered, a low level with a minimum duration of three cycles is required to assure that the interrupt will be taken. If the pending interrupt is maskable ($\overline{FIRQ}$, $\overline{IRQ}$) with its mask bit (F or I) set, the processor will clear the Sync state and continue processing in sequence. Figure 18 depicts Sync timing.

Software Interrupts. A Software Interrupt is an instruction which will cause an interrupt, and its associated vector fetch. These Software Interrupts are useful in operating system calls, software debugging, trace operations, memory mapping, and software development systems. Three levels of SWI are available on this S6809, and are prioritized in the following order: SWI, SWI2, SWI3.

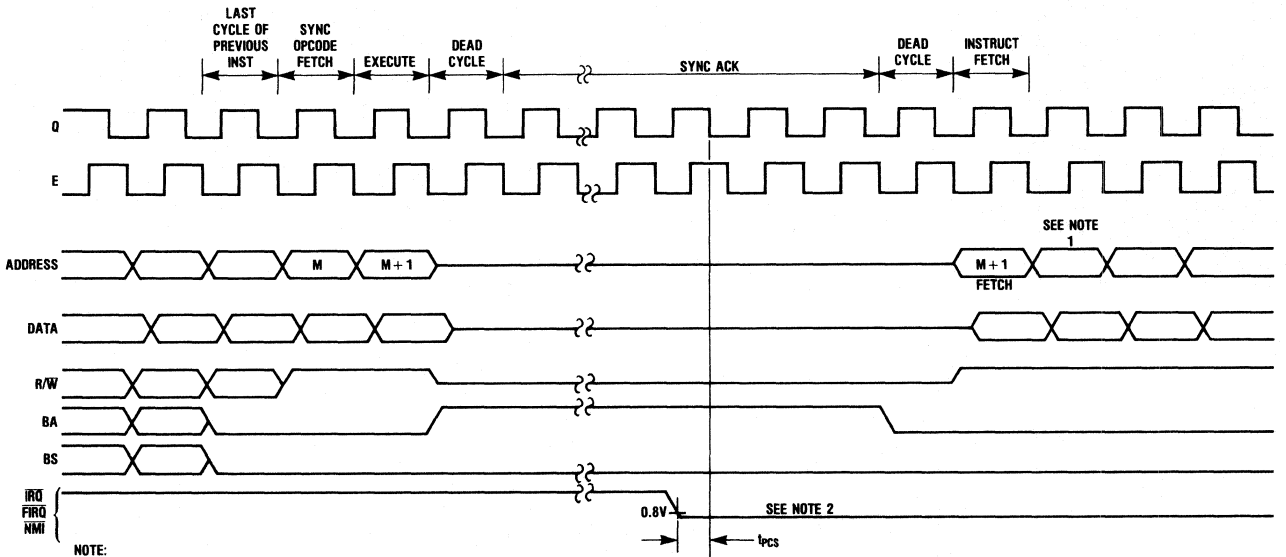
16-Bit Operations. The S6809E has the capability of processing 16-bit data. These instructions include loads, stores, compares, adds, subtracts, transfers, exchanges, pushes and pulls.

Cycle-by-Cycle Operation. The address bus cycle-by-cycle performance chart illustrates the memory-access sequence corresponding to each possible instruction and addressing mode in the S6809E. Each instruction begins with an opcode fetch. While that opcode is being internally decoded, the next program byte is always fetched. (Most instructions will use the next byte, so this technique considerably speeds throughput). Next, the operation of each opcode will follow the flowchart. $\overline{VMA}$ is an indication of $FFFF_{16}$ on the address bus, R/$\overline{W}$=1 and BS=0. The following examples illustrate the use of the chart; see Figure 19.

LBSR (Branch taken)
Cycle #
1 opcode Fetch
2 opcode +
3 opcode +
4 $\overline{VMA}$
5 $\overline{VMA}$
6 ADDR
7 $\overline{VMA}$
8 STACK (write)
9 STACK (write)

DEC (Extended)
1 opcode Fetch
2 opcode +
3 opcode +
4 $\overline{VMA}$
5 ADDR (read)
6 $\overline{VMA}$
7 ADDR (write)

Figure 17. SYNC Timing



NOTE:

1. IF THE MASK BIT IS SET WHEN THE INTERRUPT IS REQUESTED PROCESSING WILL CONTINUE WITH INSTRUCTION EXECUTION FETCHED FROM PREVIOUS STEP. HOWEVER, IF AN $\overline{NMI}$ OR AN UNMASKED $\overline{FIRQ}$ OR $\overline{IRQ}$ CAUSED INTERRUPT, THE ADDRESS PLACED ON BUS FROM PREVIOUS CYCLE (M + 1) REMAINS ON BUS AND PROCESSING CONTINUES WITH THIS CYCLE AS (m + 1) OR (n + 1) OF INTERRUPT TIMING.
2. IF MASK BITS ARE CLEAR $\overline{IRQ}$ & $\overline{FIRQ}$ MUST BE HELD LOW FOR THREE CYCLES TO GUARANTEE INTERRUPT TO BE TAKEN, ALTHOUGH ONLY ONE CYCLE IS NECESSARY TO BRING THE PROCESSOR OUT OF SYNC.

S6809E Instruction Set Tables

The instructions of the S6809E have been broken down into six different categories. They are as follows:

8-Bit Operation (Table 4)
16-Bit Operation (Table 5)
Index Register/Stack Pointer Instructions (Table 6)
Relative Branches (Long and Short)(Table 7)
Miscellaneous Instructions (Table 8)
Hexadecimal Value Instructions (Table 9)

Table 4. 8-Bit Accumulator and Memory Instructions

Mnemonic(s)	Operation
ADCA, ADCB	Add memory to accumulator with carry
ADDA, ADDB	Add memory to accumulator
ANDA, ANDB	And memory with accumulator
ASL, ASLA, ASLB	Arithmetic shift of accumulator or memory left
ASR, ASRA, ASRB	Arithmetic shift of accumulator or memory right
BITA, BITB	Bit test memory with accumulator
CLR, CLRA, CLRB	Clear accumulator or memory location
CMPA, CMPB	Compare memory from accumulator
COM, COMA, COMB	Complement accumulator or memory location
DAA	Decimal adjust A-accumulator
DEC, DECA, DECB	Decrement accumulator or memory location
EORA, EORB	Exclusive OR memory with accumulator
EXG R1, R2	Exchange R1 with R2 (R1, R2=A, B, CC, DP)
INC, INCA, INCB	Increment accumulator or memory location
LDA, LDB	Load accumulator from memory
LSL, LSLA, LSLB	Logical shift left accumulator or memory location
LSR, LSRA, LSRB	Logical shift right accumulator or memory location
MUL	Unsigned multiply (A x B→D)
NEG, NEGA, NEGB	Negate accumulator or memory
ORA, ORB	OR memory with accumulator
ROL, ROLA, ROLB	Rotate accumulator or memory left
ROR, RORA, RORB	Rotate accumulator or memory right
SBCA, SBCB	Subtract memory from accumulator with borrow
STA, STB	Store accumulator to memory
SUBA, SUBB	Subtract memory from accumulator
TST, TSTA, TSTB	Test accumulator or memory location
TFR, R1, R2	Transfer R1 to R2 (R1, R2=A, B, CC, DP)

NOTE: A, B, CC, or DP may be pushed to (pulled from) either stack with PSHS, PSHU, (PULS, PULU) instructions.

Table 5. 16-Bit Accumulator and Memory Instructions

Mnemonic(s)	Operation
ADDD	Add memory to D accumulator
CMPD	Compare memory from D accumulator
EXG D, R	Exchange D with X, Y, S, U or PC
LDD	Load D accumulator from memory
SEX	Sign Extend B accumulator into A accumulator
STD	Store D accumulator to memory
SUBD	Subtract memory from D accumulator
TFR D, R	Transfer D to X, Y, S, U or PC
TFR R, D'	Transfer X, Y, S, U or PC to D

Table 6. Index Register/Stack Pointer Instructions

Mnemonic(s)	Operation
CMPS, CMPU	Compare memory from stack pointer
CMPX, CMPY	Compare memory from index register
EXG R1, R2	Exchange D, X, Y, S, U or PC with D, X, Y, S, U or PC
LEAS, LEAU	Load effective address into stack pointer
LEAX, LEAY	Load effective address into index register
LDS, LDU	Load stack pointer from memory
LDX, LDY	Load index register from memory
PSHS	Push any register(s) onto hardware stack (except S)
PSHU	Push any register(s) onto user stack (except U)
PULS	Pull any register(s) from hardware stack (except S)
PULU	Pull any register(s) from hardware stack (except U)
STS, STU	Store stack pointer to memory
STX, STY	Store index register to memory
TFR R1, R2	Transfer D, X, Y, S, U or PC to D, X, Y, S, U or PC
ABX	Add B accumulator to X (unsigned)

Table 7. Branch Instructions

Mnemonic(s)	Operation
BCC, LBCC	Branch if carry clear
BCS, LBCS	Branch if carry set
BEQ, LBEQ	Branch is equal
BGE, LBGE	Branch if greater than or equal (signed)
BGT, LBGT	Branch if greater (signed)
BHI, LBHI	Branch if higher (unsigned)
BHS, LBHS	Branch is higher or same (unsigned)
BLE, LBLE	Branch if less than or equal (signed)
BLO, LBLO	Branch if lower (unsigned)
BLS, LBLS	Branch if lower or same (unsigned)
BLT, LBLT	Branch if less than (signed)
BMI, LBMI	Branch if minus
BNE, LBNE	Branch if not equal
BPL, LBPL	Branch is plus
BRA, LBRA	Branch always
BRN, LBRN	Branch never
BSR, LBSR	Branch to subroutine
BVC, LBVC	Branch if overflow clear
BVS, LBVS	Branch if overflow set

Table 8. Miscellaneous Instructions

Mnemonic(s)	Operation
ANDCC	AND condition code register
CWAI	AND conditon code register, then wait for interrupt
NOP	No operation
ORCC	OR condition code register
JMP	Jump
JSR	Jump to subroutine
RTI	Return from interrupt
RTS	Return from subroutine
SWI, SWI2, SWI3	Software interrupt (absolute indirect)
SYNC	Synchronize with interrupt line

AMERICAN MICROSYSTEMS, INC.

S1602

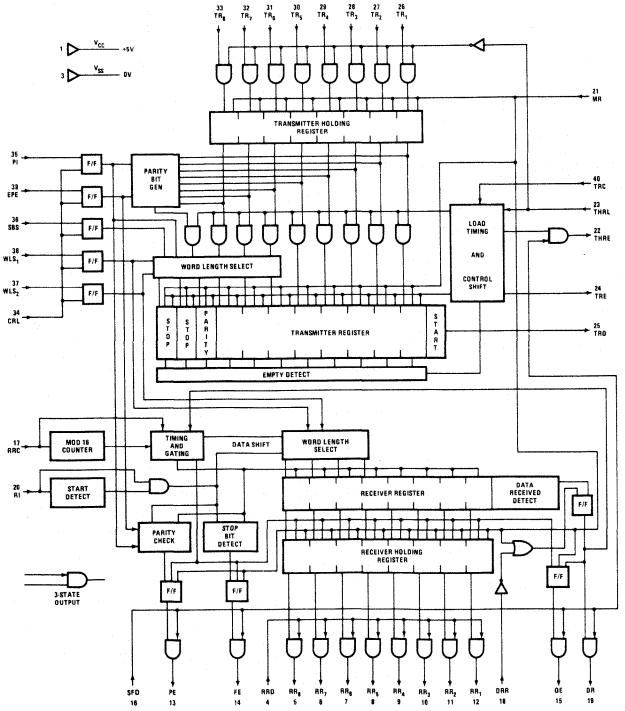
UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER

S6800

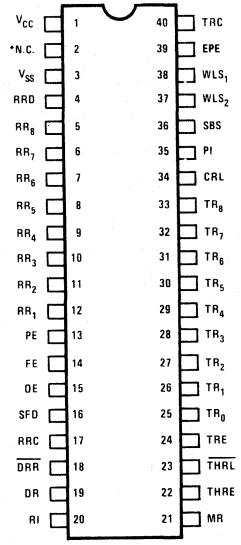
Features

- ☐ Full or Half Duplex Operation — Can Receive and Transmit Simultaneously at Different Baud Rates.
- ☐ Completely Programmable — Data Word Length, Number of Stop Bits, Parity.
- ☐ Start Bit Generated Automatically
- ☐ Data and Clock Synchronization Performed Automatically
- ☐ Double Buffered—Eliminates Timing Difficulties
- ☐ Completely Static Circuitry
- ☐ Fully TTL Compatible.
- ☐ Three-state Output Capability
- ☐ Single Power Supply: +5V
- ☐ Standard 40-Pin Dual-in-Line Package
- ☐ Plug In Compatible with Western Digital TR1602A, TR1863, Fujitsu 8868A

Block Diagram



Pin Configuration



General Description

The AMI S1602 is a programmable Universal Asynchronous Receiver/Transmitter (UART) fabricated with N-Channel silicon gate MOS technology. All control pins, input pins and output pins are TTL compatible, and a single +5 volt power supply is used. The UART interfaces asynchronous serial data from terminals or other peripherals, to parallel data for a microprocessor, computer, or other terminal. Parallel data is converted by the transmitter section of the UART into a serial word consisting of the data as well as start, parity, and stop bit(s). Serial data is converted by the receiver section of the UART into parallel data. The receiver section verifies correct code transmission by parity checking and receipt of a valid stop bit. The UART can be programmed to accept word lengths of 5, 6, 7, or 8 bits. Even or odd parity can be set. Parity generation checking can be inhibited. The number of stop bits can be programmed for one, two, or one and one-half when transmitting a 5-bit code.

Absolute Maximum Ratings*

V_{CC} Pin Potential to V_{SS} Pin	−0.3V to +7.0V
Input Voltage	−0.3V to +7.0V
Operating Temperature	0°C to +70°C
Storage Temperature	−55°C to +150°C

**Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheets. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Capacitance: $T_A = 25°$; f = 1MHz; $V_{IN} = 0V$

Symbol	Parameter	Typ.	Max.	Unit
C_{IN}	Input Capacitance for all Inputs	10	—	pF

Guaranteed Operating Conditions (Referenced to V_{SS})

Symbol	Parameter	Operating Temperature	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	0°C to +70°C	4.75	5.0	5.25	V
V_{SS}			0.0	0.0	0.0	V
V_{IH}	Logic Input High Voltage	0°C to +70°C	2.2	—	V_{CC}	V
V_{IL}	Logic Input Low Voltage	0°C to +70°C	−0.3	—	+0.8	V

D.C. Characteristics (Guaranteed Operating Ranges Unless Otherwise Noted.)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{IL}	Input Leakage Current ($V_{IN} = 0$ to 5.25V, $V_{CC} = 5.25V$)	—	—	1.4	mA
I_{LZ}	Output Leakage Current for 3-State ($V_{OUT} = 0V$ to V_{CC}, SFD = RRD = V_{IH})	−20	—	+20	μA
V_{OL}	Output Low Voltage ($I_{OL} = 1.8mA$)	—	—	0.4	V
V_{OH}	Output High Voltage ($I_{OL} = -200\mu A$)	2.4	—	—	V
I_{CC}	V_{CC} Supply Current	—	70	—	mA

A.C. Characteristics (Guaranteed Operating Ranges Unless Otherwise Noted.)

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_C	Clock Frequency for RRC and TRC (Duty Cycle = 50%)	DC	—	800	kHz
t_{PWC}	CRL Pulse Width, High	200	—	—	ns
t_{PWT}	THRL Pulse Width, Low	180	—	—	ns
t_{PWR}	DRR Pulse Width, Low	180	—	—	ns
t_{PWM}	MR Pulse Width, High	150	—	—	ns
t_C	Coincidence Time (Figure 3 and Figure 8)	180	—	—	ns
t_{HOLD}	Hold Time (Figure 3 and Figure 8)	20	—	—	ns
t_{SET}	Setup Time (Figure 3 and Figure 8)	0	—	—	ns
t_{PD0}	Propagation Delay Time High to Low, Output (C_L = 130pF + 1TTL)	—	—	350	ns
t_{PD1}	Propagation Delay Time Low to High, Output (C_L = 130pF + 1TTL)	—	—	350	ns

Pin Description

Pin	Label	Function
1	V_{CC}	**Power Supply** — normally at +5V.
2	N.C.	**No connection.** On the S1602 this is an unconnected pin. On the TR1602A this is a −12V supply. −12V is not needed on the S1602 and thus the N.C. pin allows the S1602 to be compatible with the TR1602A.
3	V_{SS}	This is normally at 0V or ground.
4	RRD	**Receive Register Disconnect.** A high logic level, V_{IH}, on this pin disconnects the Receiver Holding Register outputs from the data outputs RR_8 — RR_1 on pin 5 — 12.
5 — 12	RR_8 — RR_1	**Receiver Holding Register Data.** These are the parallel outputs from the Receiver Holding Register if the RRD input is low (V_{IL}). Data is (LSB) right justified for character formats of less than eight bits, with RR_1 being the least significant bit. Unused MSBs are forced to a low logic output level, V_{OL}.
13	PE	**Parity Error.** This output pin goes to a high level if the received parity does not agree with that programmed by the Even Parity Enable input (pin 39). This output is updated as each character is transferred to the Receiver Holding Register. The Status Flag Disconnect input (pin 16) allows additional PE lines to be tied together by providing an output disconnect capability.
14	FE	**Framing Error.** This output pin goes high if the received character has no valid stop bit. Each time a character is transferred to the Receiver Holding Register, this output is updated. The Status Flag Disconnect input (pin 16) allows additional FE lines to be tied together by providing an output disconnect capability.
15	OE	**Overrun Error.** This output pin goes high if the Data Received Flag (pin 19) did not get reset before the next character was transferred to the Receive Holding Register. The Status Flag Disconnect input (pin 16) allows additional OE lines to be tied together providing an output disconnect capability.
16	SFD	**Status Flag Disconnect.** When this input is high, PE, FE, OE, DR and THRE outputs are forced to high impedance Three State allowing bus sharing capability.

Pin Description (Continued)

Pin	Label	Function
17	RRC	**Receive Register Clock.** This clock input is 16x the desired receiver shift rate.
18	$\overline{DRR}$	**Data Received Reset.** A low level input, V_{IL}, clears the Data Received (DR) line.
19	DR	**Data Received.** When a complete character has been received and transferred to the Receiver Holding Register, this output goes to the high level, V_{OH}.
20	RI	**Receiver Input.** Serial input data enters on this line. It is transfered to the Receiver Register as determined by the character length, parity and number of stop bits. When data is not being received, this input must remain high, V_{IH}.
21	MR	**Master Reset.** A high level pulse, V_{IH}, on this input clears the internal logic. The transmitter and Receive Registers, Receiver Holding Registers, FE, OE, PE, DRR are reset. In addition, the serial output line is set to a high level, V_{OH}.
22	THRE	**Transmitter Holding Register Empty.** This output will go high when the Transmitter Holding Register completes transfer of its contents to the Transmitter Register. The high level indicates a new character may be loaded into the Transmitter Holding Register.
23	$\overline{THRL}$	**Transmitter Holding Register Load.** When a low level, V_{IL}, is applied to this input, a character is loaded into the Transmitter Holding Register. The character is transferred to the Transmitter Register on a low to high level, V_{IH}, transition as long as the Transmitter Register is not currently in the process of transmitting a character. If a character is being transmitted, the transfer is delayed until the transmission is completed. The new character is then transferred simultaneously with the start of the serial transmission of the new character.
24	TRE	**Transmitter Register Empty.** Goes high when the Transmitter Register has completed the serial transmission of a full character including the required number of stop bits. A high will be maintained until the start of transmission of the next character.
25	TRO	**Transmitter Register Output.** Transmits the Transmitter Register contents (Start bit, Data bits, Parity bit and Stop bit(s)) serially. Remains high, V_{OH}, when no data is being transmitted. Therefore, start of transmission is determined by transition of the Start bit from high to low level voltage, V_{OL}.
26—33	$TR_1 - TR_8$	**Transmitter Register Data Inputs.** The THRL strobe loads the character on these lines into the Transmitter Holding Register. If WLS_1 and WLS_2 have selected a character of less than 8 bits, the character is right justified to the least significant bit, TR_1 with the excess bits not used. A high input level, V_{IH}, will cause a high output level, V_{OH}, to be transmitted.
34	CRL	**Control Register Load.** The control bits, (WLS_1, WLS_2, EPE, PI, SBS), are loaded into the Control Register when the input is high. This input may be either strobed or hard wired to the high level.
35	PI	**Parity Inhibit.** Parity generation and verification circuitry are inhibited when this input is high. The PE output will be held low as well. When in the inhibit condition the Stop bit(s) will follow the last data bit on transmission.
36	SBS	**Stop Bit(s) Select.** A high level will select two Stop bits, and a low level selects one Stop bit. If 5-bit words are selected, a high level will generate one and one-half Stop bits.

Pin Description (Continued)

Pin	Label	Function
37, 38	WLS_2, WLS_1	**Word Length Select.** The state of these two (2) inputs determines the character length (exclusive of parity) as follows:

WLS_2	WLS_1	WORD LENGTH
LOW	LOW	5 bits
LOW	HIGH	6 bits
HIGH	LOW	7 bits
HIGH	HIGH	8 bits

39	EPE	**Even Parity Enable.** A high voltage level, V_{IH}, on this input will select even parity, while a low voltage level, V_{IL}, selects odd parity.
40	TRC	**Transmitter Register Clock.** The frequency of this clock input should be 16 times the desired baud rate.

Figure 1. Receiver Operating Timing

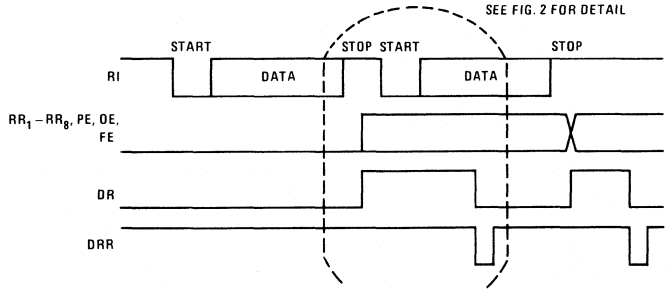


Figure 2. Timing for Status Flags, RR_1 thru RR_8 and DR

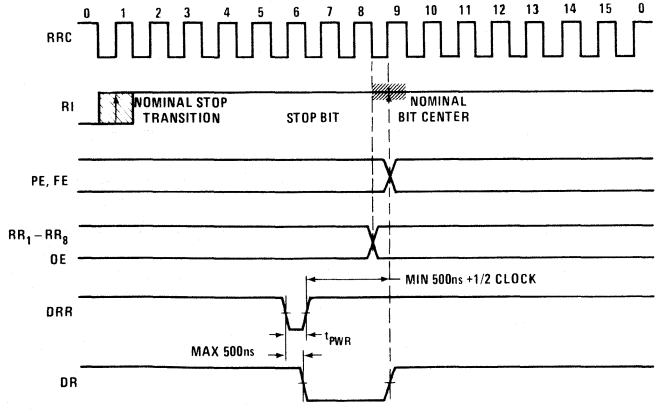


Figure 3. Transmitter Operating Timing

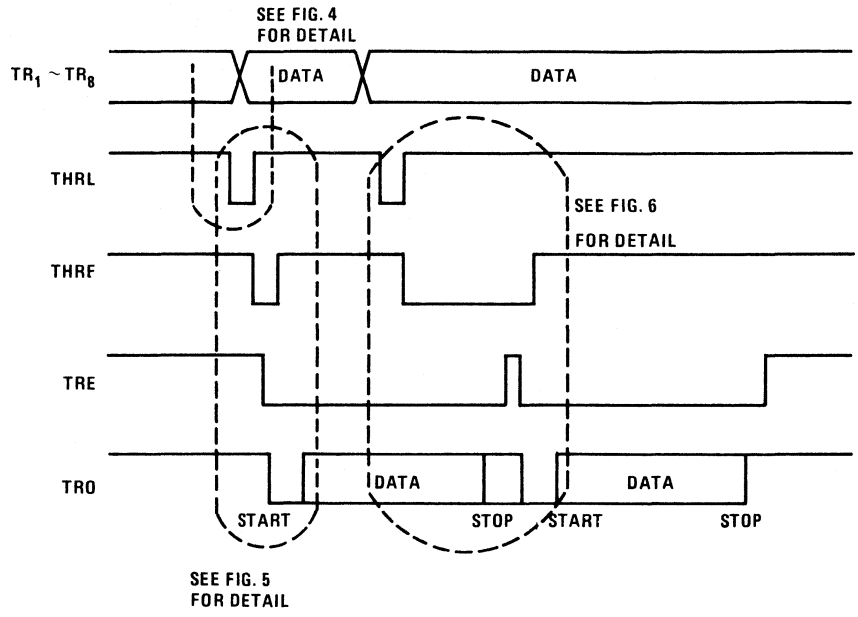


Figure 4. Data Input Load Cycle

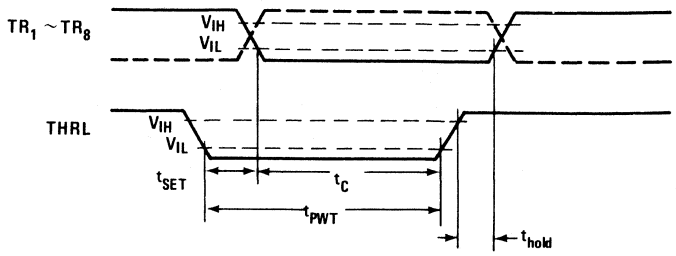
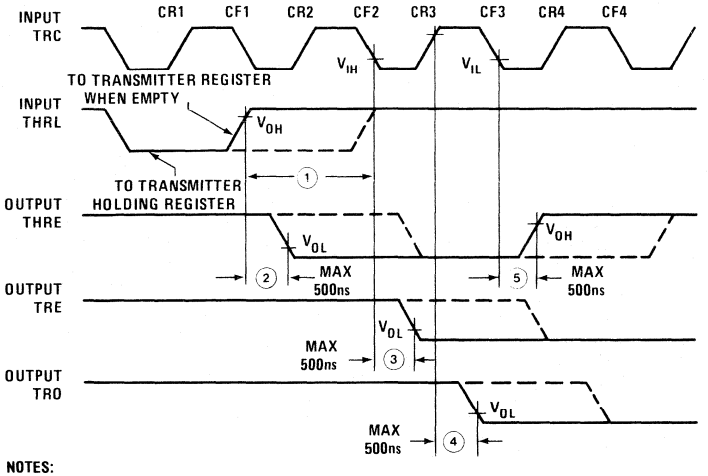


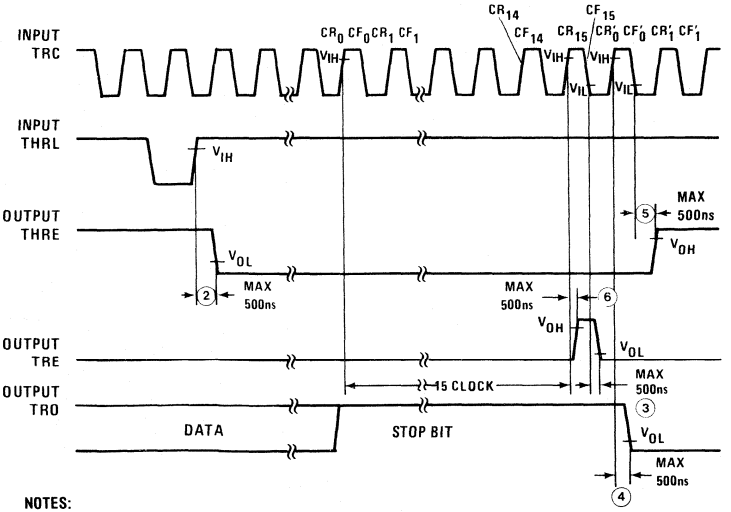
Figure 5. Transmitter Output Timing (1)



NOTES:

1. When the positive transition of THRL is 500ns or more before the falling edge of TRC (CF2 in the figure), TRE is enabled at CF2. But, when 500ns>①>0ns, TRE is invalid between CF2 and CF3.
2. THRE goes to low during 500ns Max. from the positive transition of THRL.
3. TRE goes to low during 500ns Max. from the first falling edge of TRC after THRE goes to low with TRE high.
4. TRO goes to low (START BIT) during 500ns Max. from the first rising edge of TRC after TRE goes to low.
5. THRE goes to high during 500ns Max. from the falling edge of TRC after START BIT is enabled.

Figure 6. Transmitter Output Timing (2)



NOTES:

2-5, refer to Figure 5.

6. TRANSMITTER REGISTER EMPTY goes to high during 500ns Max. from the 15th rising edge of TRC after STOP BIT is enables.

Figure 7. Input After Master Reset

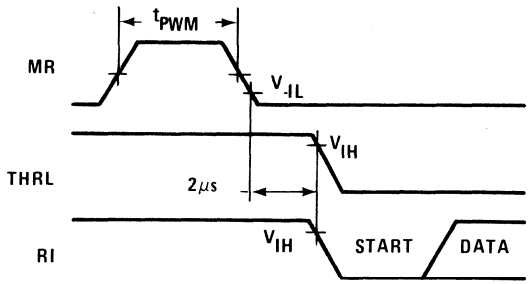


Figure 8. Control Register Load Cycle

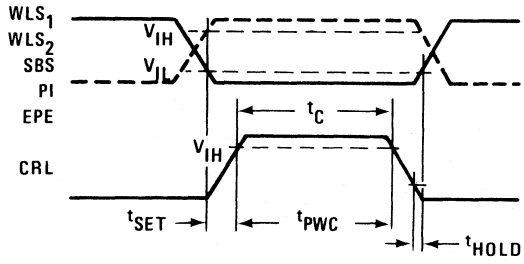


Figure 9. Status Flag Output

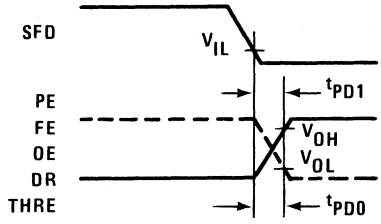
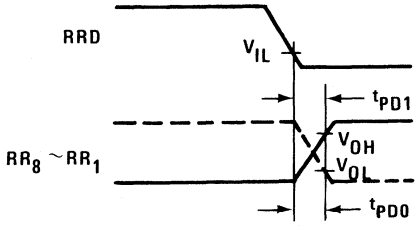


Figure 10. Data Output



AMERICAN MICROSYSTEMS, INC.

S2350

Universal Synchronous Receiver/Transmitter

Features

- ☐ **500kHz Data Rates**
- ☐ **Internal Sync Detection**
- ☐ **Fill Character Register**
- ☐ **Double Buffered Input/Output**
- ☐ **Bus Oriented Outputs**
- ☐ **5-8 Bit Characters**
- ☐ **Odd/Even or No Parity**
- ☐ **Error Status Flags**
- ☐ **Single Power Supply (+5V)**
- ☐ **Input/Output TTL-Compatible**

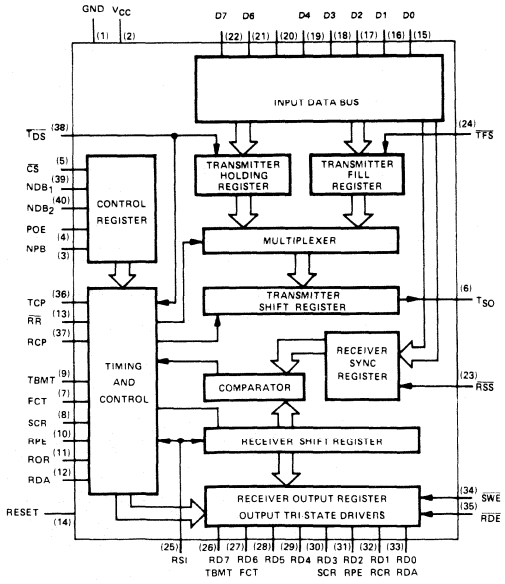
General Description

The S2350 Universal Synchronous Receiver Transmitter (USRT) is a single chip MOS/LSI device that totally replaces the serial-to-parallel and parallel-to-serial conversion logic required to interface a word parallel controller or data terminal to a bit-serial, synchronous communication network.

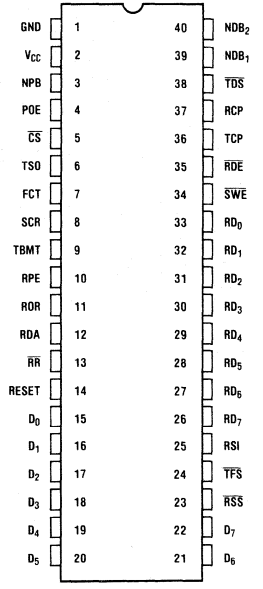
The USRT consists of separate receiver and transmitter sections with independent clocks, data lines and status. Common with the transmitter and receiver are word length and parity mode. Data is transmitted and received in a NRZ format at a rate equal to the respective input clock frequency.

S6800

Block Diagram



Pin Configuration



Data messages are transmitted as a contiguous character stream, bit synchronous with respect to a clock and character synchronous with respect to framing or "sync" characters initializing each message. The USRT receiver compares the contents of the internal Receiver Sync Register with the incoming data stream in a bit transparent mode. When a compare is made, the receiver becomes character synchronous formatting a 5, 6, 7, or 8-bit character for output each character time. The receiver has an output buffer register allowing a full character time to transfer the data out. The receiver status outputs indicate received data available (RDA), receiver overrun (ROR), receive parity error (RPE) and sync character received (SCR). Status bits are available on individual output lines and can also be multiplexed onto the output data lines for bus organized systems. The data lines have tri-state outputs.

The USRT transmitter outputs 5, 6, 7, or 8-bit characters with correct parity at the transmitter serial output (TSO). The transmitter is buffered to allow a full character time to respond to a transmitter buffer empty (TBMT) request for data. Data is transmitted in a NRZ format changing on the positive transition of the transmitter clock (TCP). The character transmitter fill register is inserted into the data message if a data character is not loaded into the transmitter after a TBMT request.

Typical Applications

- ☐ Computer Peripherals
- ☐ Communication Concentrators
- ☐ Integrated Modems
- ☐ High Speed Terminals
- ☐ Time Division Multiplexing
- ☐ Industrial Data Transmission

Absolute Maximum Ratings

Ambient Temperature Under Bias	0°C to +70°C
Storage Temperature	−65°C to +150°C
Positive Voltage on any Pin with Respect to GROUND	+7V
Negative Voltage on any Pin with Respect to GROUND	−0.5V
Power Dissipation	0.75W

D.C. (Static) Electrical Characteristics* (V_{CC} = 5.0V ± 5%; T_A = 0°C to +70°C unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{IL}	Input Low Voltage	−0.5		+0.8	V	
I_{IL}	Input Leakage Current			10	μA	V_{IN} = O_{TO} V_{CC} V
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −100μA
V_{OL}	Output Low Voltage			+0.4	V	I_{OL} = 1.6mA
C_{IN}	Input Capacitance			10	pF	V_{IN} = 0V; f = 1.0MHz
C_{OUT}	Output Capacitance			12	pF	V_{IN} = 0V; f = 1.0MHz
I_{CC}	V_{CC} Supply Current			100	mA	No Load; V_{CC} = 5.25V

*Electrical characteristics included in this advanced product description are objective specifications and may be subject to change.

A.C. (Dynamic) Electrical Characteristics* (V_{CC} = 5.0V ± 5%; T_A = 0°C to +70°C unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
TCP, RCP	Clock Frequency	DC		500	kHz	
Input Pulse Widths						
P_{TCP}	Transmit Clock	900			nsec	CL = 20pF
P_{RCP}	Receive Clock	900			nsec	1TTL Load
P_{RST}	Reset	500			nsec	
P_{TDS}	Transmit Data Strobe	200			nsec	
P_{TFS}	Transmit Fill Strobe	200			nsec	
P_{RSS}	Receive Sync Strobe	200			nsec	
P_{CS}	Control Strobe	200			nsec	
P_{RDE}	Receive Data Enable	400			nsec	Note 1
P_{SWE}	Status Word Enable	400			nsec	Note 1
P_{RR}	Receiver Restart	500			nsec	
Switching Characteristics						
T_{TSO}	Delay, TCP Clock to Serial Data Out			700	nsec	
T_{TBMT}	Delay, TCP Clock to TBMT Output			1.4	μsec	
T_{TBMT}	Delay, TDS to TBMT			700	nsec	
T_{STS}	Delay, SWE to Status Reset			700	nsec	
T_{RDO}	Delay, SWE, RDE to Data Outputs			400	nsec	1TTL Load
T_{HRDO}	Hold Time SWE, RDE to Off State			400	nsec	C_L = 130pF
T_{DTS}	Data Set Up Time TDS, TFS, RSS, CS	0			nsec	
T_{DTH}	Data Hold Time TDS	700			nsec	
T_{DTI}	Data Hold Time TFS, RSS	200			nsec	
T_{CNS}	Control Set Up Time NDB1, NDB2, NPB, POE	0			nsec	
T_{CNH}	Control Hold Time NDB1, NDB2, NPB, POE	200			nsec	
T_{RDA}	Delay RDE to RDA Output	700			nsec	

NOTE 1: Required to reset status and flags.

Figure 1. Timing Waveform

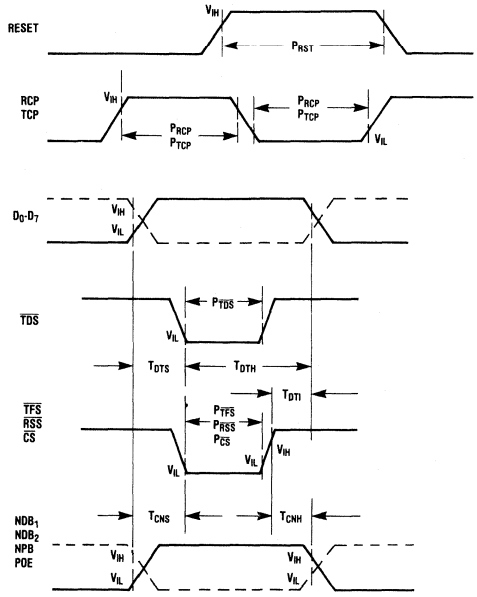


Figure 2. Timing Waveform

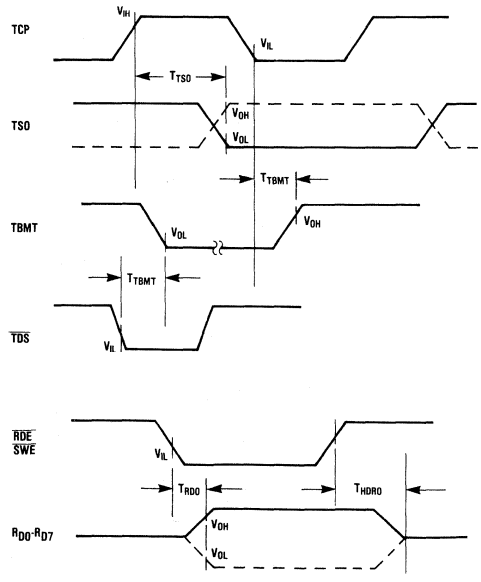
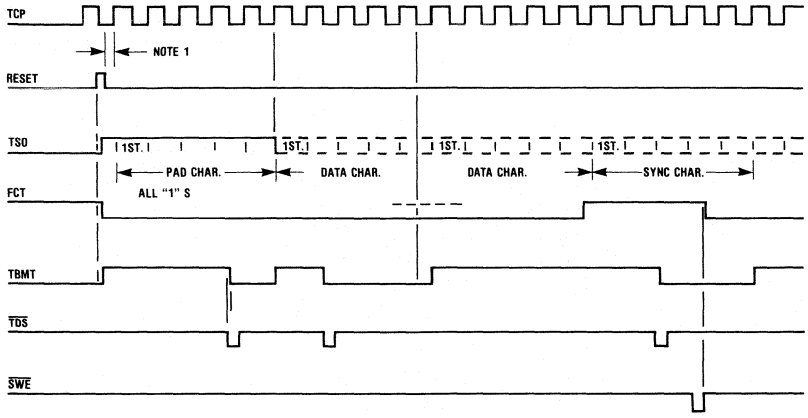
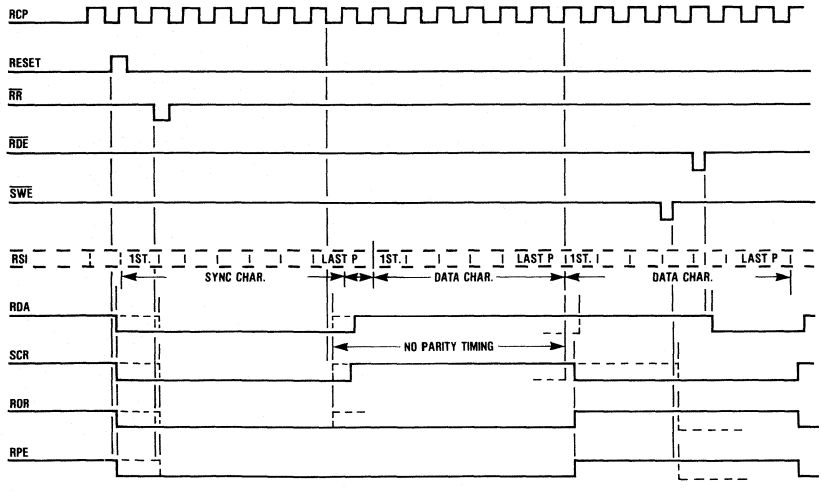


Figure 3. Transmitter Timing Diagram



NOTE 1 DATA TRANSMISSION WILL START ON THE FIRST LOW TO HIGH TRANSITION OF TCP AFTER RESET IS LOW. THE INITIAL RESET PULSE SHOULD NOT OCCUR UNTIL 100 MICROSECONDS AFTER POWER IS APPLIED.

Figure 4. Receiver Timing Diagram



Pin Definitions

Pin	Label	Function
(1)	GND	Ground
(2)	V_{CC}	+ 5 Volts ± 5%
(14)	RESET	MASTER RESET. A V_{IH} initializes both the receiver and transmitter. The Transmitter Shift Register is set to output a character of all logic 1's. FCT is reset to V_{OL} and TBMT set to V_{OH} indicating the Transmitter Holding Register is empty. The receiver status is initialized to a V_{OL} on RPE, SCR, and RDA. The sync character detect logic is inhibited until a RR pulse is received.
(15 – 22)	D0 – D7	DATA INPUTS. Data on the eight data lines are loaded into the Transmitter Holding Register by $\overline{TDS}$, the Transmitter Fill Register by $\overline{TFS}$, and the Receiver Sync Register by $\overline{RSS}$. The character is right justified with the LSB at D0. For word lengths less than 8 bits, the unused inputs are ignored. Data transmission is LSB first.
(38)	$\overline{TDS}$	TRANSMIT DATA STROBE. A V_{IL} loads data on D0-D7 into the Transmitter Holding Register and resets TBMT to a V_{OL}.
(24)	$\overline{TFS}$	TRANSMIT FILL STROBE. A V_{IL} loads data on D0-D7 into the Transmitter Fill Register. The character in the Transmitter Fill Register is transmitted whenever a new character is not loaded in the allotted time.
(23)	$\overline{RSS}$	RECEIVER SYNC STROBE. A V_{IL} loads data on D0-D7 into the Receiver Sync Register. SCR is set to V_{OH} whenever data in the Receiver Shift Register compares with the character in the Receiver Sync Register.
(9)	TBMT	TRANSMIT BUFFER EMPTY. A V_{OH} indicates the data in the Transmitter Holding Register has been transferred to the Transmitter Shift Register and new data may be loaded. TBMT is reset to V_{OL} by a V_{IL} on $\overline{TDS}$. A V_{IH} on RESET sets TBMT to a V_{OH}. TBMT is also multiplexed onto the RD7 output (26) when $\overline{SWE}$ is at V_{IL} and $\overline{RDE}$ is at V_{IH}.
(6)	TSO	TRANSMITTER SERIAL OUTPUT. Data entered on D0-D7 are transmitted serially, least significant bit first, on TSO at a rate equal to the Transmit Clock frequency, TCP. Source of the data to the transmitter shift register is the Transmitter Holding Register or Transmitter Fill Register.
(36)	TCP	TRANSMIT CLOCK. Data is transmitted on TSO at the frequency of the TCP input in a NRZ format. A new data bit is started on each negative to positive transition (V_{IL} to V_{IH}) of TCP.
(26 – 33)	RD7 – RD0	RECEIVED DATA OUTPUTS RD0-RD7 contain data from the Receiver Output Register or selective status conditions depending on the state of $\overline{SWE}$ and $\overline{RDE}$ per the following table:

(34) $\overline{SWE}$	(35) $\overline{RDE}$	(33) RD0	(32) RD1	(31) RD2	(30) RD3	(39) RD4	(28) RD5	(27) RD6	(26) RD7
V_{IL}	V_{IL}	X	X	X	X	X	X	X	X
V_{IL}	V_{IH}	RDA	ROR	RPE	SCR	V_{OL}	V_{OL}	FCT	TBMT
V_{IH}	V_{IL}	DB0	BD1	DB2	DB3	DB4	DB5	DB6	DB7
V_{IH}	V_{IH}	X	X	X	X	X	X	X	X

X – Output is in the OFF or Tri-State condition
DB0 – LSB of Receiver Output Register
DB7 – MSB of Receiver Output Register
The two unused outputs are held at V_{OL} in the output status condition.

Pin Definitions (continued)

Pin	Label	Function
(35)	$\overline{RDE}$	RECEIVE DATA ENABLE. A V_{IL} enables the data in the Receiver Output Register onto the output data lines RD0 – RD7. The trailing edge (V_{IL} to V_{III} transition) of $\overline{RDE}$ resets RDA to the V_{OL} condition.
(7)	FCT	FILL CHARACTER TRANSMITTED. A V_{OH} on FCT indicates data from the Transmitter Fill Register has been transferred to the Transmitter Shift Register. FCT is reset to V_{OL} when data is transferred from the Transmitter Holding Register to the Transmitter Shift Register, or on the trailing edge (V_{IL} to V_{IH}) of the $\overline{SWE}$ pulse, or when RESET is V_{IH}. FCT is multiplexed onto the RD6 output (27) when $\overline{SWE}$ is at V_{IL} and $\overline{RDE}$ is at V_{IH}.
(25)	RSI	RECEIVER SERIAL INPUT. Serial data is clocked into the Receiver Shift Register, least significant bit first, on RSI at a rate equal to the Receive Clock frequency RCP.
(37)	RCP	RECEIVE CLOCK. Data is transferred from RSI input to the Receiver Shift Register at the frequency of the RCP input. Each data bit is entered on the positive to negative transition (V_{IH} to V_{IL}) of RCP.
(12)	RDA	RECEIVED DATA AVAILABLE. A V_{OH} indicates a character has been transferred from the Receiver Shift Register to the Receiver Output Register. RDA is reset to V_{OL} on the trailing edge (V_{IL} to V_{IH} transition) of $\overline{RDE}$, by a V_{IL} on $\overline{RR}$ or a V_{IH} on RESET. RDA is multiplexed onto the RD0 output (33) when $\overline{SWE}$ is V_{IL} and $\overline{RDE}$ is V_{IH}.
(8)	SCR	SYNC CHARACTER RECEIVED. A V_{OH} indicates the data in the Receiver Shift Register is identical to the data in the Receiver Sync Register. SCR is reset to a V_{OL} when the character in the Receiver Shift Register does not compare to the Receiver Sync Register, on the trailing edge (V_{IL} to V_{IH} transition) of $\overline{SWE}$, by a V_{IL} on $\overline{RR}$ or a V_{IH} on RESET. SCR is multiplexed onto the RD3 output (30) when $\overline{SWE}$ is a V_{IL} and $\overline{RDE}$ is V_{IH}.
(34)	$\overline{SWE}$	STATUS WORD ENABLE. A V_{IL} enables the internal status conditions onto the output data lines RD0 – RD7. The trailing edge of $\overline{SWE}$ pulse resets FCT, ROR, RPE, and SCR to V_{OL}.
(11)	ROR	RECEIVER OVERRUN. A V_{OH} indicates data has been transferred from the Receiver Shift Register to the Receiver Output Register when RDA was still set to V_{OH}. The last data in the Output Register is lost. ROR is reset by the trailing edge (V_{IL} to V_{IH}) of $\overline{SWE}$, a V_{IL} on $\overline{RR}$, a V_{IH} on RESET or a V_{OL} to V_{OH} transition of RDA. ROR is multiplexed onto the RD1 output (32) when $\overline{SWE}$ is V_{IL} and $\overline{RDE}$ is V_{IH}.
(10)	RPE	RECEIVER PARITY ERROR. A V_{OH} indicates the accumulated parity on the received character transferred to the Output Register does not agree with the parity selected by POE. RPE is reset with the next received character with correct parity, the trailing edge (V_{IL} to V_{IH}) of $\overline{SWE}$, a V_{IL} on $\overline{RR}$ or a V_{IH} on RESET. RPE is multiplexed onto the RD2 output (31) when $\overline{SWE}$ is V_{IL} and $\overline{RDE}$ is V_{IH}.

Pin Definitions (continued)

Pin	Label	Function
(13)	$\overline{RR}$	RECEIVER RESTART. A V_{IL} resets the receiver section by clearing the status RDA, SCR, ROR, and RPE to V_{OL}. The trailing edge of $\overline{RR}$ (V_{IL} to V_{IH}) also puts the receiver in a bit transparent mode to search for a comparison, each bit time, between the contents of the Receiver Shift Register and the Receiver Sync Register. The number of data bits per character for the comparison is set by NDB1 and NDB2. After a compare is made SCR is set to V_{OH}, the sync character is transferred to the Receiver Output Register, and the receiver enters a word synchronous mode framing an input character each word time. **NOTE:** Parity is not checked on the first sync character but is enabled for every succeeding character.
(39)	NDB1	NUMBER DATA BITS. The number of Data Bits per character are determined by NDB1 and NDB2. The number of data bits does not include the parity bit. NDB2 / NDB1 / CHARACTER LENGTH V_{IL} / V_{IL} / 5 Bits V_{IL} / V_{IH} / 6 Bits V_{IH} / V_{IL} / 7 Bits V_{IH} / V_{IH} / 8 Bits For character length less than 8 bits, unused inputs are ignored and unused outputs are held to V_{OL}. Data is always right justified with D0 and RD0 being the least significant bits.
(3)	NPB	NO PARITY BIT. A V_{IH} eliminates generation of a parity bit in the transmitter and checking of parity in the receiver. With parity disabled, the RPE status bit is held at V_{OL}.
(4)	POE	PARITY ODD/EVEN. A V_{IH} directs both the transmitter and receiver to operate with even parity. A V_{IL} forces parity operation. NPB must be V_{IL} for parity to be enabled.
(5)	$\overline{CS}$	CONTROL STROBE. A V_{IL} loads the control inputs NDB1, NDB2, POE, and NPB into the Control Register. For static operation, $\overline{CS}$ can be tied directly to ground.

ASYNCHRONOUS COMMUNICATION INTERFACE ADAPTER

Features

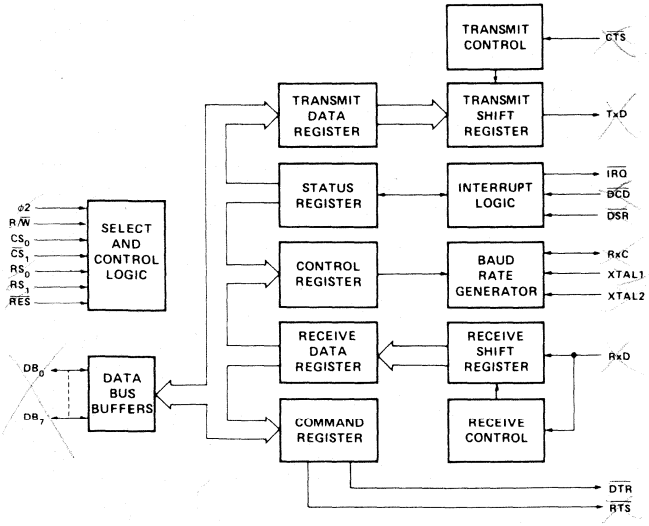
- ☐ On-Chip Baud Rate Generator: 15 Programmable Baud Rates Derived from a Standard 1.8432MHz External Crystal (50 to 19,200 Baud)
- ☐ Programmable Interrupt and Status Register to Simplify Software Design
- ☐ Single +5 Volt Power Supply
- ☐ Serial Echo Mode
- ☐ False Start Bit Detection
- ☐ 8-Bit Bi-Directional Data Bus for Direct Communication With the Microprocessor
- ☐ External 16× Clock Input for Non-Standard Baud Rates (Up to 125K Baud)
- ☐ Programmable: Word Lengths; Number of Stop Bits; and Parity Bit Generation and Detection
- ☐ Data Set and Modem Control Signals Provided
- ☐ Parity: (Odd, Even, None, Mark, Space)
- ☐ Full-Duplex or Half-Duplex Operation
- ☐ 5, 6, 7, 8 and 9-Bit Transmission

General Description

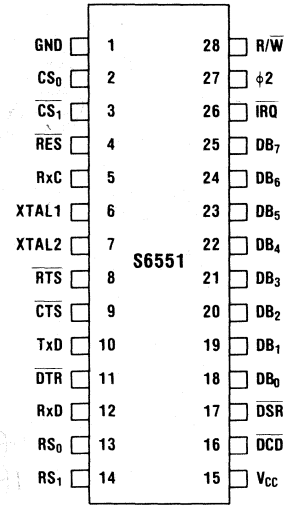
The S6551/S68051 is an Asynchronous Communication Adapter (ACIA) intended to provide for interfacing the 6500/6800 microprocessor families to serial communication data sets and modems. A unique feature is the inclusion of an on-chip programmable baud rate generator, with a crystal being the only external component required.

S6800

Block Diagram



Pin Configuration



Absolute Maximum Ratings

Supply Voltage V_{CC}	−0.3V to +7.0V
Input/Output Voltage V_{IN}	−0.3V to +7.0V
Operating Temperature Range T_A	0°C to +70°C
Storage Temperature Range T_{stg}	−55°C to +150°C

All inputs contain protection circuitry to prevent damage to high static charges. Care should be exercised to prevent unnecessary application of voltages in excess of the allowable limits.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Operating Characteristics (V_{CC} = 5.0V ± 5, T_A = 0C to +70°C, unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage	2.0	—	V_{CC}	V
V_{IL}	Input Low Voltage	−0.3	—	0.8	V
I_{IN}	Input Leakage Current: V_{IN} = 0 to 5V (φ2, R/$\overline{W}$, $\overline{RES}$, CS_0, $\overline{CS_1}$, RS_0, RS_1, $\overline{CTS}$, R×D, $\overline{DCD}$, $\overline{DSR}$)	—	±1.0	±2.5	μA
I_{TSI}	Input Leakage Current for High Impedance State (Three State)	—	±2.0	±10.0	μA
V_{OH}	Output High Voltage: I_{LOAD} = −100μA (DB_0-DB_7, T×D, R×C, $\overline{RTS}$, $\overline{DTR}$)	2.4	—	—	V
V_{OL}	Output Low Voltage: I_{LOAD} = 1.6mA (DB_0-DB_7, T×D, R×C, $\overline{RTS}$, $\overline{DTR}$, $\overline{IRQ}$)	—	—	0.4	V
I_{OH}	Output High Current (Sourcing): V_{OH} = 2.4V (DB_0-DB_7, T×D, R×C, $\overline{RTS}$, $\overline{DTR}$)	−100	—	—	μA
I_{OL}	Output Low Current (Sinking): V_{OL} = 2.4V (DB_0-DB_7, T×D, R×C, $\overline{RTS}$, $\overline{DTR}$, $\overline{IRQ}$)	1.6	—	—	mA
I_{OFF}	Output Leakage Current (Off State): V_{OUT} = 5V ($\overline{IRQ}$)	—	1.0	10.0	μA
C_{CLK}	Clock Capacitance (φ2)	—	—	20	pF
C_{IN}	Input Capacitance (Except XTAL1 and XTAL2)	—	—	10	pF
C_{OUT}	Output Capacitance	—	—	10	pF
P_D	Power Dissipation (See Graph) (T_A = 0°C)	—	170	300	mW

Write Cycle ($V_{CC}=5.0V\pm5$, $T_A=0C$ to $+70°C$, unless otherwise noted)

Symbol	Parameter	S6551		S65B51		Unit
		Min.	Max.	Min.	Max.	
t_{CYC}	Cycle Time	1.0	—	0.5	—	μs
t_C	φ2 Pulse Width	400	—	200	—	ns
t_{ACW}	Address Set-Up Time	120	—	70	—	ns
t_{CAH}	Address Hold Time	0	—	0	—	ns
t_{WCW}	R/$\overline{W}$ Set-Up Time	120	—	70	—	ns
t_{CWH}	R/$\overline{W}$ Hold Time	0	—	0	—	ns
t_{DCW}	Data Bus Set-Up Time	150	—	60	—	ns
t_{HW}	Data Bus Hold Time	20	—	20	—	ns

(t_r and t_f=10 to 30ns)

Figure 1. Power Dissipation vs Temperature

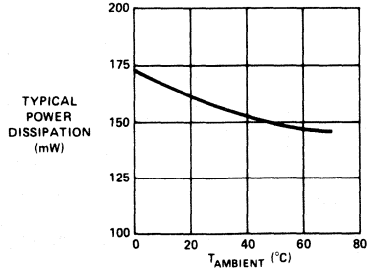
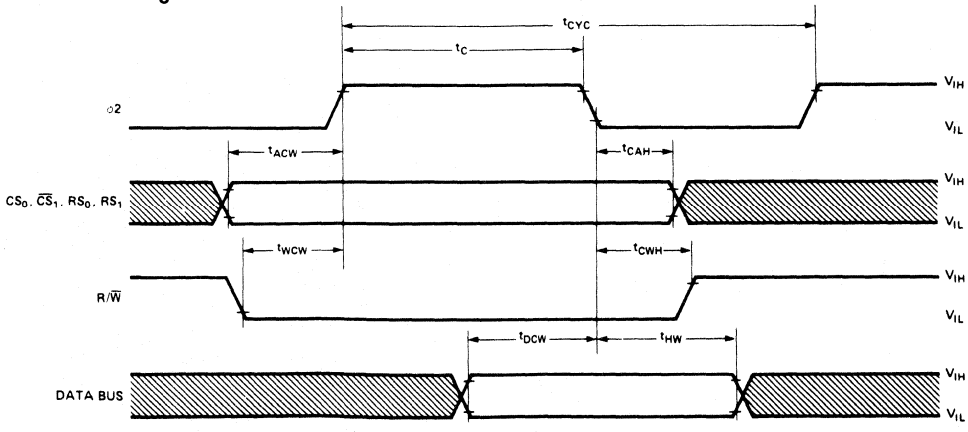


Figure 2. Write Timing Characteristics



Read Cycle (V_{CC} = 5.0V ± 5, T_A = 0C to +70°C, unless otherwise noted)

Symbol	Parameter	S6551		S65B51		Unit
		Min.	Max.	Min.	Max.	
t_{CYC}	Cycle Time	1.0	—	0.5	—	μs
t_C	φ2 Pulse Width	400	—	200	—	ns
t_{ACR}	Address Set-Up Time	120	—	70	—	ns
t_{CAR}	Address Hold Time	0	—	0	—	ns
t_{WCR}	R/$\overline{W}$ Set-Up Time	120	—	70	—	ns
t_{CDR}	Read Access Time (Valid Data)	—	200	—	150	ns
t_{HR}	Read Hold Time	20	—	20	—	ns
t_{CDA}	Bus Active Time (Invalid Data)	40	—	40	—	ns

Figure 3. Clock Generation

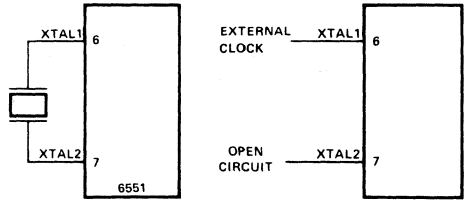


Figure 4. Read Timing Characteristics

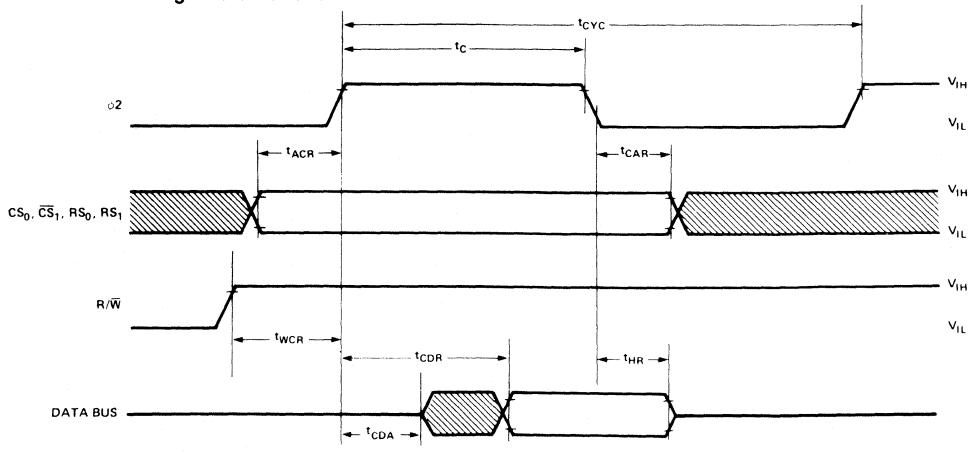


Figure 5. Test Load for Data Bus (DB_0-DB_7), $\overline{TxD}$, $\overline{DTR}$, RTS Outputs

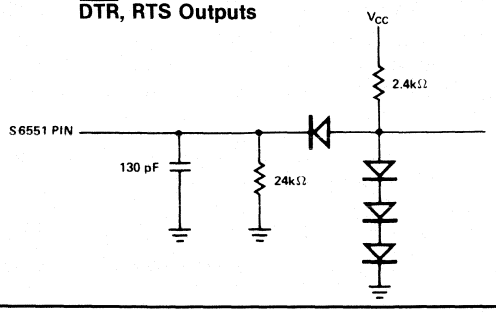


Figure 6a. Interrupt and Output Timing

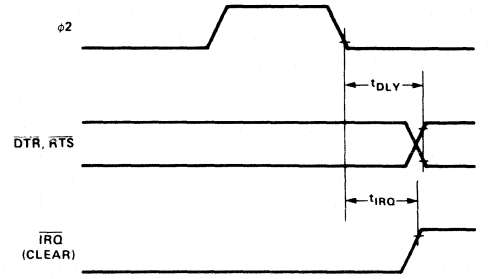
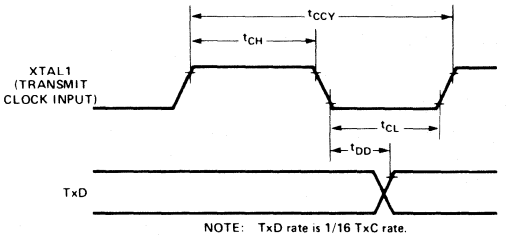
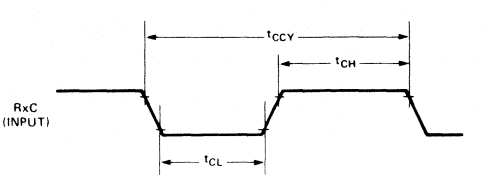


Figure 6b. Transmit Timing with External Clock



NOTE: TxD rate is 1/16 TxC rate.

Figure 6c. Receive External Clock Timing



NOTE: RxD rate is 1/16 RxC rate.

S6800

Transmit/Receive Characteristics

Symbol	Parameter	S6551		S65B51		Unit
		Min.	Max.	Min.	Max.	
t_{CCY}	Transmit/Receive Clock Rate	400*	—	400*	—	ns
t_{CH}	Transmit/Receive Clock High Time	175	—	175	—	ns
t_{CL}	Transmit/Receive Low Time	175	—	175	—	ns
t_{DD}	EXTAL1 to TxD Propagation Delay	—	500	—	500	ns
t_{DLY}	Propagation Delay ($\overline{RTS}$, DTR)	—	500	—	500	ns
t_{IRQ}	$\overline{IRQ}$ Propagation Delay (Clear)	—	500	—	500	ns

(t_r and t_f=10 to 30ns)

*The baud rate with external clocking is: Baud Rate = $\frac{1}{16 \times T_{CCY}}$

Pin Description

$\overline{RES}$ (Reset). During system initialization a low on the $\overline{RES}$ input will cause internal registers to be cleared.

φ2 Input Clock. The input clock is the system φ2 clock and is used to trigger all data transfers between the system microprocessor and the S6551.

R/$\overline{W}$ (Read/Write). The R/$\overline{W}$ is generated by the microprocessor and is used to control the direction of data transfers. A high on the R/$\overline{W}$ pin allows the processor to read the data supplied by the S6551. A low on the R/$\overline{W}$ pin allows a write to the S6551.

$\overline{IRQ}$ (Interrupt Request). The $\overline{IRQ}$ pin is an interrupt signal from the interrupt control logic. It is an open drain output, permitting several devices to be connected to the common $\overline{IRQ}$ microprocessor input. Normally a high level, $\overline{IRQ}$ goes low when an interrupt occurs.

DB_0-DB_7 (Data Bus). The DB_0-DB_7 pins are the eight data lines used for transfer of data between the processor and the S6551. These lines are bi-directional and are normally high-impedance except during Read cycles when selected.

CS_0-$\overline{CS_1}$ (Chip Selects). The two chip select inputs are normally connected to the processor address lines either directly or through decoders. The S6551 is selected when CS_0 is high and $\overline{CS_1}$ is low.

RS_0, RS_1 (Register Selects). The two register select lines are normally connected to the processor address lines to allow the processor to select the various S6551 internal registers. The following table indicates the internal register select coding:

Table 1

RS_1	RS_0	WRITE	READ
0	0	Transmit Data Register	Receiver Data Register
0	1	Programmed Reset (Data is "Don't Care")	Status Register
1	0	Command Register	
1	1	Control Register	

The table shows that only the Command and Control registers are read/write. The Programmed Reset operation does not cause any data transfer, but is used to clear the S6551 registers. The Programmed Reset is slightly different from the Hardware Reset ($\overline{RES}$) and these differences are described in the individual register definitions.

XTAL1, XTAL2 (Crystal Pins). These pins are normally directly connected to the external crystal (1.8432MHz) used to derive the various baud rates. Alternatively, an externally generated clock may be used to drive the XTAL1 pin, in which case the XTAL2 pin must float. The choice of crystal is not critical, but CTS Knights MPO18 is recommended.

T×D (Transmit Data). The T×D output line is used to transfer serial NRZ (non-return-to-zero) data to the modem. The LSB (least significant bit) of the Transmit Data Register is the first data bit transmitted and the rate of data transmission is determined by the baud rate selected.

R×D (Receive Data). The R×D input line is used to transfer serial NRZ data into the ACIA from the modem, LSB first. The receiver data rate is either the programmed baud rate or the rate of an externally generated receiver clock. This selection is made by programming the Control Register.

R×C (Receive Clock). The R×C is a bi-directional pin which serves as either the receiver 16×clock input or the receiver 16×clock output. The latter mode results if the internal baud rate generator is selected for receiver data clocking.

$\overline{RTS}$ (Request to Send). The $\overline{RTS}$ output pin is used to control the modem from the processor. The state of the $\overline{RTS}$ pin is determined by the contents of the Command Register.

$\overline{CTS}$ (Clear to Send). The $\overline{CTS}$ input pin is used to control the transmitter operation. The enable state is with $\overline{CTS}$ low. The transmitter is automatically disabled if $\overline{CTS}$ is high.

$\overline{DTR}$ (Data Terminal Ready). This output pin is used to to indicate the status of the S6551 to the modem. A low on $\overline{DTR}$ indicates the S6551 is enabled and a high indicates it is disabled. The processor controls this pin via bit 0 of the Command Register.

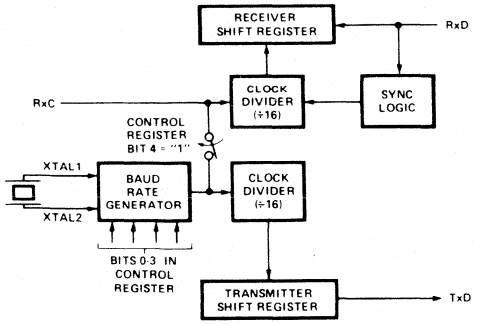
$\overline{DSR}$ (Data Set Ready). The $\overline{DSR}$ input pin is used to indicate to the S6551 the status of the modem. A low indicates the "ready" state and a high, "not-ready." $\overline{DSR}$ is a high-impedance input and must not be a no-connect. If unused, it should be driven high or low, but not switched.

$\overline{DCD}$ (Data Carrier Detect). The $\overline{DCD}$ input pin is used to indicate to the S6551 the status of the carrier-detect output of the modem. A low indicates that the modem carrier signal is present and a high, that it is not. $\overline{DCD}$, like $\overline{DSR}$, is a high-impedance input and must not be a no-connect.

Internal Organization

The Transmitter/Receiver sections of the S6551 are depicted by the block diagram in Figure 7.

Figure 7. Transmitter/Receiver Clock Circuits



Bits 0-3 of the Control Register select the divisor used to generate the baud rate for the Transmitter. If the Receiver clock is to use the same baud rate as the Transmitter, then R×C becomes an output pin and can be used to slave other circuits to the S6551.

Control Register

The Control Register is used to select the desired mode for the S6551. The word length, number of stop bits, and clock controls are all determined by the Control Register, which is depicted in Figure 8.

Command Register

The Command Register is used to control Specific Transmit/Receive functions and is shown in Figure 9.

Figure 8. Control Register Format

CONTROL REGISTER

7	6	5	4	3	2	1	0

STOP BITS

0 = 1 Stop Bit
1 = 2 Stop Bits
1 Stop Bit if Word Length = 8 Bits and Parity*
1½ Stop Bits if Word Length = 5 Bits and No Parity.

WORD LENGTH

BIT 6	BIT 5	DATA WORD LENGTH
0	0	8
0	1	7
1	0	6
1	1	5

RECEIVER CLOCK SOURCE

0 = External Receiver Clock
1 = Baud Rate Generator

BAUD RATE GENERATOR

0	0	0	0	16x EXTERNAL CLOCK
0	0	0	1	50 BAUD
0	0	1	0	75
0	0	1	1	109.92
0	1	0	0	134.58
0	1	0	1	150
0	1	1	0	300
0	1	1	1	600
1	0	0	0	1200
1	0	0	1	1800
1	0	1	0	2400
1	0	1	1	3600
1	1	0	0	4800
1	1	0	1	7200
1	1	1	0	9600
1	1	1	1	19,200

*This allows for 9 bit transmission (8 data bits plus parity).

	7	6	5	4	3	2	1	0
HARDWARE RESET	0	0	0	0	0	0	0	0
PROGRAM RESET	–	–	–	–	–	–	–	–

Figure 9. Command Register Format

COMMAND REGISTER

7	6	5	4	3	2	1	0

PARITY CHECK CONTROLS

BIT 7	BIT 6	BIT 5	OPERATION
–	–	0	Parity Disabled - No Parity Bit Generated - No Parity Bit Received
0	0	1	Odd Parity Receiver and Transmitter
0	1	1	Even Parity Receiver and Transmitter
1	0	1	Mark Parity Bit Transmitted, Parity Check Disabled
1	1	1	Space Parity Bit Transmitted, Parity Check Disabled

NORMAL/ECHO MODE FOR RECEIVER

0 = Normal
1 = Echo (Bits 2 and 3 must be "0")

DATA TERMINAL READY

0 = Disable Receiver and All Interrupts ($\overline{DTR}$ high)
1 = Enable Receiver and All Interrupts ($\overline{DTR}$ low)

RECEIVER INTERRUPT ENABLE

0 = $\overline{IRQ}$ Interrupt Enabled from Bit 3 of Status Register
1 = $\overline{IRQ}$ Interrupt Disabled

TRANSMITTER CONTROLS

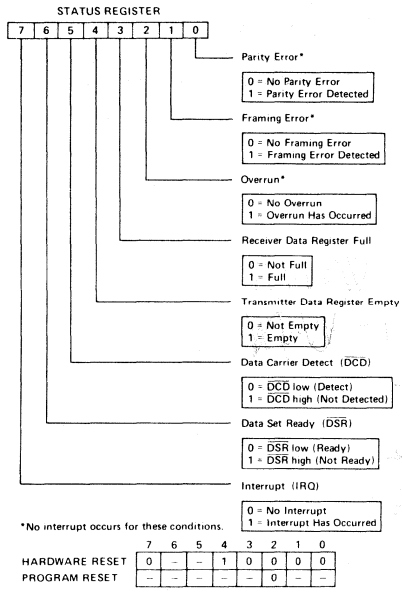
BIT 3	BIT 2	TRANSMIT INTERRUPT	$\overline{RTS}$ LEVEL	TRANSMITTER
0	0	Disabled	High	Off
0	1	Enabled	Low	On
1	0	Disabled	Low	On
1	1	Disabled	Low	Transmit BRK

	7	6	5	4	3	2	1	0
HARDWARE RESET	0	0	0	0	0	0	0	0
PROGRAM RESET	–	–	–	0	0	0	0	0

Status Register

The Status Register is used to indicate to the processor the status of various S6551 functions and is outlined in Figure 10.

Figure 10. Status Register Format



Transmit and Receive Data Registers

These registers are used as temporary data storage for the S6551 Transmit and Receive circuits. The Transmit Data Register is characterized as follows:

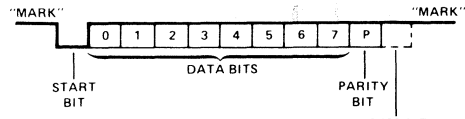
- ☐ Bit 0 is the leading bit to be transmitted.
- ☐ Unused data bits ae the high-order bits and are "don't care" for transmission.

The Receive Data Register is characterized in a similar fashion:

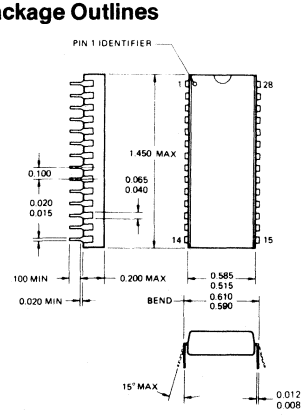
- ☐ Bit 0 is the leading bit received.
- ☐ Unused data bits are the high-order bits and are "0" for the receiver.
- ☐ Parity bits are not contained in the Receive Data Register, but are stripped-off after being used for external parity checking. Parity and all unused high-order bits are "0".

Figure 11 illustrates a single transmitted or received data word, for the example of 8 data bits, parity, and 1 stop bit.

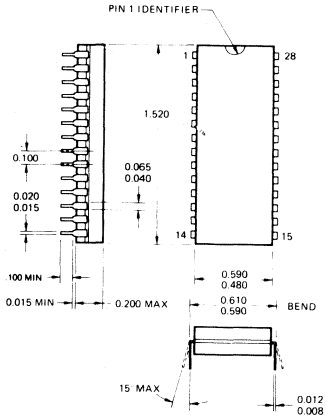
Figure 11. Serial Data Stream Example



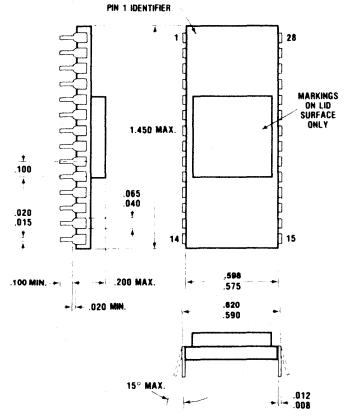
Package Outlines



28-Lead Plastic



28-Lead Cerdip



28-Lead Ceramic

AMERICAN MICROSYSTEMS, INC.

S6821/S68A21/S68B21

PERIPHERAL INTERFACE ADAPTER (PIA)

Features

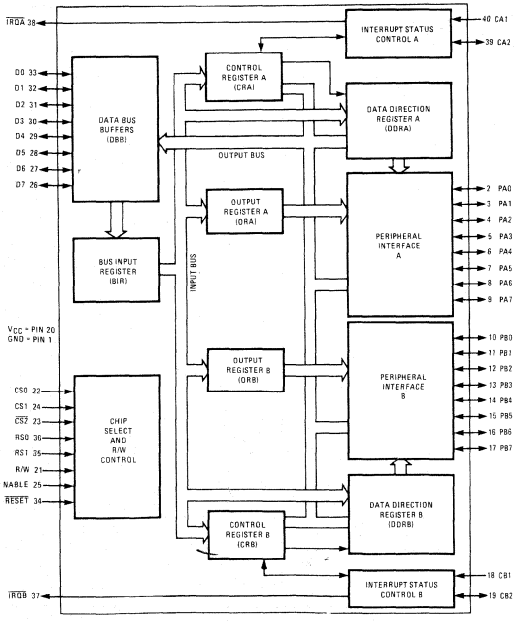
- ☐ 8-Bit Bidirectional Bus for Communication with the MPU
- ☐ Two Bidirectional 8-Bit Buses for Interface to Peripherals
- ☐ Two Programmable Control Registers
- ☐ Two Programmable Data Direction Registers
- ☐ Four Individually-Controlled Interrupt Input Lines: Two Usable as Peripheral Control Outputs
- ☐ Handshake Control Logic for Input and Output Peripheral Operation
- ☐ High-Impedance Three-State and Direct Transistor Drive Peripheral Lines
- ☐ Program Controlled Interrupt and Interrupt Disable Capability
- ☐ CMOS Compatible Peripheral Lines
- ☐ Two TTL Drive Capability on all A and B Side Buffers
- ☐ TTL Compatible
- ☐ Static Operation

General Description

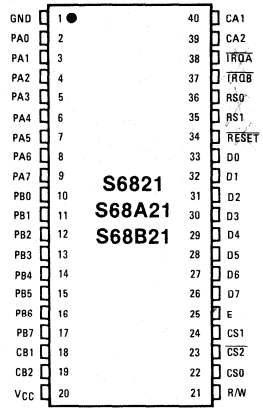
The S6821/S68A21/S68B21 are peripheral Interface Adapters that provide the universal means of interfacing peripheral equipment to the S6800/S68A00/S68B00 Microprocessing Units (MPU). This device is capable of interfacing the MPU to peripherals through two 8-bit bidirectional peripheral data buses and four control lines. No external logic is required for interfacing to most peripheral devices.

The functional configuration of the PIA is programmed by the MPU during system initialization Each of the peripheral data lines can be programmed to act as an

Block Diagram



Pin Configuration



General Description (Continued)

input or output, and each of the four control/interrupt lines may be programmed for one of several control modes. This allows a high degree of flexibility in the overall operation of the interface.

The PIA interfaces to the S6800/S68A00/S68B00 MPUs with an eight-bit bidirectional data bus, three chip select lines, two register select lines, two interrupt request lines, read/write line, enable line and reset line. These signals, in conjunction with S6800/S68A00/S68B00 VMA output, permit the MPU to have complete control over the PIA. VMA may be utilized to gate the input signals to the PIA.

Absolute Maximum Ratings:

Symbol	Rating	Value	Unit
V_{CC}	Supply Voltage	−0.3 to +7.0	Vdc
V_{IN}	Input Voltage	−0.3 to +7.0	Vdc
T_A	Operating Temperature Range	0° to +70°	°C
T_{stg}	Storage Temperature Range	−55° to +150°	°C
θ_{ja}	Thermal Resistance	82.5	°C/W

Note:
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Electrical Characteristics

V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = T_L to T_H unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Conditions
Bus Control Inputs (R/$\overline{W}$, Enable, $\overline{Reset}$, RS0, RS1, CS0, CS1, $\overline{CS2}$)						
V_{IH}	Input High Voltage	V_{SS}+2.0	—	V_{CC}	Vdc	
V_{IL}	Input Low Voltage	V_{SS}−0.8	—	V_{SS}+0.8	Vdc	
I_{IN}	Input Leakage Current	—	1.0	2.5	μAdc	V_{IN}=0 to 5.25 Vdc
C_{IN}	Capacitance	—	—	7.5	pF	V_{IN}=0, T_A=25°C, f=1.0MHz
Interrupt Outputs ($\overline{IRQA}$, $\overline{IRQB}$)						
V_{OL}	Output Low Voltage	—	—	V_{SS}+0.4	Vdc	I_{LOAD}=3.2 mAdc
I_{LOH}	Output Leakage Current (Off State)	—	1.0	10	μAdc	V_{OH}=2.4 Vdc
C_{OUT}	Capacitance	—	—	5.0	pF	V_{IN}=0, T_A=25°C, f=1.0MHz
Data Bus (D0-D7)						
V_{IH}	Input High Voltage	V_{SS}+2.0	—	V_{CC}	Vdc	
V_{IL}	Input Low Voltage	V_{SS}−0.3	—	V_{SS}+0.8	Vdc	
I_{TSI}	Three State (Off State) Input Current	—	2.0	10	μAdc	V_{IN}=0.4 to 2.4 Vdc
V_{OH}	Output High Voltage	V_{SS}+2.4	—	—	Vdc	I_{LOAD}=−205μAdc
V_{OL}	Output Low Voltage	—	—	V_{SS}+0.4	Vdc	I_{LOAD}=1.6mAdc
C_{IN}	Capacitance	—	—	12.5	pF	V_{IN}=0, T_A=25°C f=1.0MHz

Electrical Characteristics (Continued)

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Conditions
Peripheral Bus (PA0-PA7, PB0-PB7, CA1, CA2, CB1, CB2)						
I_{IN}	Input Leakage Current R/$\overline{W}$, $\overline{Reset}$, RS0, CS0, CS1, $\overline{CS2}$, CA1, CB1, Enable		1.0	2.5	μAdc	V_{IN}=0 to 5.25 Vdc
I_{TSI}	Three-State (Off State) Input Current PB0-PB7, CB2		2.0	10	μAdc	V_{IN}=0.4 to 2.4 Vdc
I_{IH}	Input High Current PA0-PA7, CA2	−200	−400		μAdc	V_{IH}=2.4 Vdc
I_{OH}	Darlington Drive Current PB0-PB7, CB2	−1.0		.10	mAdc	V_O=1.5 Vdc
I_{IL}	Input Low Current PA0-PA7, CA2		−1.3	−2.4	mAdc	V_{IL}=0.4Vdc
V_{OH}	Output High Voltage PA0-P7, PB0-PB7, CA2, CB2 PA0-PA7, CA2	V_{SS}+2.4 V_{CC}−1.0			Vdc	I_{LOAD}=−200μAdc I_{LOAD}=−10μAdc
V_{OL}	Output Low Voltage			V_{SS}+0.4	Vdc	I_{LOAD}=3.2mAdc
C_{IN}	Capacitance			10	pF	V_{IN}=0, T_A=25°C, f=1.0MHz
Power Requirements						
P_D	Power Dissipation			550	mW	

A.C. (Dynamic) Characteristics Loading=30pF and one TTL load for PA0-PA7, PB0-PB7, CA2, CB2
=130pF and one TTL load for D0-D7, $\overline{IRQA}$, $\overline{IRQB}$
(V_{CC}=+5.0V±5%, T_A=0°C to +70°C unless otherwise noted)

Peripheral Timing Characteristics: V_{CC}−5.0V±5%, V_{SS}=0V, T_A=T_L to T_H unless otherwise specified

		S6821		S68A21		S68B21		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Units
t_{PDSU}	Peripheral Data Setup Time	200		135		100		ns
t_{PDH}	Peripheral Data Hold Time	0		0		0		ns
t_{CA2}	Delay Time, Enable Negative Transition to CA2 Negative Transition		1.0		0.670		0.5	μs
t_{RS1}	Delay Time, Enable Negative Transition to CA2 Positive Transition		1.0		0.670		0.50	μs
t_r, t_f	Rise and Fall Times for CA1 and CA2 Input Signals		1.0		1.0		1.0	μs
t_{RS2}	Delay Time from CA1 Active Transition to CA2 Positive Transition		2.0		1.35		1.0	μs
t_{PDW}	Delay Time, Enable Negative Transition to Peripheral Data Valid		1.0		0.670		0.5	μs
t_{CMOS}	Delay Time, Enable Negative Transition to Peripheral CMOS Data Valid PA0-PA7, CA2		2.0		1.35		1.0	μs

Peripheral Timing Characteristics (Continued)

Symbol	Parameter	S6821		S68A21		S68B21		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CB2}	Delay Time, Enable Positive Transition to CB2 Negative Transition		1.0		0.670		0.5	μs
t_{DC}	Delay Time, Peripheral Data Valid to CB2 Negative Transition	2.0		20		20		ns
t_{RS1}	Delay Time, Enable Positive Transition to CB2 Positive Transition		1.0		0.670		0.5	μs
PW_{CT}	Peripheral Control Output Pulse Width, CA2/CB2	550		550		550		ns
t_r, t_f	Rise and Fall Times for CB1 and CB2 Input Signals		1.0		1.0		1.0	μs
t_{RS2}	Delay Time, CB1 Active Transition to CB2 Positive Transition		2.0		1.35		1.0	μs
t_{IR}	Interrupt Release Time, $\overline{IRQA}$ and $\overline{IRQB}$		1.60		1.1		0.85	μs
t_{RS3}	Interrupt Response Time		1.0		1.0		1.0	μs
PW_I	Interrupt Input Pulse Width	500		500		500		ns
t_{RL}	Reset Low Time*	1.0		0.66		0.5		μs

*The Reset line must be high a minimum of 1.0μs before addressing the PIA.

Figure 1. Enable Signal Characteristics

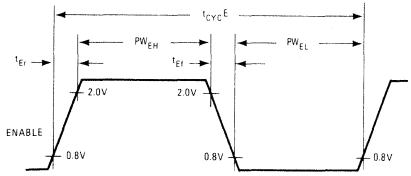


Figure 2. Bus Read Timing Characteristics (Read Information from PIA)

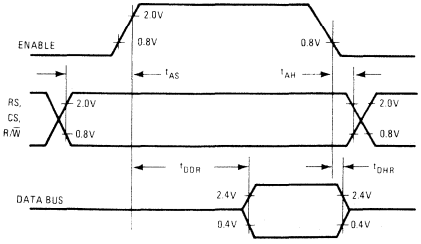


Figure 3. Bus Write Timing Characteristics (Write Information into PIA)

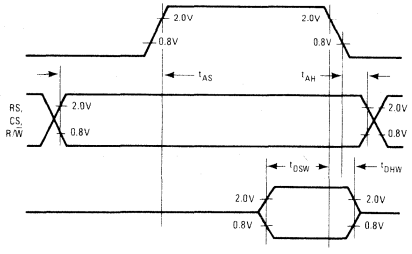
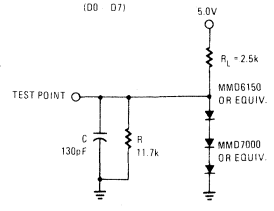


Figure 4. Bus Timing Test Loads



Bus Timing Characteristics (V_{CC} = +5.0V ±5%, V_{SS} = 0, T_A = T_L to T_H unless otherwise noted.)

Symbol	Parameter	S6821		S68A21		S68B21		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{cyc(E)}$	Enable Cycle Time	1000		666		500		ns
PW_{EH}	Enable Pulse Width, High	450		280		220		ns
PW_{EL}	Enable Pulse Width, Low	430		280		210		ns
t_{Er},t_{Ef}	Enable Pulse Rise and Fall Times		25		25		25	ns
t_{AS}	Setup Time, Address and R/W Valid to Enable Positive Transition	160		140		70		ns
t_{AH}	Address Hold Time	10		10		10		ns
t_{DDR}	Data Delay Time, Read		320		220		180	ns
t_{DHR}	Data Hold Time, Read	10		10		10		ns
t_{DSW}	Data Setup Time, Write	195		80		60		ns
t_{DHW}	Data Hold Time, Write	10		10		10		ns

Figure 5. TTL Equiv. Test Load

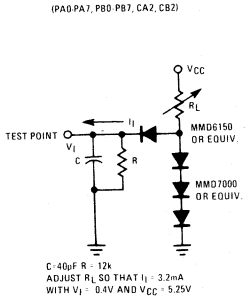


Figure 6. CMOS Equiv. Test Load

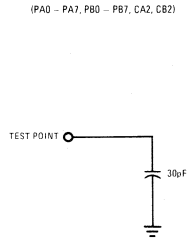


Figure 7. NMOS Equiv. Test Load

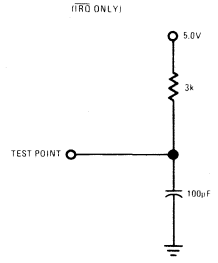


Figure 8. Peripheral Data Setup and Hold Times (Read Mode)

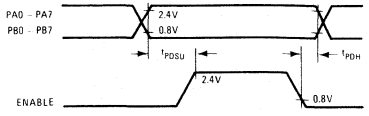
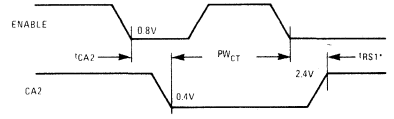


Figure 9. CA2 Delay Time (Read Mode; CRA-5 = CRA-3 = 1, CRA-4 = 0)



*Assumes part was deselected during the previous E pulse.

Figure 10. CA2 Delay Time (Read Mode; CRA-5 = 1, CRA-3 = CRA-4 = 0)

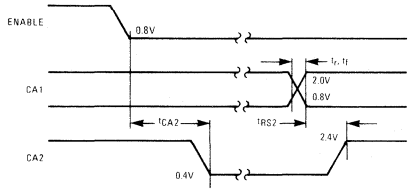


Figure 11. Peripheral CMOS Data Delay Times (Write Mode; CRA-5 = CRA-3 = 1, CRA-4 = 0)

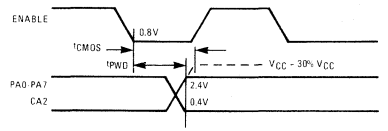
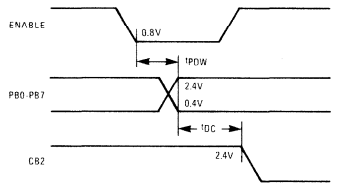


Figure 12. Peripheral Data and CB2 Delay Times (Write Mode; CRB-5 = CRB-3 = 1, CRB-4 = 0)



CB2 Note:
CB2 goes low as a result of the positive transition of Enable.

Figure 13. CB2 Delay Time (Write Mode; CRB-5 = CRB-3 = 1. CRB-4 = 0)

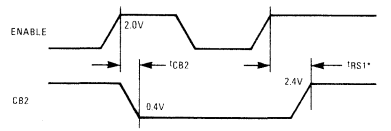
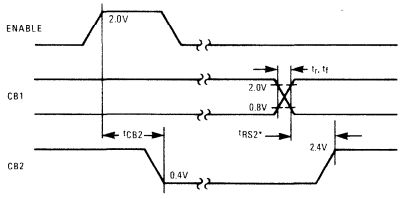
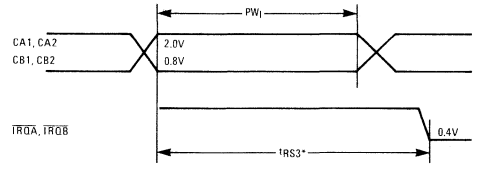


Figure 14. CB2 Delay Time (Write Mode; CRB-5 = 1, CRB-3 = CRB-4 = 0)



*Assumes part was deselected during any previous E pulse.

Figure 15. Interrupt Pulse Width and $\overline{IRQ}$ Response



*Assumes Interrupt Enable Bits are set.

Figure 16. $\overline{IRQ}$ Release Time

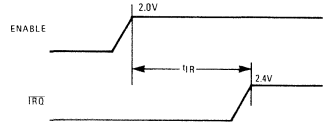
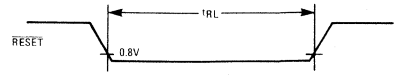
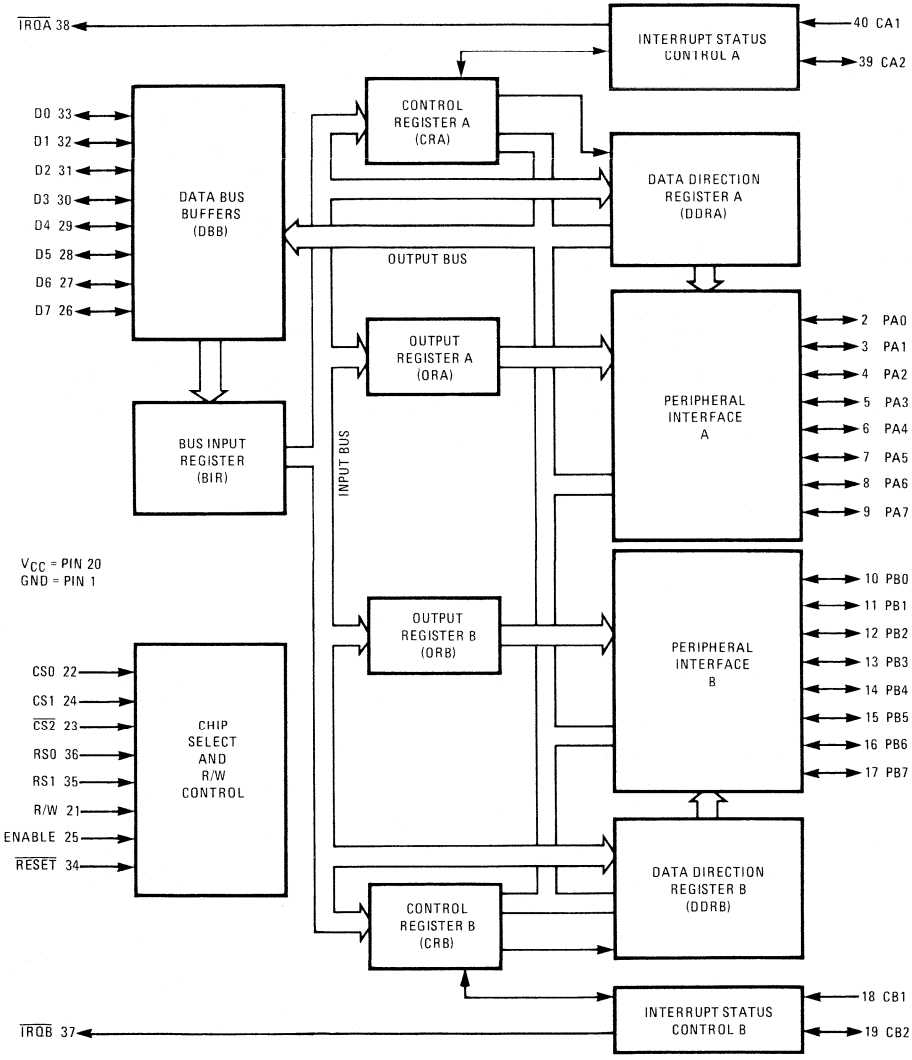


Figure 17. $\overline{Reset}$ Low Time.



*The $\overline{Reset}$ line must be a V_{IH} for a minimum of 1.0μs before addressing the PIA.

Expanded Block Diagram



Interface Description

MPU/PIA Interface

Pin	Label	Function
(33)	D0	**Bidirectional Data** — The bidirectional data lines (D0-D7) allow the transfer of data between the MPU and the PIA. The data bus output drivers are three-state devices that remain in the high-impedance (off) state except when the MPU performs a PIA read operation. The Read/Write line is in the Read (high) state when the PIA is selected for a Read operation.
(32)	D1	
(31)	D2	
(30)	D3	
(29)	D4	
(28)	D5	
(27)	D6	
(26)	D7	
(25)	E	**Enable** — The enable pulse, E, is the only timing signal that is supplied to the PIA. Timing of all other signals is referenced to the leading and trailing edges of the E pulse. This signal will normally be a derivative of the S6800 $\phi 2$ Clock. The E pulse is used to condition the interrupt/control lines CA1, CA2, CB1 and CB2. At least one E pulse must occur from the inactive edge to the active edge of the input signal to set the interrupt flag, when the lines are used as inputs.
(21)	R/W	**Read/Write** — This signal is generated by the MPU to control the direction of data transfers on the Data Bus. A low state on the PIA Read/Write line enables the input buffers and data is transferred from the MPU to the PIA on the E signal if the device has been selected. A high on the Read/Write line sets up the PIA for a transfer of data to the bus. The PIA output buffers are enabled when the proper address and the enable pulse E are present.
(34)	$\overline{\text{RESET}}$	**$\overline{\text{Reset}}$** — The active low $\overline{\text{Reset}}$ line is used to reset all register bits in the PIA to a logical zero (low). This line can be used as a power-on reset and as a master reset during system operation.
(22)	CS0	**Chip Select** — These three input signals are used to select the PIA. CS0 and CS1 must be high and $\overline{\text{CS2}}$ must be low for selection of the device. Data transfers are then performed under the control of the Enable and Read/Write signals. The chip select lines must be stable for the duration of the E pulse.
(24)	CS1	
(23)	$\overline{\text{CS2}}$	
(36)	RS0	**PIA Register Select** — The two register select lines are used to select the various registers inside the PIA. These two lines are used in conjunction with internal Control Registers to select a particular register that is to be written or read. The Register select lines should be stable for the duration of the E pulse while in the read or write cycle.
(35)	RS1	

(38)	$\overline{IRQA}$	**Interrupt Request** — The active low Interrupt Request lines ($\overline{IRQA}$ and $\overline{IRQB}$) act to interrupt the MPU either directly or through interrupt priority circuitry. These lines are "open source" (no load device on the chip) and are capable of sinking a current of 1.6mA from an external source. This permits all interrupt request lines to be tied together in a wire-OR configuration.
(37)	$\overline{IRQB}$	

Each Interrupt Request line has two internal interrupt flag bits that will cause the Interrupt Request line to go low. Each flag bit is associated with a particular peripheral interrupt line. Also, four interrupt enable bits are provided in the PIA which may be used to inhibit a particular interrupt from a peripheral device.

Servicing an interrupt by the MPU is accomplished by a software routine that, on a prioritized basis, sequentially reads and tests the two control registers in each PIA for interrupt flag bits that are set.

The Interrupt Flag is cleared (zeroed) as a result of an MPU Read Peripheral Data Operation.

PIA/Peripheral Interface

Pin	Label	Function
(2)	PA0	**Section A Peripheral Data** — Each of the peripheral data lines can be programmed to act as an input or output. This is accomplished by setting a "1" in the corresponding Data Direction Register bit for those lines which are to be outputs. A "0" in a bit of the Data Direction Register causes the corresponding peripheral data line to act as an input. During an MPU Read Peripheral Data Operation, the data on peripheral lines programmed to act as inputs appears directly on the corresponding MPU Data Bus lines. In the input mode the internal pullup resistor on these lines represents a maximum of one standard TTL load.
(3)	PA1	
(4)	PA2	
(5)	PA3	
(6)	PA4	
(7)	PA5	
(8)	PA6	
(9)	PA7	

The data in Output Register A will appear on the data lines that are programmed to be outputs. A logical "1" written into the register will cause a "high" on the corresponding data line while a "0" results in a "low." Data in Output Register A may be read by an MPU "Read Peripheral Data A" operation when the corresponding lines are programmed as outputs. This data will be read properly if the voltage on the peripheral data lines is greater than 2.0 volts for a logic "1" output and less than 0.8 volts for a logic "0" output. Loading the output lines such that the voltage on these lines does not reach full voltage causes the data transferred into the MPU on a Read operation to differ from that contained in the respective bit of Output Register A.

(10)	PB0	**Section B Peripheral Data** — The peripheral data lines in the B Section of the PIA can be programmed to act as either inputs or outputs in a similar manner to PA0-PA7. However, the output buffers driving these lines differ from those driving lines PA0-PA7. They have three-state capability, allowing them to enter a high impedance state when the peripheral data line is used as an input. In addition, data on the peripheral data lines PB0-PB7 will be read properly from those lines programmed as outputs even if the voltages are below 2.0 volts for a "high." As outputs, these lines are compatible with standard TTL and may also be used as a source of up to 1 milliampere at 1.5 volts to directly drive the base of a transistor switch.
(11)	PB1	
(12)	PB2	
(13)	PB3	
(14)	PB4	
(15)	PB5	
(16)	PB6	
(17)	PB7	

(40) (18)	CA1 CB1	**Interrupt Input** — Peripheral Input lines CA1 and CB1 are input-only lines that set the interrupt flags of the control registers. The active transition for these signals is also programmed by the two control registers.
(39)	CA2	**Peripheral Control** — The peripheral control line CA2 can be programmed to act as an interrupt input or as a peripheral control output. As an output, this line is compatible with standard TTL; as an input the internal pullup resistor on this line represents one standard TTL load. The function of this signal line is programmed with Control Register A.
(19)	CB2	**Peripheral Control** — Peripheral Control line CB2 may also be programmed to act as an interrupt input or peripheral control output. As an input, this line has high input impedance and is compatible with standard TTL. As an output, it is compatible with standard TTL and may also be used as a source of up to 1 milliampere at 1.5 volts to directly drive the base of a transistor switch. This line is programmed by Control Register B.
(1)	GND	**Ground**
(20)	V_{CC}	+5Volts ±5%

AMERICAN MICROSYSTEMS, INC.

S68H21

PERIPHERAL INTERFACE ADAPTER (PIA)

Features

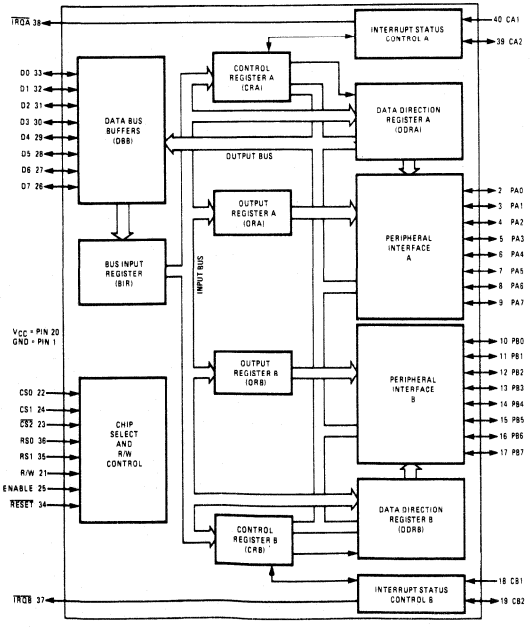
- ☐ **8-Bit Bidirectional Bus for Communication with the MPU**
- ☐ **Two Bidirectional 8-Bit Buses for Interface to Peripherals**
- ☐ **Two Programmable Control Registers**
- ☐ **Two Programmable Data Direction Registers**
- ☐ **Four Individually-Controlled Interrupt Input Lines: Two Usable as Peripheral Control Outputs**
- ☐ **Handshake Control Logic for Input and Output Peripheral Operation**
- ☐ **High-Impedance Three-State and Direct Transistor Drive Peripheral Lines**
- ☐ **Program Controlled Interrupt and Interrupt Disable Capability**
- ☐ **CMOS Compatible Peripheral Lines**

General Description

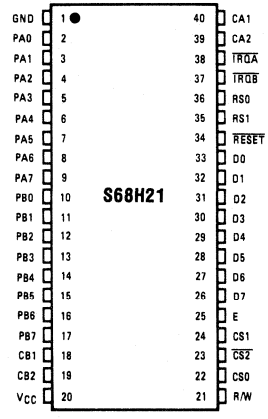
The S68H21 is a peripheral Interface Adapter that provides the universal means of interfacing peripheral equipment to the S68H00 Microprocessing Unit (MPU). This device is capable of interfacing the MPU to peripherals through two 8-bit bidirectional peripheral data buses and four control lines. No external logic is required for interfacing to most peripheral devices.

The functional configuration of the PIA is programmed by the MPU during system initialization. Each of the peripheral data lines can be programmed to act as an input or output, and each of the four control/interrupt lines may be programmed for one of several control modes. This allows a high degree of flexibility in the overall operation of the interface.

Block Diagram



Pin Configuration



General Description (Continued)

The PIA interfaces to the S68H00 with an eight-bit bidirectional data bus, three chip chip select lines, two interrupt request lines, read/write line, enable line and reset line. These signals, in conjunction with the S68H00 output, permit the MPU to have complete control over the PIA. VMA may be utilized to gate the input signals to the PIA.

Absolute Maximum Ratings

Supply Voltage	−0.3 to +7.0V
Input Voltage	−0.3 to +7.0V
Operating Temperature Range	0° to +70°C
Storage Temperature Range	−55° to +150°C

Note:
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Electrical Characteristics

V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = 0°C to +70°C unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{IH}	Input High Voltage	V_{SS}+2.0		V_{CC}	Vdc	
V_{IL}	Input Low Voltage	V_{SS}−0.8		V_{SS}+0.8	Vdc	
I_{IN}	Input Leakage Current R/W, $\overline{\text{Reset}}$, RS0, RS1, CS0, $\overline{\text{CS2}}$, CS1, CA1, CB1, Enable		1.0	2.5	μAdc	V_{IN}=0 to 5.25 Vdc
I_{TSI}	Three State (Off State) Input Current D0-D7, PB0-PB7, CB2		2.0	10	μAdc	V_{IN}=0.4 to 2.4 Vdc
I_{IH}	Input High Current PA0-PA7, CA2	−200	−400		μAdc	V_{IH}=2.4Vdc
I_{IL}	Input Low Current PA0-PA7, CA2		−1.3	−2.4	mAdc	V_{IL}=0.4Vdc
V_{OH}	Output High Voltage					
	D0-D7	V_{SS}+2.4			Vdc	I_{LOAD}=−205μAdc
	Other Output	V_{SS}+2.4			Vdc	I_{LOAD}=−200μAdc
V_{OL}	Output Low Voltage					
	D0-D7			V_{SS}+0.4	Vdc	I_{LOAD}=1.6mAdc
	Other Outputs			V_{SS}+0.4	Vdc	I_{LOAD}=3.2mAdc
I_{OH}	Output High Current Sourcing					
	D0-D7	−205			μAdc	V_{OH}=2.4Vdc
	Other Outputs	−100			μAdc	
	PB0-PB7, CB2	−1.0	−2.5	−10	mAdc	V_0=1.5Vdc, the current for driving other than TTL, e.g., Darlington Base
I_{LOH}	Output Leakage Current $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$		1.0	10	μAdc	V_{OH}=2.4Vdc
P_D	Power Dissipation			550	mW	
C_{IN}	Capacitance					
	D0-D7			12.5	pF	V_{IN}=0, T_A=+25°C, f=1.0MHz
	PA0-PA7, PB0-PB7, CA2, CB2			10	pF	
	Enable, R/W, $\overline{\text{Reset}}$, RS0, RS1, CS0, CS1, $\overline{\text{CS2}}$, CA1, CB1			7.5	pF	
C_{OUT}	$\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$			5.0	pF	

Note: The PA0-PA7 Peripheral Data lines and the CA2 Peripheral Control line can drive two standard TTL loads. In the input mode, the internal pullup resistor on these lines represents a maximum of 1.5 standard TTL loads.

A.C. (Dynamic Characteristics

Loading = 30pF and one TTL load for PA0-PA7, PB0-PB7, CA2, CB2
= 130pF and one TTL load for D0-D7, $\overline{IRQA}$, $\overline{IRQB}$
(V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C unless otherwise noted.)

Read Timing Characteristics (Figure 1)

Timing Characteristics (V_{CC} = 5.0V ±5%, V_{SS} = 0, T_A = 0°C to +70°C unless otherwise noted.)

Symbol	Parameter	Min.	Max.	Units	Conditions
t_{PDSU}	Peripheral Data Setup Time	90		ns	
t_{PDH}	Peripheral Data Hold Time	0		ns	
t_{CA2}	Delay Time, Enable Negative Transition to CA2 Negative Transition		0.4	μs	
t_{RS1}	Delay Time, Enable Negative Transition to CA2 Positive Transition		0.4	μs	
t_r, t_f	Rise and Fall Times for CA1 and CA2 Input Signals		1.0	μs	
t_{RS2}	Delay Time from CA1 Active Transition to CA2 Positive Transition		0.85	μs	
t_{PDW}	Delay Time, Enable Negative Transition to Peripheral Data Valid		0.4	μs	
t_{CMOS}	Delay Time, Enable Negative Transition to Peripheral CMOS PA0-PA7, CA2 Data Valid		0.85	μs	V_{CC}−30% V_{CC}; Figure 6, Load C
t_{CB2}	Delay Time, Enable Positive Transition to CB2 Negative Transition		0.4	μs	
t_{DC}	Delay Time, Peripheral Data Valid to CB2 Negative Transition	2.0		ns	
t_{RS1}	Delay Time, Enable Positive Transition to CB2 Positive Transition		0.4	μs	
PW_{CT}	Peripheral Control Output Pulse Width, CA2/CB2	550		ns	
t_r, t_f	Rise and Fall Times for CB1 and CB2 Input Signals		1.0	μs	
t_{RS2}	Delay Time, CB1 Active Transition to CB2 Positive Transition		0.85	μs	
t_{IR}	Interrupt Release Time, $\overline{IRQA}$ and $\overline{IRQB}$		0.70	μs	
t_{RS3}	Interrupt Response Time		1.0	μs	
PW_I	Interrupt Input Pulse Width	500		ns	
t_{RL}	Reset Low Time*	0.4		μs	

*The Reset line must be high a minimum of 1.0μs before addressing the PIA.

Bus Timing Characteristics

(V_{CC}=5.0V ±5%, T_A=0°C to +70°C unless otherwise noted.)

Read

Symbol	Parameter	Min.	Max.	Units
$t_{CYC(E)}$	Enable Cycle Time	0.4		μs
PW_{EH}	Enable Pulse Width, High	0.18		μs
PW_{EL}	Enable Pulse Width, Low	0.18		ns
t_{AS}	Setup Time, Address and R/W to Enable Positive Transition	55		ns
t_{DDR}	Data Delay Time		160	ns
t_H	Data Hold Time	10		ns
t_{AH}	Address Hold Time	10		ns
t_{Er}, t_{Ef}	Rise and Fall Time for Enable Input		25	ns

Write

Symbol	Parameter	Min.	Max.	Units
$t_{CYC(E)}$	Enable Cycle Time	0.4		μs
PW_{EH}	Enable Pulse Width, High	0.18		μs
PW_{EL}	Enable Pulse Width, Low	0.18		ns
t_{AS}	Setup Time, Address and R/W to Enable Positive Transition	55		ns
t_{DSW}	Data Setup Time	50		ns
t_H	Data Hold Time	10		ns
t_{AH}	Address Hold Time	10		ns
t_{Er}, t_{Ef}	Rise and Fall Time for Enable Input		25	ns

Figure 1. Peripheral Data Setup Time (Read Mode)

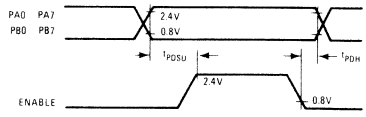
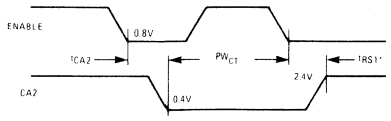


Figure 2. CA2 Delay Time (Read Mode; CRA-5=CRA-351, CRA-4=0)



*Assumes part was deselected during the previous E pulse.

Figure 3. CA2 Delay Time (Read Mode; CRA-5 = 1, CRA-3 = CRA-4 = 0)

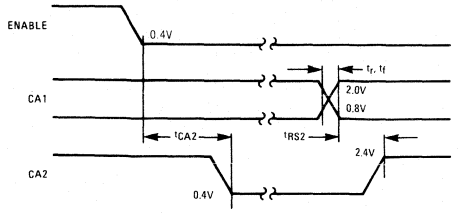


Figure 4. Peripheral CMOS Data Delay Times (Write Mode; CRA-5 = CRA-3 = 1, CRA-4 = 0)

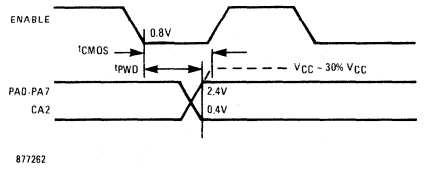
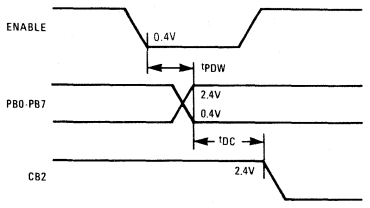
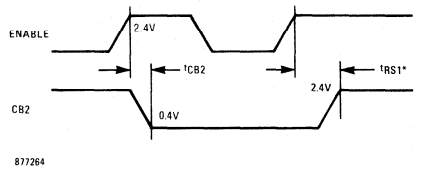


Figure 5. Peripheral Data and CB2 Delay Times (Write Mode; CRB-5 = CRB-3 = 1, CRB-4 = 0)



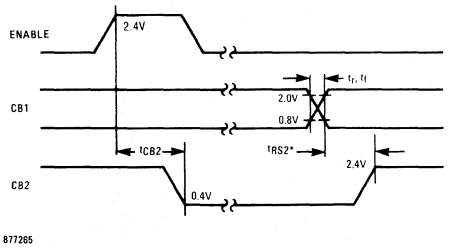
CB2 Note:
CB2 goes low as a result of the positive transition of Enable.

Figure 6. CB2 Delay Time (Write Mode; CRB-5 = CRB-3 = 1, CRB-4 = 0)



*Assumes part was deselected during the previous E pulse.

Figure 7. CB2 Delay Time (Write Mode; CRB-5 = 1, CRB-3 = CRB-4 = 0)



*Assumes part was deselected during any previous E pulse.

Figure 8. $\overline{IRQ}$ Release Time

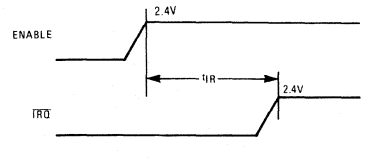
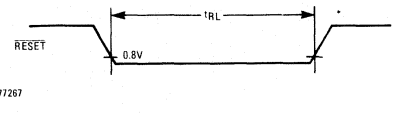


Figure 9. $\overline{RESET}$ Low Time



*The $\overline{Reset}$ line must be a V_{IH} for a minimum of 1.0μs before addressing the PIA.

Figure 10. Bus Read Timing Characteristics (Read Information from PIA)

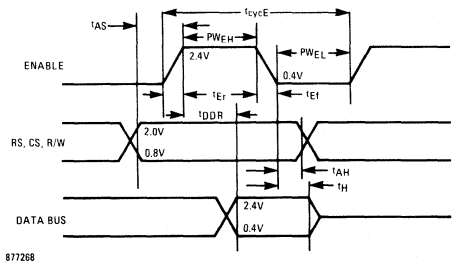


Figure 11. Bus Write Timing Characteristics (Write Information into PIA)

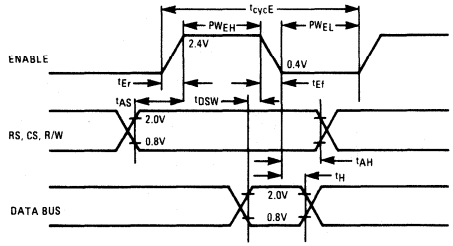


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Figure 12. Peripheral Data Hold Time (Read Mode)

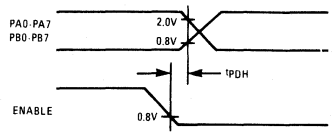

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Figure 13. Peripheral Control Output Pulse Width

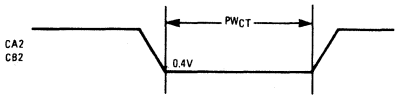

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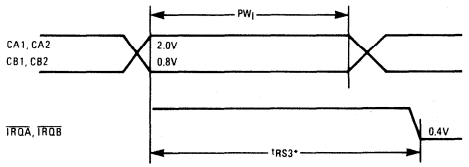
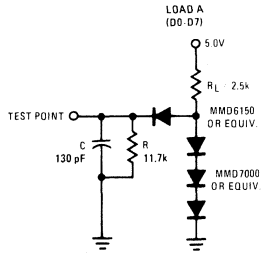
Figure 14. Interrupt Pulse Width and $\overline{IRQ}$ Response

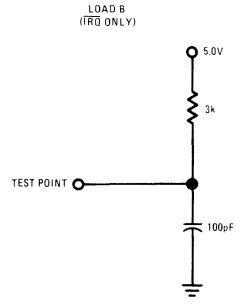


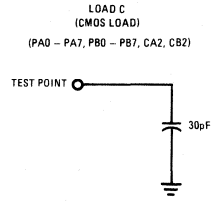
877272

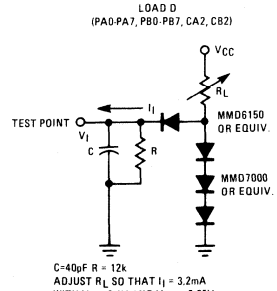
*Assumes Interrupt Enable Bits are set.

Figure 15. Bus Timing Test Loads









877257

PROGRAMMABLE TIMER

Features

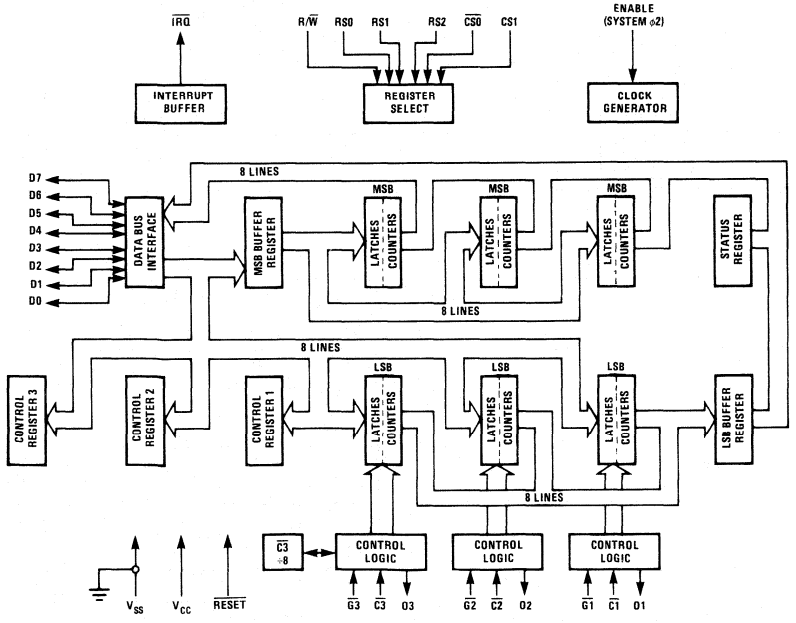
- ☐ Operates from a Single 5 Volt Supply
- ☐ Fully TTL Compatible
- ☐ Single System Clock Required (Enable)
- ☐ Selectable Prescaler on Time 3 Capable of 4MHz for the S6840, 6MHz for the S68A40 and 8MHz for the S68B40
- ☐ Programmable Interrupts ($\overline{IRQ}$) Output to MPU
- ☐ Readable Down Counter Indicates Counts to Go to Time-Out
- ☐ Selectable Gating for Frequency or Pulse-Width Comparison
- ☐ $\overline{RESET}$ Input
- ☐ Three Asynchronous External Clock and Gate/Trigger Inputs Internally Synchronized
- ☐ Three Maskable Outputs

General Description

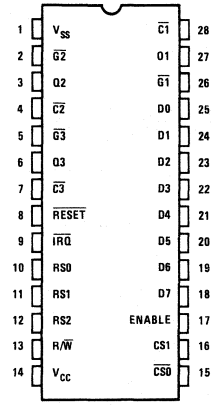
The S6840 is a programmable subsystem component of the S6800 family designed to provide variable system time intervals.

The S6840 has three 16-bit binary counters, three corresponding control registers and a status register. These counters are under software control and may be used to cause system interrupts and/or generate output signals. The S6840 may be utilized for such tasks as frequency measurements, event counting, interval measuring and similar tasks. The device may be used for square wave generation, gated delay signals, single pulses of controlled duration, and pulse width modulation as well as system interrupts.

Block Diagram



Pin Configuration



Absolute Maximum Ratings

Supply Voltage V_{CC}	−0.3 to +7.0V
Input Voltage V_{IN}	−0.3 to +7.0V
Operating Temperature Range T_A	0° to +70°C
Storage Temperature Range T_{stg}	−55° to +150°C
Thermal Resistance θ_{JA}	82.5°C/W

Note:
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Electrical Characteristics

V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = 0°C to +70°C unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{IH}	Input High Voltage	V_{SS}+2.0		V_{CC}	V	
V_{IL}	Input Low Voltage	V_{SS}−0.3		V_{SS}+0.8	V	
I_{IN}	Input Leakage Current		1.0	2.5	μA	V_{IN}=0 to 5.25 V
I_{TSI}	Three State (Off State) Input Current D0-D7		2.0	10	μA	V_{IN}=0.4 to 2.4 V
V_{OH}	Output High Voltage D0-D7 Other Outputs	 V_{SS}+2.4 V_{SS}+2.4			 V V	 I_{LOAD}=−205μA I_{LOAD}=−200μA
V_{OL}	Output Low Voltage D0-D7 01−03, $\overline{IRQ}$			 V_{SS}+0.4 V_{SS}+0.4	 V V	 I_{LOAD}=1.6mA I_{LOAD}=3.2mA
I_{LOH}	Output Leakage Current (Off State) $\overline{IRQ}$		1.0	10	μA	V_{OH}=2.4V
P_D	Power Dissipation			550	mW	
C_{IN}	Capacitance D0-D7 All Others			 12.5 7.5	 pF	 V_{IN}=0, T_A=+25°C, f=1.0MHz
C_{OUT}	$\overline{IRQ}$ 01, 02, 03			5.0 10	pF	V_{IN}=0, T_A=+25°C, f=1.0MHz

Bus Timing Characteristics

Read (See Figure 1)

Symbol	Characteristic	S6840 Min.	S6840 Max.	S68A40 Min.	S68A40 Max.	S68B40 Min.	S68B40 Max.	Unit
t_{CYCE}	Enable Cycle Time	1.0	10	0.666	10	0.5	10	μs
PW_{EH}	Enable Pulse Width, High	0.45	4.5	0.280	4.5	0.22	4.5	μs
PW_{EL}	Enable Pulse Width, Low	0.43		0.280		0.21		μs
t_{AS}	Setup Time, Address and R/W Valid to Enable Positive Transition	160		140		70		ns
t_{DDR}	Data Delay Time		320		220		180	ns
t_H	Data Hold Time	10		10		10		ns
t_{AH}	Address Hold Time	10		10		10		ns
t_{Er}, t_{Ef}	Rise and Fall Time for Enable Input		25		25		25	ns

Bus Timing Characteristics (Continued)

Read (See Figure 1)

Symbol	Characteristic	S6840 Min.	S6840 Max.	S68A40 Min.	S68A40 Max.	S68B40 Min.	S68B40 Max.	Unit
t_{CYCE}	Enable Cycle Time	1.0	10	0.666	10	0.5	10	μs
PW_{EH}	Enable Pulse Width, High	0.45	4.5	0.280	4.5	0.22	4.5	μs
PW_{EL}	Enable Pulse Width, Low	0.43		0.280		0.21		μs
t_{AS}	Setup Time, Address and R/W Valid to Enable Positive Transition	160		140		70		ns
t_{DSW}	Data Setup Time	195		80		60		ns
t_H	Data Hold Time	10		10		10		ns
t_{AH}	Address Hold Time	10		10		10		ns
t_{Er}, t_{Ef}	Rise and Fall Time for Enable Input		25		25		25	ns

AC Operating Characteristics

(See Figures 3 and 7)

Symbol	Characteristic	S6840 Min.	S6840 Max.	S68A40 Min.	S68A40 Max.	S68B40 Min.	S68B40 Max.	Unit
t_r, t_f	Input Rise and Fall Times (Figures 4 and 5) $\overline{C}$, $\overline{G}$ and $\overline{Reset}$		1.0		0.666*		0.500*	μs
PW_L	Input Pulse Width (Figure 4) (Asynchronous Mode) $\overline{C}$, $\overline{G}$ and $\overline{Reset}$	$t_{CYCE}+t_{su}+t_{hd}$		$t_{CYCE}+t_{su}+t_{hd}$		$t_{CYCE}+t_{su}+t_{hd}$		ns
PW_H	Input Pulse Width (Figure 5) (Asynchronous Mode) $\overline{C}$, $\overline{G}$ and $\overline{Reset}$	$t_{CYCE}+t_{su}+t_{hd}$		$t_{CYCE}+t_{su}+t_{hd}$		$t_{CYCE}+t_{su}+t_{hd}$		ns
t_{su}	Input Setup Time (Figure 6) (Synchronous Mode) $\overline{C}$, $\overline{G}$ and $\overline{Reset}$ $\overline{C3}$ (÷8 Prescaler Mode only)	200		120		75		ns
t_{hd}	Input Hold Time (Figure 6) (Synchronous Mode) $\overline{C}$, $\overline{G}$ and $\overline{Reset}$ $\overline{C3}$ (÷8 Prescaler Mode only)	50		50		50		ns
PW_L, PW_H	Input Pulse Width (Synchronous Mode) $\overline{C3}$ (÷8 Prescaler Mode only)	125		84		62.5		ns
	Output Delay, O1-O3 (Figure 7)							
t_{co}	(V_{OH}=2.4V, Load B) TTL		700		460		340	ns
t_{cm}	(V_{OH}=2.4V, Load D) MOS		450		450		340	ns
t_{cmos}	(V_{OH}=0.7 V_{DD}, Load D) CMOS		2.0		1.35		1.0	μs
t_{IR}	Interrupt Release Time		1.2		0.9		0.7	μs

* t_r and $t_f \leq t_{CYCE}$

Figure 1. Bus Read Timing Characteristics (Read Information from PTM)

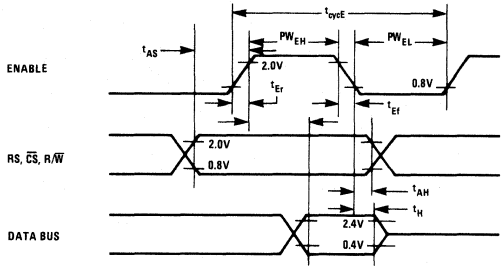


Figure 2. Bus Write Timing Characteristics (Write Information into PTM)

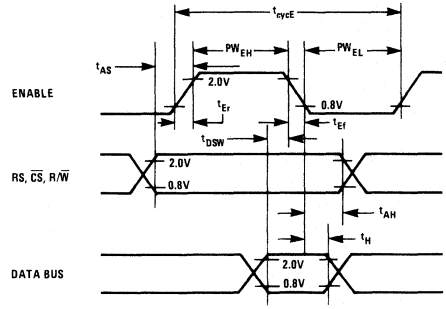


Figure 3. Input Pulse Width Low

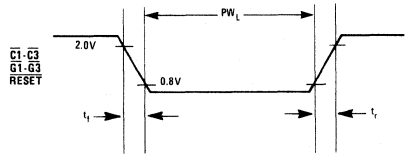


Figure 4. Input Pulse Width High

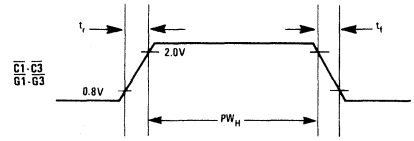


Figure 5. Input Setup and Hold Times

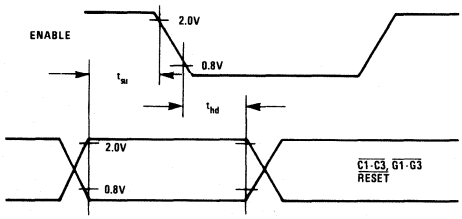


Figure 6. Output Delay

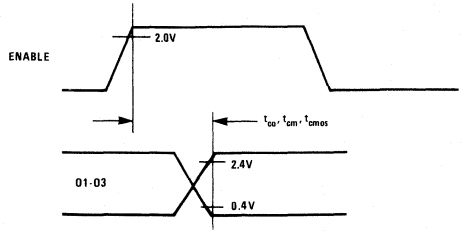


Figure 7. $\overline{IRQ}$ Release Time

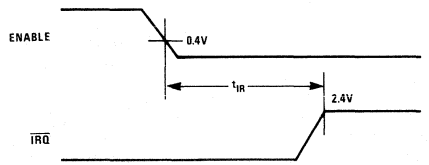
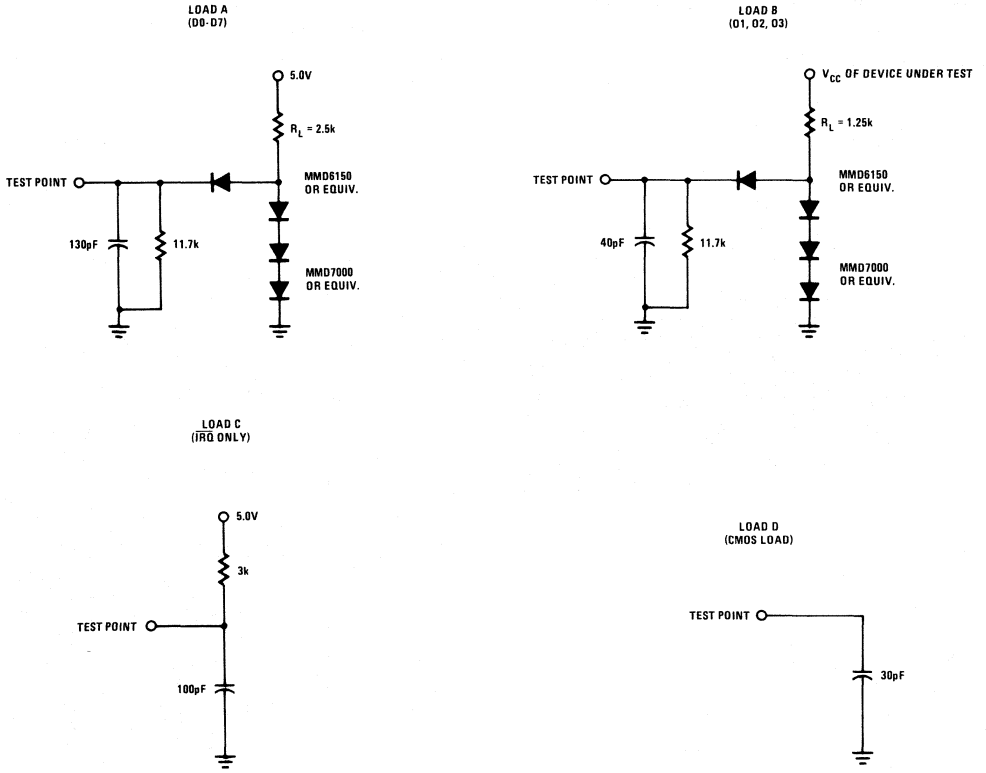


Figure 8. Bus Timing Test Loads



AMERICAN MICROSYSTEMS, INC.

PRELIMINARY DATA SHEET

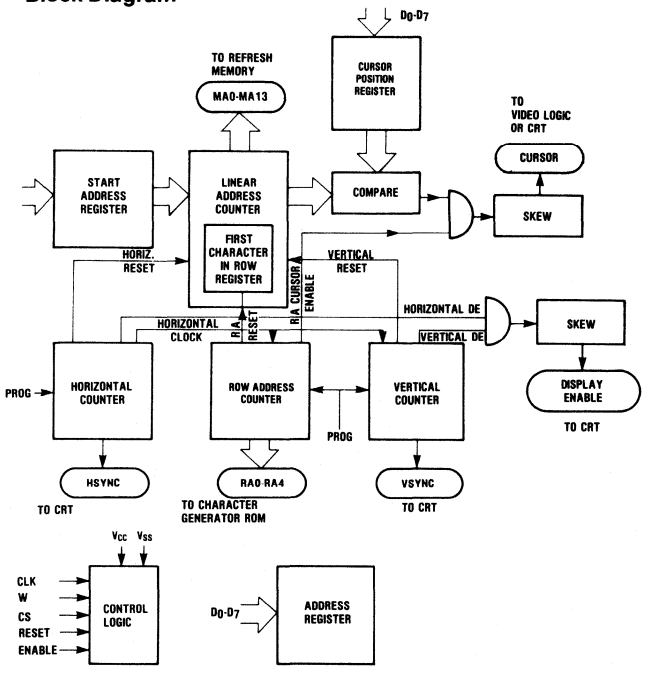
S68045

CRT CONTROLLER (CRTC)

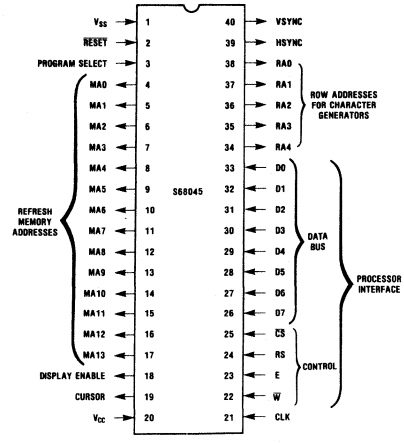
Features

- ☐ Generates Refresh Addresses and Row Selects
- ☐ Generates Video Monitor Inputs: Horizontal and Vertical Sync and Display Enable
- ☐ Low Cost; MC6845/SY6545 Pin Compatible
- ☐ Text Can Be Scrolled on a Character, Line or Page Basis
- ☐ Addresses 16K Bytes of Memory
- ☐ Screen Can Be Up to 128 Characters Tall By 256 Wide
- ☐ Character Font Can Be 32 Lines High With Any Width
- ☐ Two Complete ROM Programs
- ☐ Cursor and/or Display Can Be Delayed 0, 1 or 2 Clock Cycles
- ☐ Four Cursor Modes:
  - Non-Blink
  - Slow Blink
  - Fast Blink
  - Reverse Video With Addition of a Single TTL Gate
- ☐ Three Interlace Modes
  - Normal Sync
  - Interlace Sync
  - Interlace Sync and Video
- ☐ Full Hardware Scrolling
- ☐ NMOS Silicon Gate Technology
- ☐ TTL-Compatible, Single +5 Volt Supply

Block Diagram



Pin Configuration



General Description

The S68045 CRT Controller performs the complex interface between an S6800 Family microprocessor and a raster scan display CRT system. The S68045 is designed to be flexible yet low cost. It is configured to both simplify the development and reduce the cost of equipment such as intelligent terminals, word processing, and information display devices.

The CRT Controller consists of both horizontal and vertical counting circuits, a linear address counter, and control registers. The horizontal and vertical counting circuits generate the Display Enable, HSYNC, VSYNC, and RA0-RA4 signals. The RA0-RA4 lines are scan line count signals to the external character generator ROM. The number of characters per character row, scan lines per character row, character rows per screen, and the horizontal and vertical SYNC position and width are all mask programmable. The S68045 is capable of addressing 16K of memory for display. The CRT may be scrolled or paged through the entire display memory under MPU control. The cursor control register determines the cursor location on the screen, and the cursor format can be programmed for fast blink, slow-blink, or non-blink appearance, with programmable size. By adding a single TTL gate, the cursor can even be reversed video. The device features two complete, independent programs implemented in user-specified ROM. Either set of programmable variables (50/60Hz refresh rate, screen format, etc.) is available to the user at any time.

The S68045 is pin compatible with the MC6845, operates from a single 5-volt supply, and is designed using the latest in minimum-geometry NMOS technology.

Absolute Maximum Ratings

Supply Voltage V_{CC}	−0.3°C to +7.0°C
Input Voltage V_{IN}	−0.3V to +7.0V
Operating Temperature Range T_A	0°C to +70°C
Storage Temperature Range T_{stg}	−55°C to +150°C

Bus Timing Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{CYCE}	Enable Cycle Time	1.0			μs	
PW_{EH}	Enable Pulse Width, High	0.45		25	μs	
PW_{EL}	Enable Pulse Width, Low	0.43			μs	
t_{AS}	Setup Time, CS and RS Valid to Enable Positive Transition	160			ns	
t_H	Data Hold Time	10			ns	
t_{AH}	Address Hold Time	10			ns	
t_{Er}, t_{Ef}	Rise and Fall for Enable Input			25	ns	
t_{DSW}	Data Setup Time	195			ns	

Electrical Characteristics

V_{CC}=5.0V±5%; V_{SS}=0, T_A=0°C to +70°C unless otherwise noted

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{IH}	Input High Voltage	2.0		V_{CC}	Vdc	
V_{IL}	Input Low Voltage	−0.3		0.8	Vdc	
I_{IN}	Input Leakage Current		1.0	2.5	μAdc	
V_{OH}	Output High Voltage	2.4			Vdc	I_{LOAD}=−100μA
V_{OL}	Ouput Low Voltage			0.4	Vdc	I_{LOAD}=1.6mA
P_D	Power Dissipation		600		mW	
C_{IN}	Input Capacitance D0-D7 All Others			12.5 10	pF pF	
C_{OUT}	Output Capacitance All Outputs			10	pF	
P_{WCL}	Minimum Clock Pulse Width, Low	160			ns	
P_{WCH}	Clock Pulse Width, High	200		10,000	ns	
f_c	Clock Frequency			2.5	MHz	
t_{cr}, t_{cf}	Rise and Fall Time for Clock Input			20	ns	
t_{MAD}	Memory Address Delay Time			200	ns	
t_{RAD}	Raster Address Delay Time			200	ns	
t_{DTD}	Display Timing Delay Time			300	ns	
t_{HSD}	Horizontal Sync Delay Time			300	ns	
t_{VSD}	Vertical Sync Delay Time			300	ns	
t_{CDD}	Cursor Display Timing Delay Time			300	ns	

Systems Operation

The S68045 CRTC generates all of the signals needed for the proper operation of a CRT system including HSYNC, VSYNC, Display Enable, Cursor control signals (refer to Figure 1), the refresh memory addresses (MA0-MA13) and row addresses (RA0-RA4). The CRTC's timing is derived from the CLK input, which is divided down from the dot rate counter.

The CRTC, which is compatible with the 6800 family, communicates with the MPU by means of the standard 8-bit data bus. This primary data bus uses a buffered interface for writing information to the display refresh RAM by means of a separate secondary data bus. This arrangement allows the MPU to forget about the display except for those time periods when data is actually being changed on the screen. The address bus for the refresh RAM is continuously multiplexed between the MPU and the CRTC.

Since the MPU is allowed transparent read/write access to the display memory, the refresh RAM appears as just another RAM to the processor. This means that the refresh memory can also be used for program storage. Care should be taken by the system designer, however, to insure that the portion of memory being used for program storage is not actively displayed.

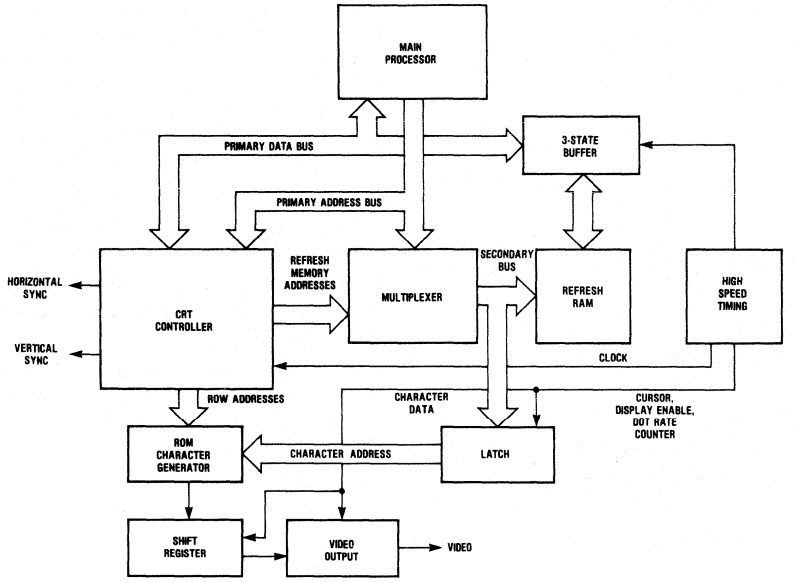
Displayed Data Control

Display Refresh Memory Addresses (MA0-MA13) — 14 bits of address provide the CRTC with access of up to 16K of memory for use in refreshing the screen.

Row Addresses (RA0-RA4) — 5 bits of data that provide the output from the CRTC to the character generator ROM. They allow up to 32 scan lines to be included in a character.

Cursor — This TTL compatible, active high output indicates to external logic that the cursor is being displayed.

Figure 1. Typical CRT Controller System



The character address of the cursor is held in a register, so the cursor's position is not lost even when scrolled off the screen.

CRT Control

All three CRT control signals are TTL compatible, active high outputs.

Display Enable — Indicates that valid data is being clocked to the CRT for the active display area.

Vertical Sync (VSYNC) — Makes certain the CRTC and the CRT's vertical timing are synchronized so the picture is vertically stable.

Horizontal Sync (HSYNC) — Makes certain the CRTC and the CRT's horizontal timing are synchronized so the picture is horizontally stable.

Processor Interface

All processor interface lines are three state, TTL/MOS compatible inputs.

Chip Select ($\overline{CS}$)—The $\overline{CS}$ line selects the CRTC when low to write to the internal Register File. This signal should only be active when there is a valid stable address being decoded from the processor.

Register Select — The RS line selects either the Address Register (RS="0") or one of the Data Registers (RS="1") of the internal Register File.

To address one of the software programmable registers (R12, R13, R14 or R15 in Table 2) first access the Address Register ($\overline{CS}$=0, RS=0) and write the number of the desired register. Then write into the actual register by addressing the data register section ($\overline{CS}$=0, RS=1) and enter the appropriate data.

Write ($\overline{W}$) — The $\overline{W}$ line allows a write to the internal Register File.

Data Bus (D0-D7) — The data bus lines (D0-D7) are write-only and allow data transfers to the CRTC internal register file.

Enable (E) — The Enable signal enables the data bus input buffers and clocks data to the CRTC. This signal is usually derived from the processor clock, and the high to low transition is the active edge.

S68045 Control Clock (CLK) — The clock signal is a high impedance, TTL/MOS compatible input which assures the CRTC is synchronized with the CRT itself. The CLK signal is divided down by external circuitry from the dot rate counter. The CLK frequency is equal to

the dot rate frequency divided by the width of a single character block (including framing) expressed in dots, CLK is equal to the character rate.

Program (PROG) — The voltage on this pin determines whether the screen format in ROM 0 (PROG LOW) or ROM 1 (PROG HIGH) is being used.

Reset ($\overline{RES}$) — The $\overline{RES}$ input resets the CRTC. An (active) low input on this line forces these actions:

a) MA0-MA13 are loaded with the contents of R12/R13 (the start address register).

b) The horizontal, vertical, and raster address counter are reset to the first raster line of the first displayed character in the first row.

c) All other outputs go low.

Note that none of the internal registers are affected by $\overline{RES}$.

$\overline{RES}$ on the CRTC differs from the reset for the rest of the 6800 family in the following aspects:

a) MA0-MA13 and RA0-RA4 go to the start addresses, instead of FFFF.

b) Display recommences immediately after $\overline{RES}$ goes high.

Internal Register Description — There is a bank of 15 control registers in the 68045, most of which are mask programmed. The exceptions are the Address Register, the two Start Address Registers (R12 & R13) and the Cursor Location Registers (R14 & R15). All software programmable registers are write only. The Address Register is 5 bits long. The software programmable registers are made available to the data lines whenever the chip select ($\overline{CS}$) goes low. When $\overline{CS}$ goes high, the data lines show a high impedance to the microprocessor.

Horizontal Total Register (R0) — The full horizontal period, expressed in character times, is masked in R0. (See Figure 2a.)

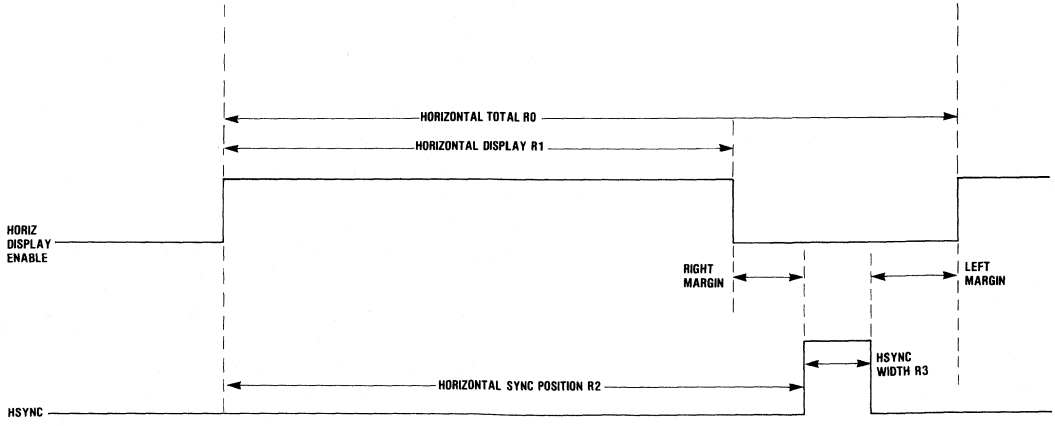
Horizontal Displayed Register (R1) — This register contains the number of characters to be actually displayed in a row. (See Figure 2a.)

Horizontal SYNC Position Register (R2) — The contents of R2 (also in character times) should be slightly larger than the value in R1 to allow for a non-displayed right border. (See Figure 2a.)

Sync Width Register (R3) — The width of the HSYNC pulse expressed in character times is masked into the lower four bits of R3. The width of the HSYNC pulse has to be non-zero.

The width of the VSYNC pulse is masked into the upper

Figure 2a. Approximate Timing Diagram



FOR MORE EXACT DIAGRAMS REFER TO THE BACK OF THE DATA SHEET. THE HORIZONTAL DISPLAY ENABLE IS ANDED WITH THE VERTICAL DISPLAY ENABLE TO PRODUCE THE DISPLAY ENABLE AT PIN 18. NOTE THE (a) FIGURE IS TIMED IN TERMS OF INDIVIDUAL CHARACTERS, WHEREAS THE (b) FIGURE IS TIMED IN TERMS OF CHARACTER ROWS.

four bits of R3 without any modification, with the exception that all zeroes will make VSYNC 16 characters wide.

Vertical Total Register (R4) — This register contains the total number of character rows — both displayed and non-displayed — per screen. This number is just the total number of scan lines used divided by the number of scan lines in a character row. If there is a remainder, it is placed in R5. (See Figure 2b).

Vertical Total Adjust Register (R5) — See description of R4. A fractional number of character row times is used to obtain a refresh rate which is exactly 50HZ, 60HZ, or some other desired frequency. (See Figure 2b).

Vertical Displayed Register (R6) — This register contains the total number of character rows that are actually displayed on the CRT screen. (See Figure 2b).

Vertical SYNC Position (R7) — R7 contains the position of the vertical SYNC pulse in character row times with respect to the top character row. Increasing the value shifts the data up. (See Figure 2b).

Interlace Mode Register (R8) — R8 controls which of the three available raster scan modes will be used (See Figure 3).

- Non-interlace or Normal sync mode
- Interlaced sync mode
- Interlaced sync and Video mode

The Cursor and Display Enable outputs can be delayed (skewed) 0, 1 or 2 clock cycles with respect to the refresh memory address outputs (MA0-MA13). The amount the cursor is delayed is independent of how much the Display Enable signal is delayed. This feature allows the system designer to account for memory address propagation delay through the RAM, ROM, etc.

Maximum Scan Line Register (R9) — Determines the number of scan lines per character row including top and bottom spacing.

Cursor Start Register (R10) — Contains the raster line where the cursor start (see Figure 4). The cursor start line can be anywhere from line 0 to line 31.

The cursor can be in one of the following formats.

- Non-blinking
- Slow blinking (1/16) the vertical refresh rate)
- Fast blinking (1/32 the vertical refresh rate)
- Reverse video (non-blinking, slow blinking, or fast blinking)

The reverse video cursor needs an external TTL XOR gate to be placed in the video circuit.

To implement the reverse video cursor, the cursor start line (R10) should be set to line 0 and the cursor end line (R11) should be set to whatever is in R9 so that the cursor covers the entire block. On the circuit level, the output from the Cursor pin (pin 19) should be taken through the XOR gate along with the output from the shift register. (See Figure 5.) With this setup the character whose memory address is in the cursor register (R14/R15) will have it's background high (because Cursor along is high) but the character itself will be off (because both cursor and the character are both high.

Figure 2b. Approximate Timing Diagram

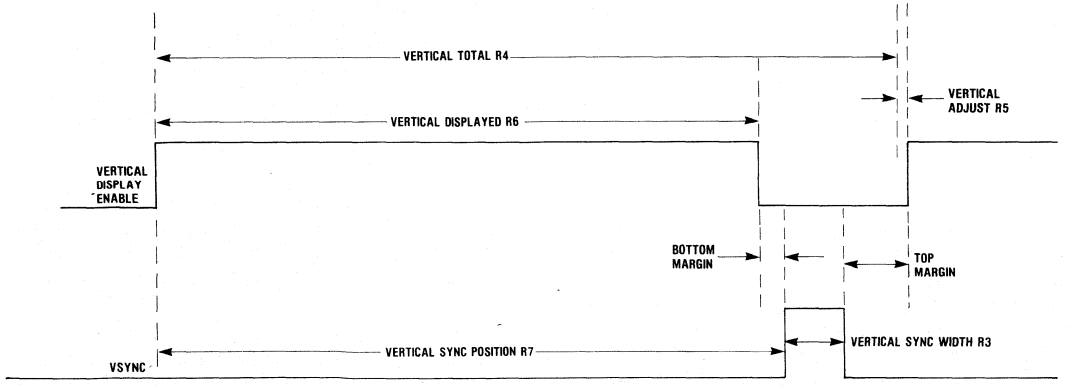


Figure 3. Interface Control

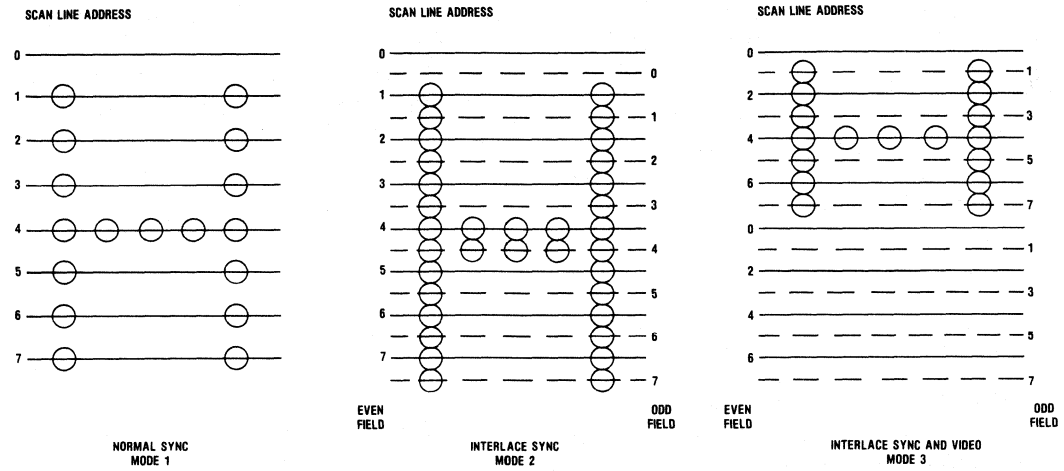
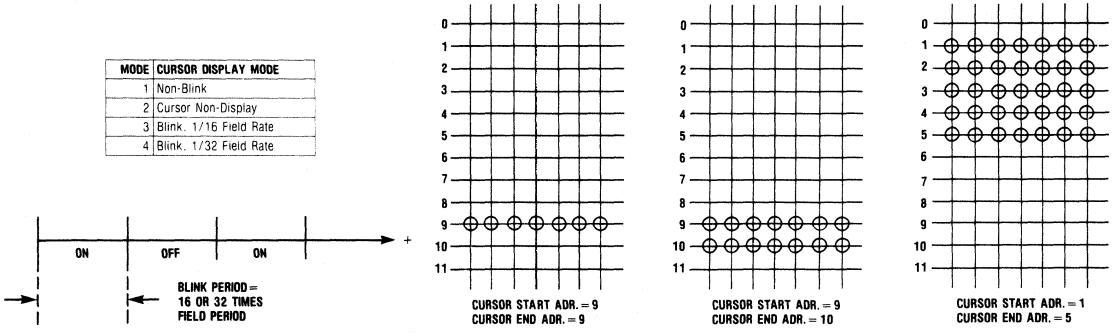


Figure 4. Cursor Control

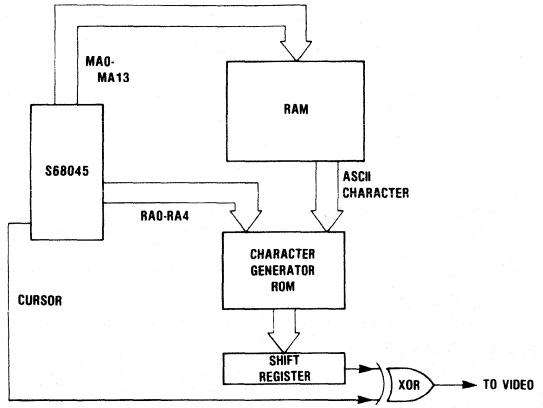
MODE	CURSOR DISPLAY MODE
1	Non-Blink
2	Cursor Non-Display
3	Blink. 1/16 Field Rate
4	Blink. 1/32 Field Rate



Memory Start Address Register (R12/R13) — These two software programmable, write-only registers taken together contain the memory address of the first character displayed on the screen. Register R12 contains the upper six bits of the fourteen refresh memory address bits, while R13 contains the lower eight bits. The Linear Address Generator begins counting from the address in R12/R13. By changing the starting address, the display can be scrolled up or down through the 16K memory block by character, line or page. If the value in R12/R13 is near the end of the 16K block the display will wrap around to the front.

Cursor Address Register (R14/R15) — These two software programmable, write-only registers, taken together, contain the address in memory of the cursor character.

Figure 5. Implementation of a Reversed Video Cursor



Register R14 contains the upper six bits and register R15 contains the lower eight bits of the character. Cursor position is associated with an address in memory rather than with a position on the screen. This way cursor position is not lost when the display is scrolled.

Address Register — The five bit address register is unique in that it does not store any CRT-related information, but is used as the address storage register in an indirect access of the other registers. When the Register Select pin (RS) is low, the address register is accessed by D0-D4. When RS is high, the register whose address is in the address register is accessed.

CRTC Internal Description

There are four counters which determine what the CRTC's output will be (see Block Diagram):

1) Horizontal Counter
2) Vertical Counter
3) Row Address Counter
4) Linear Address Counter

The first two counters, and to some extent the third, take care of the physical operation of the monitor. The Linear Address Counter, on the other hand, is responsible for the data that is displayed on the screen.

Surrounding these counters are the registers R0-R15. Coincidence logic continuously compares the contents of each counter with the contents of the register(s) associated with it. When a match is found, appropriate action is taken; the counter is reset to a fixed or dynamic value, or a flag (such as VSYNC) is set, or both.

Two sets of registers — The start Address Register (R12/R13) and the Cursor Position Register (R14/R15) — are programmable via the Data lines (D0-D7). The other registers are all mask programmed. There are two ROM programs available on each chip. Selection of which ROM program will be accessed is performed by the PROG pin.

Horizontal Counter

The Horizontal Counter produces four output flags: HSYNC, Horizontal Display Enable, Horizontal Reset to the Linear Address Counter, and the horizontal clock.

The Horizontal Counter is driven by the character rate clock, which was derived from the dot rate clock (see Table 1). Immediately after the valid display area is entered the Horizontal Counter is reset to zero but continues incrementing.

HSYNC is the only one of the four signals which is fed to an external device (the CRT). The Horizontal Counter is compared to registers R0, R2 and R3 to give an HSYNC of the desired frequency (R0), position (R2) and width (R3). (See Figure 2a.)

Horizontal Display Enable is an internal flag which, when ANDed with Vertical DE, is output at the Display Enable pin. The Horizontal Counter determines the proper frequency (R0), and width (R1).

The Horizontal Reset and the horizontal clock are actually identical signals: the only difference is the way they are used. Both are pulsed once for each scan line, so their frequency is equal to the character rate clock frequency divided by the entire horizontal period (display, non-display and retrace) expressed in character times

Table 1. Comparison of all CRTC Clocks

NAME	LOCATION OF CLOCK	DIVIDED BY:	CONTROLLING REGISTER	PRODUCES
DOT RATE CLOCK	EXTERNAL	TOTAL WIDTH OF A CHARACTER BLOCK IN DOTS	EXTERNAL	CHARACTER RATE CLOCK
CHARACTER RATE CLOCK	EXTERNAL INPUT	TOTAL NUMBER OF CHARACTERS IN A ROW	R0	HORIZONTAL CLOCK
HORIZONTAL CLOCK	INTERNAL	TOTAL NUMBER OF SCAN LINES IN A CHARACTER ROW	R9	ROW ADDRESS CLOCK
ROW ADDRESS CLOCK	INTERNAL	TOTAL NUMBER OF CHARACTER ROWS PER SCREEN	R4, R5	VERTICAL CLOCK

Table 2. CRTC Internal Register Assignment

$\overline{CS}$	RS	ADDRESS REGISTER 4	3	2	1	0	REGISTER#	REGISTER FILE
MASK PROGRAMMABLE							R0	HORIZONTAL TOTAL
							R1	HORIZONTAL DISPLAYED
							R2	HORIZONTAL SYNC POSITION
							R3	HORIZONTAL SYNC WIDTH
							R4	VERTICAL TOTAL
							R5	VERTICAL TOTAL ADJUST
							R6	VERTICAL DISPLAYED
							R7	VERTICAL SYNC POSITION
							R8	INTERLACE MODE
							R9	MAX SCAN LINE ADDRESS
							R10	CURSOR START
							R11	CURSOR END
0	1	0	1	1	0	0	R12	START ADDRESS (H)
0	1	0	1	1	0	1	R13	START ADDRESS (L)
0	1	0	1	1	1	0	R14	CURSOR (H)
0	1	0	1	1	1	1	R15	CURSOR (L)
0	0	X	X	X	X	X	X	ADDRESS REGISTER

X DON'T CARE

(which is stored in R0). The horizontal clock drives the Vertical and Row address Counters. The horizontal reset is discussed with the Linear Address Counter.

Vertical Counter

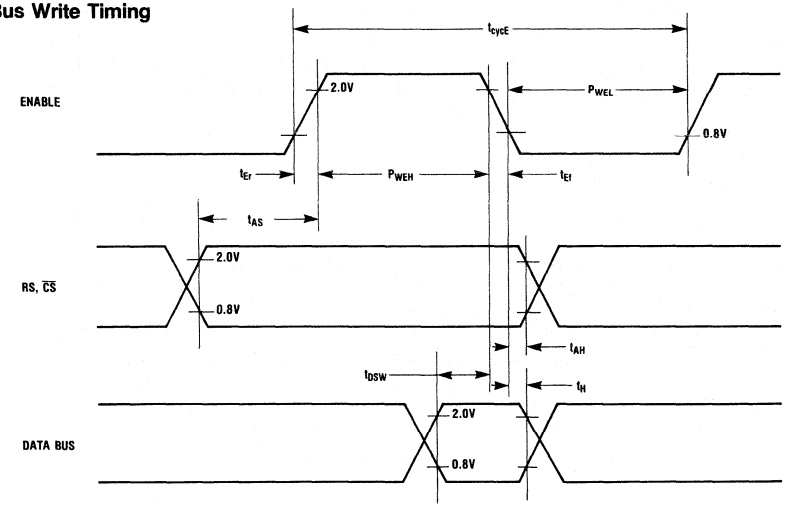
The Vertical Counter produces three output flags: VSYNC, Vertical Display Enable, and Vertical Reset to the Linear Address Counter. The Vertical Counter is driven by the horizontal clock. Immediately after vertical retrace the Vertical Counter is reset to zero but continues incrementing.

VSYNC is the only one of the three signals which is fed to an external device (the CRT). The Vertical Counter is compared to registers R3, R4, R5 and R7 to give a VSYNC of the desired frequency (R4, R5), position (R7) and width (R3). (See Figure 2b.)

Vertical Display Enable is an internal flag which, when ANDed with Horizontal DE, is output at the Display Enable pin. The Vertical Counter determines the proper frequency (R4, R5) and width (R6).

Vertical Reset is pulsed once for each screen. The frequency of Vertical Reset is equal to the horizontal clock frequency divided by the total number of scan lines in a screen (which is equal to (R4×R9)+R5). It will be discussed with the Linear Address Counter.

Figure 6. Bus Write Timing



Row Address Counter

The Row Address Counter produces three sets of output: the five Row Address lines (RA0-RA4), the Row Address Cursor Enable flag and the Row Address Reset flag. The Row Address Counter is driven by the horizontal clock. Immediately after a full character row has been completed by the Row Address Counter is reset to zero but continues incrementing. Note that the Row Address Counter actually counts scan lines, which are different from character rows. A full character row consists of however many scan lines are in register R9.

The Row Address Lines, RA0-RA4, are the only data lines from the Row Address Counter that are fed to an external device (the character generator ROM). The Row Address lines just carry the count that is currently in the Row Address Counter. The counter is reset whenever the count equals the contents of the Maximum Scan Line Register (R9.)

Row Address Cursor Enable is a flag going to the Cursor output AND gate. The Row Address Cursor Enable flag goes high whenever the count in the Row Address Counter is greater than or equal to the Cursor Start Register (R10) but less than or equal to the Cursor End Register (R11). The other input to the Cursor output AND gate goes high whenever the address in the Linear Address Counter is equal to the address in the Cursor Position Reister (R14/R15).

Row Address Reset is pulsed whenever the Row Address Counter is reset. It will be discussed with the Linear Address Counter.

Linear Address Counter

The Linear Address Counter (LAC) produces only one set of outputs: The Refresh Memory Address lines (MA0-MA13). These fourteen bits are fed externally to the Refresh RAM and internally to the Cursor Position coincidence circuit. The LAC is driven by the character rate clock and continuously increments during the display, non-display and retrace portions of the screen. It contains an internal read/write register which stores the memory address of the first displayed character in the current row.

When any of the three Reset flags already mentioned (Horizontal, Row Address and Vertical) is pulsed, the value in the internal register is loaded into the counter. If the reset is a Horizontal Reset the value in the internal register is not modified before the load. If the reset is a Row Address Reset, the value in the internal "first character" register is first increased by the number of characters displayed on a single character row (register

R1). The new contents of the internal register are then loaded into the Linear Address Counter.

If the reset is a Vertical Reset, the value in Start Address Register (R12/R13) is first loaded into the internal register, and then into the Linear Address Counter.

The fourteen output lines allow 16K of memory to be accessed. By incrementing or decrementing the number in the Start Address Register, the screen can be scrolled forward or backward through Display Refresh RAM on a character, line, or page basis.

Figure 7. Bus Timing Character

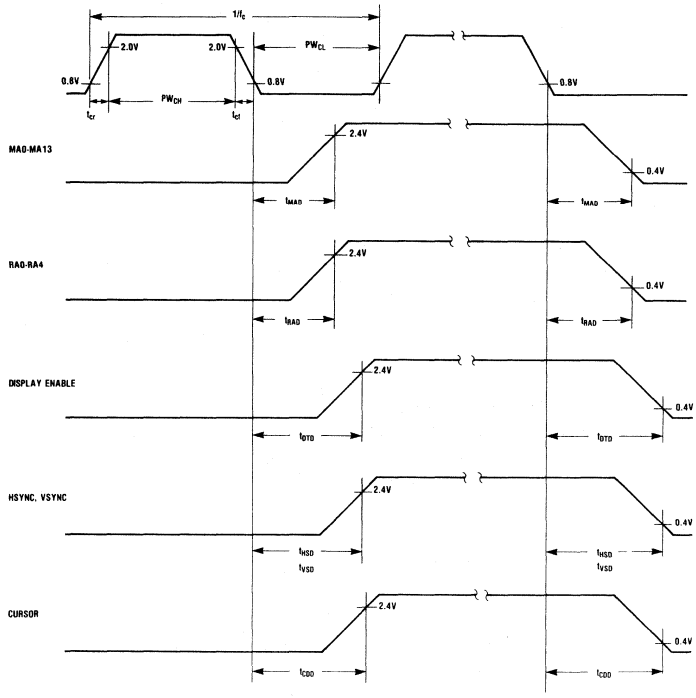
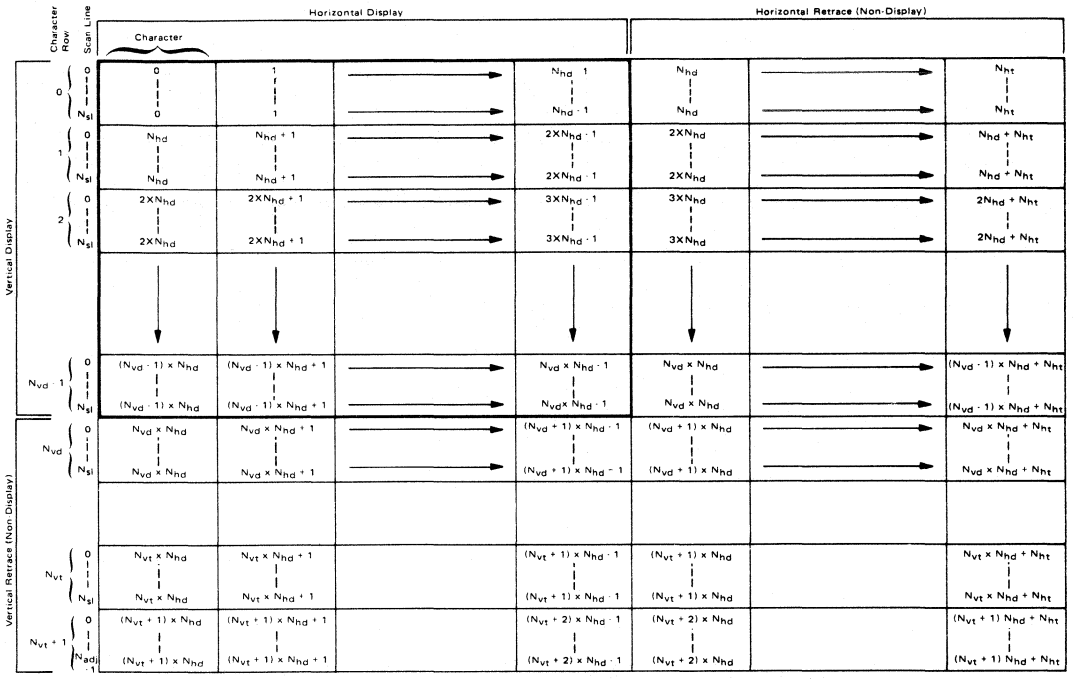
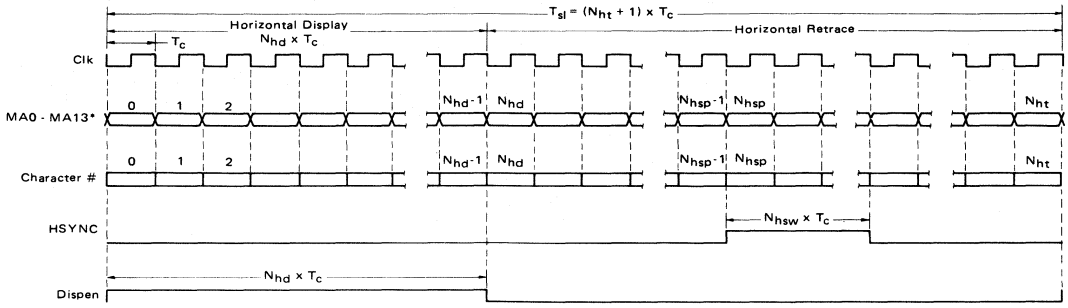


Figure 8. Refresh Memory Addressing (MA0-MA13) State Chart



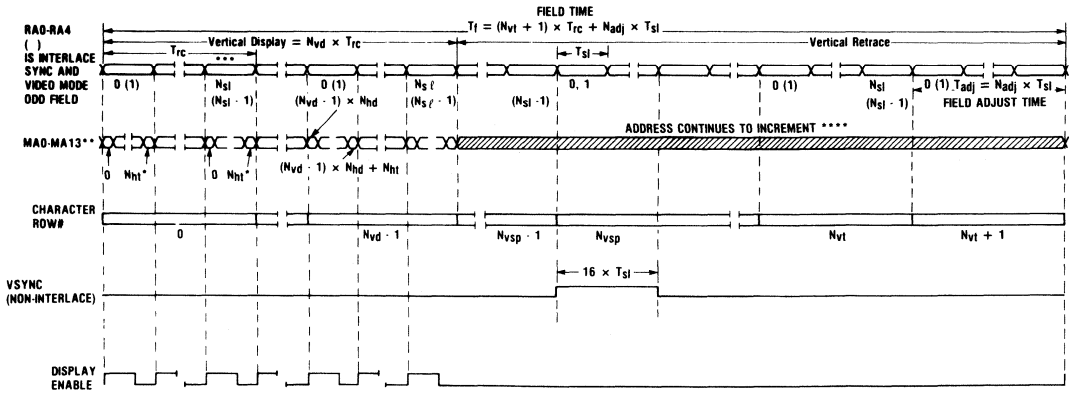
NOTE 1 The initial MA is determined by the contents of start address register, R12/R13. Timing is shown for R12/R13 = 0. Only Non-Interlace and Interlace Sync Modes are shown.

Figure 9. CRTC Horizontal Timing



*Timing is shown for first displayed scan row only. See Chart in Figure 16 for other rows. The initial MA is determined by the contents of Start Address Register, R12/R13. Timing is shown for R12/R13 = 0.

Figure 10. CRTC Vertical Timing

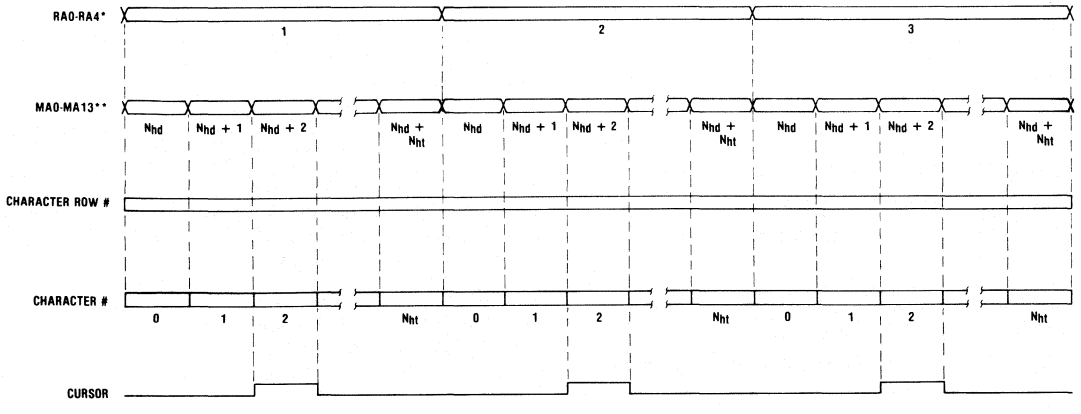


* N_{ht} - there must be an even number of character times for both interlace modes.

** Initial MA is determined by R12/R13 (Start Address Register), which is zero in this timing example.

*** N_{ht} must be an even number of scan lines for Interlace Sync and Video Mode.

Figure 11. Cursor Timing



* Timing is shown for non-interlace and interlace sync modes.
Example shown has cursor programmed as:
Cursor Register = N_{hd} + 2
Cursor Start = 1
Cursor End = 3

** The initial MA is determined by the contents of Start Address Register, R12/R13. Timing is shown for R12/R13 = 0.

AMERICAN MICROSYSTEMS, INC.

S6846

ROM-I/O-TIMER

Features

- 2048x8-Bit Bytes of Mask-Programmable ROM
- 8-Bit Bidirectional Data Port for Parallel Interface Plus Two Control Lines
- Programmable Interval Timer-Counter Functions
- Programmable I/O Peripheral Data, Control and Direction Registers
- Compatible with the Complete S6800 Microcomputer Product Family
- TTL-Compatible Data and Peripheral Lines
- Single 5 Volt Power Supply

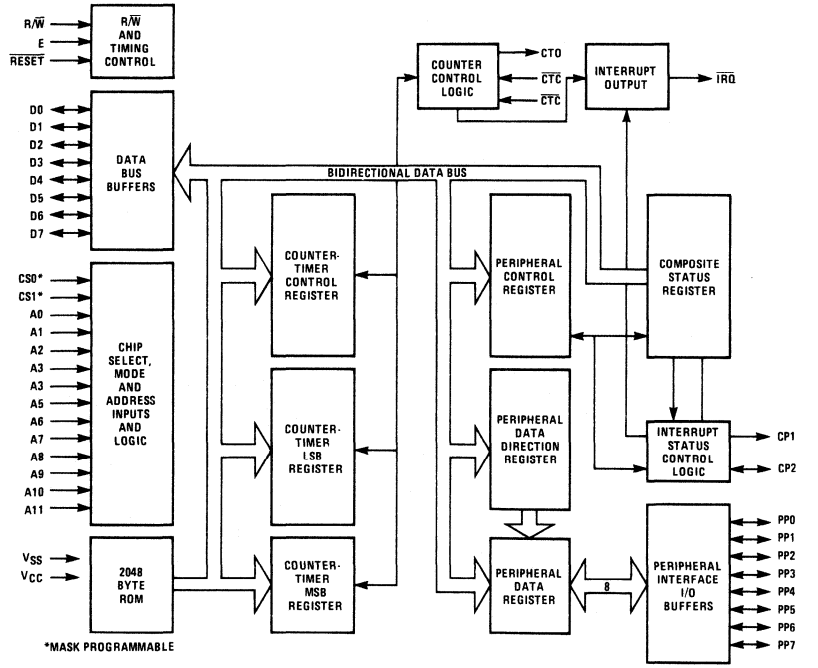
General Description

The S6846 combination chip provides the means, in conjunction with the S6802, to develop a basic 2-chip microcomputer system. The S6846 consists of 2048 bytes of mask-programmable ROM, an 8-bit bidirectional data port with control lines, and a 16-bit programmable timer-counter.

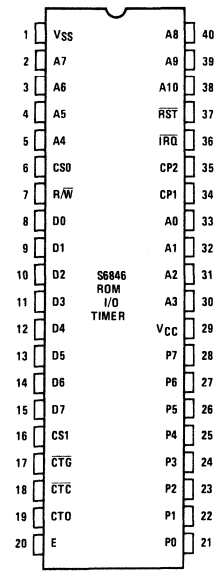
This device is capable of interfacing with the S6802 (basic S6800, clock and 128 bytes of RAM) as well as the S6800 if desired. No external logic is required to interface with most peripheral devices.

The S6846 combination chip may be partitioned into three functional operating sections: programmed storage, timer-counter functions, and a parallel I/O port.

Block Diagram



Pin Configuration



General Description (Continued)

Programmed Storage

The mask-programmable ROM section is similar to other AMI ROM products. The ROM is organized in a 2048 by 8-bit array to provide read only storage for a minimum microcomputer system. Two mask-programmable chip selects are available for user definition.

Address inputs A0-A10 allow any of the 2048 bytes of ROM to be uniquely addressed. Internal registers associated with the I/O functions may be selected with A0, A1 and A2. Bidirectional data lines (D0-D7) allow the transfer of data between the MPU and the S6846.

Timer-Counter Functions

Under software control this 16-bit binary counter may be programmed to count events, measure frequencies and time intervals, or similar tasks. It may also be used for square wave generation, single pulses of controlled duration, and gated delayed signals. Interrupts may be generated from a number of conditions selectable by software programming.

The timer-counter control register allows control of the interrupt enables, output enables, and selection of an internal or external clock source. Input pin $\overline{CTC}$ (counter-timer clock) will accept an asynchronous pulse to be used as a clock to decrement the internal register for the counter-timer. If the divide-by-8 prescaler is used, the maximum clock rate can be four times the master clock frequency with a maximum of 4 MHz. Gate input ($\overline{CTG}$) accepts an asynchronous TTL-compatible signal which may be used as a trigger or gating function to the counter-timer. A counter-timer output ($\overline{CTO}$) is also available and is under software control via selected bits in the timer-counter control register. This mode of operation is dependent on the control register, the gate input, and the external clock.

Parallel I/O Port

The parallel bidirectional I/O port has functional operational characteristics similar to the B port on the S6821 PIA. This includes 8 bidirectional data lines and two handshake control signals. The control and operation of these lines are completely software programmable.

The interrupt input (CP1) will set the interrupt flags of the peripheral control register. The peripheral control (CP2) may be programmed to act as an interrupt input or as a peripheral control output.

Figure 1. Typical Microcomputer

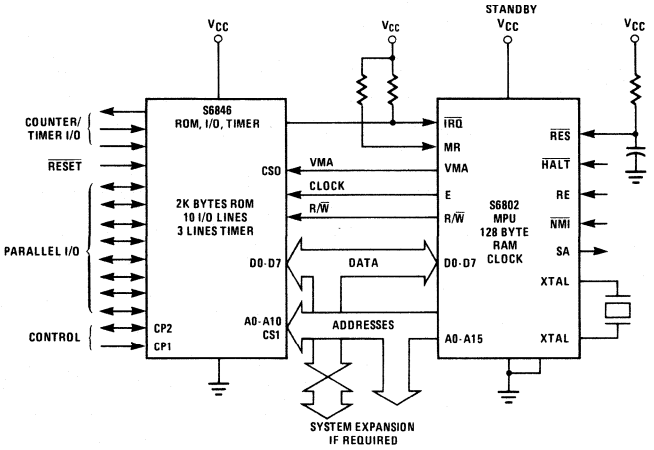


Figure 1 is a block diagram of a typical cost effective microcomputer. The MPU is the center of the microcomputer system and is shown in a minimum system interfacing with a ROM combination chip. It is not intended that this system be limited to this function but that it be expandable with other parts in the S6800 Microcomputer family if desired.

Absolute Maximum Ratings

Supply Voltage	-0.3Vdc to +7.0Vdc
Input Voltage	-0.3Vdc to +7.0Vdc
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	-55°C to +150°C
Thermal Resistance	70°C/W

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

Electrical Characteristics (V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = 0°C to +70°C unless otherwise noted.)

Symbol	Parameter		Min.	Typ.	Max.	Unit	Conditions
V_{IH}	Input High Voltage	All Inputs	V_{SS} + 2.0		V_{CC}	Vdc	
V_{IL}	Input Low Voltage	All Inputs	V_{SS} -0.3		V_{SS} + 0.8	Vdc	
V_{OS}	Clock Overshoot/Undershoot — Input High Level — Input Low Level		V_{CC} -0.5 V_{SS} -0.5		V_{CC} + 0.5 V_{SS} + 0.5	Vdc	
I_{in}	Input Leakage Current	R/$\overline{W}$, $\overline{Reset}$, CS0, CS1 CP1, $\overline{CTG}$, $\overline{CTC}$, E, A0-A11		1.0	2.5 100	μAdc	V_{in} = 0 to 5.25Vdc
I_{TSI}	Three-State (Off State) Input Current	D0-D7 PP0-PP7, CR2		2.0	10 100	μAdc	V_{in} 0.4 to 2.4Vdc
V_{OH}	Output High Voltage	D0-D7 CP2, PP0-PP7 Other Outputs	V_{SS} + 2.4 V_{SS} + 2.4 V_{SS} + 2.4			Vdc Vdc	I_{Load} = -205μAdc, I_{Load} = -145μAdc, I_{Load} = -100μAdc
V_{OL}	Output Low Voltage	D0-D7 Other Outputs			V_{SS} + 0.4 V_{SS} + 0.4	Vdc	I_{Load} = 1.6mAdc I_{Load} = 3.2mAdc
I_{OH}	Output High Current (Sourcing)	D0-D7 Other Outputs CP2, PP0-PP7	-205 -200 -1.0		 -10	μAdc mADC	V_{OH} = 2.4Vdc V_O = 1.5Vdc, the current for driving other than TTL, e.g., Darlington Base
I_{OL}	Output Low Current (Sinking)	D0-D7 Other Outputs	1.6 3.2			mAdc	V_{OL} = 0.4Vdc
I_{LOH}	Output Leakage Current (Off State)	$\overline{IRQ}$			10	μAdc	V_{OH} = 2.4Vdc
P_D	Power Dissipation				1000	mW	
C_{in}	Capacitance	D0-D7 PP0-PP7, CP2 A0-A10, R/$\overline{W}$, $\overline{Reset}$, CS0, CS1, CP1, $\overline{CTC}$, $\overline{CTG}$ $\overline{IRQ}$			20 12.5 10 7.5	pF	V_{in} = 0, T_A = 25°C, f = 1.0MHz
C_{out}		PP0-PP7, CP2, CTO			5.0 10	pF	
f	Frequency of Operation		0.1		1.0	MHz	
	Clock Timing						
t_{cycE}	Cycle Time		1.0			μs	
t_{RL}	Reset Low Time		2			μs	
t_{IR}	Interrupt Release				1.6	μs	

Read/Write Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
PW_{EL}	Enable Pulse Width, Low	430			ns	
PW_{EH}	Enable Pulse Width, High	430			ns	
t_{AS}	Set Up Time (Address CS0, CS1, R/W)	160			ns	
t_{DDR}	Data Delay Time			320	ns	
t_H	Data Hold Time	10			ns	
t_{AH}	Address Hold Time	10			ns	
t_{Ef}, t_{Er}	Rise and Fall Time			25	ns	
t_{DSW}	Data Set Up Time	195			ns	

Bus Timing
Peripheral I/O Lines

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{PDSU}	Peripheral Data Setup	200			ns	
t_{Pr}, t_{Pc}	Rise and Fall Times CP1, CP2			1.0	μs	
t_{CP2}	Delay Time E to CP2 Fall			1.0	μs	
t_{DC}	Delay Time I/O Data CP2 Fall	20			μs	
t_{RS1}	Delay Time E to CP2 Rise			1.0	μs	
t_{RS2}	Delay Time CP1 to CP2 Rise			2.0	μs	
t_{PDW}	Peripheral Data Delay			1.0	μs	

Timer-Counter Lines

t_{CR}, t_{CF}	Input Rise and Fall Time CTC and CTG			100	ns	
t_{PWH}	Input Pulse Width High (Asynchronous Mode)	t_{cyc} + 250			ns	
t_{PWL}	Input Pulse Width Low (Asynchronous Mode)	t_{cyc} + 250			ns	
t_{su}	Input Setup Time (Synchronous Mode)	200			ns	
t_{hd}	Input Hold Time (Synchronous Mode)	50			ns	
t_{CTO}	Output Delay			1.0	μs	

Figure 2. Bus Read Timing (Read Information from S6846)

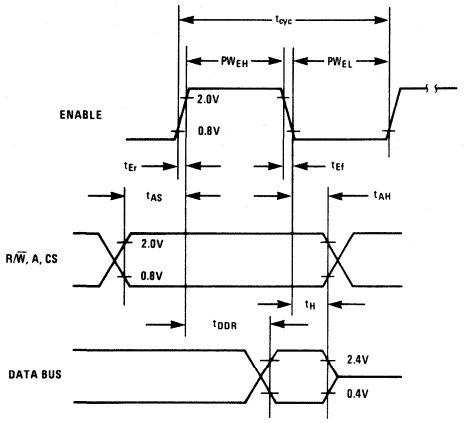


Figure 3. Bus Write Timing (Write Information from MPU)

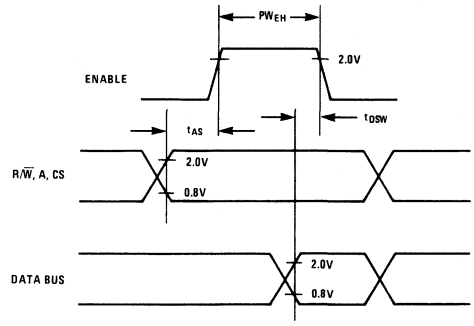


Figure 4. Peripheral Data and CP2 Delay (Control Mode PCR5 = 1, PCR4 = 0, PCR3 = 1)

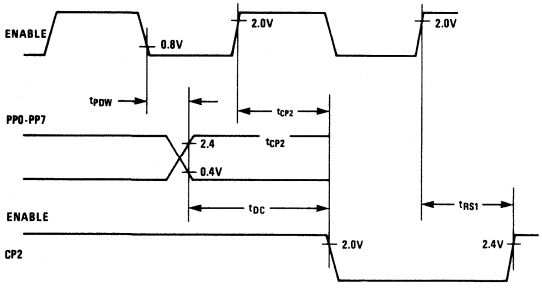


Figure 5. IRQ Release Time

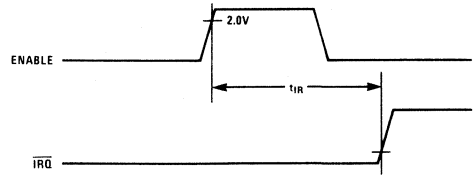


Figure 6. Peripheral Port Setup Time

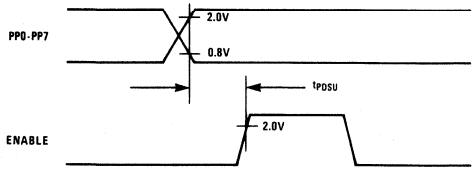


Figure 7. CP2 Delay Time (PCR5 = 1, PCR4 = 0, PCR3 = 0)

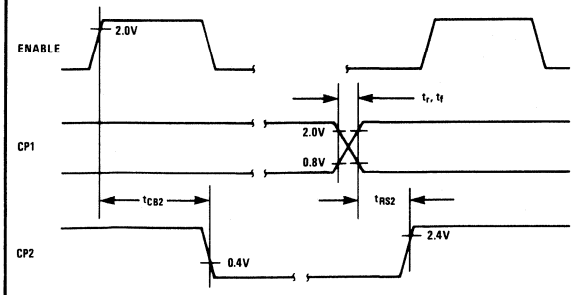


Figure 8. Input Pulse Widths

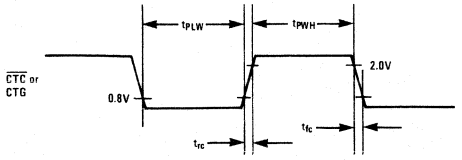
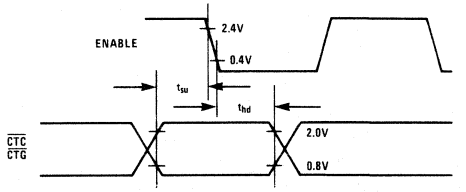


Figure 9. Input Setup and Hold Times



NOTE: This mode is valid only for synchronous operation.

Figure 10. Output Delay

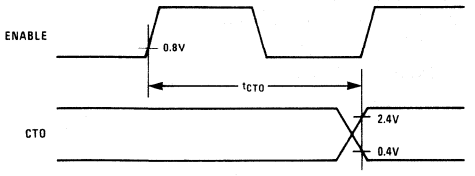
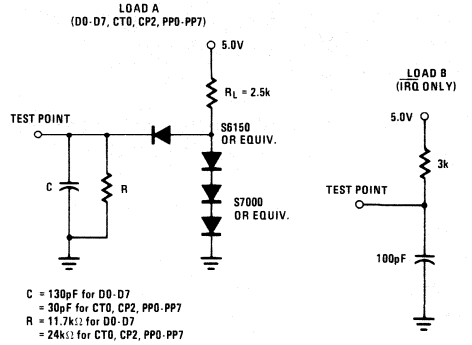


Figure 11. Bus Timing Test Loads



C = 130pF for D0-D7
= 30pF for CTO, CP2, PP0-PP7
R = 11.7kΩ for D0-D7
= 24kΩ for CTO, CP2, PP0-PP7

S6800

AMERICAN MICROSYSTEMS, INC.

S68047

VIDEO DISPLAY GENERATOR

Features

- ☐ 32 x 16 (512 total) Alphanumeric Two Color Display on Black Background with Internal or External Character Generator ROM.
- ☐ Two Semigraphics Modes with Display Densities Ranging from 64 x 32 to 64 x 48 in 8 and 4 Color Sets Respectively, plus Black.
- ☐ Full Graphics Modes with Display Densities Ranging from 64 x 64 to 256 x 192 in 2 and 4 Colors.
- ☐ Full NTSC Compatible Composite Video with Choice of Interlaced and Non-interlaced Display Versions.
- ☐ Provides Microprocessor Compatible Interface Signals.
- ☐ Generates Display Refresh RAM Addresses.
- ☐ NMOS Device, Single 5V Supply, TTL Compatible Logic Levels.
- ☐ Color Set Select Pin Can Give 8 Color Displays in Full Graphics Mode.

General Description

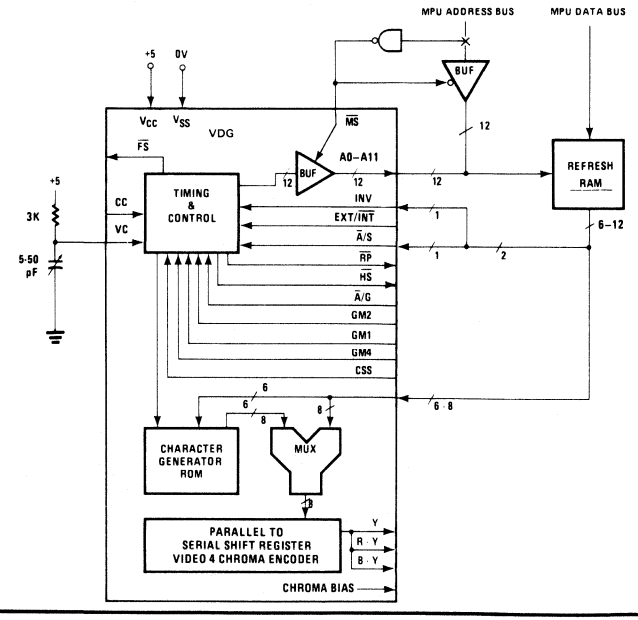
The S68047 Video Display Generator (VDG) is designed to produce composite video suitable for display on a standard American NTSC compatible black/white television or color televison or monitor.

There are three major types of display which the S68047 can generate. These include an alphanumerics mode of which there are two types, each with normal or inverted video; a semigraphics mode of which there are also two types; and full graphics mode of which there are eight types.

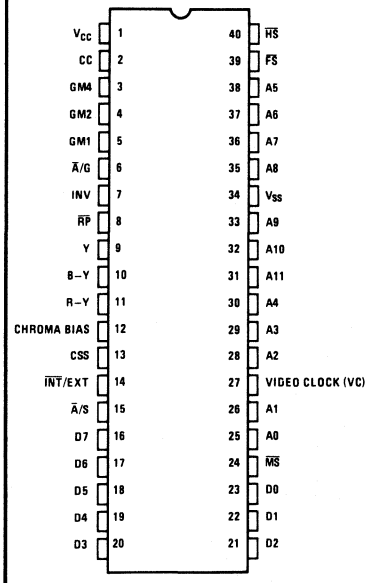
Alphanumeric Modes

The alphanumeric modes, internal and external, enable the S68047 to display a matrix of 32 x 16 (512 total) characters. The internal mode utilizes an on-chip 64 ASCII character ROM to display each character in a 5 x 7 dot matrix font. In the external alphanumeric

Block Diagram



Pin Configuration



General Description (Continued)

mode, an external memory is required, either ROM or RAM, which is used to display the 32 x 16 character matrix with each character located within an 8 x 12 dot matrix of customized font. Switching between internal and external alphanumerics modes and normal and inverted video can be accomplished on a character by character basis.

Semigraphic Modes

The two semigraphic modes, semigraphic 4 (SG4) and semigraphic 6 (SG6), subdivide each of the 512 (32 x 16) character blocks of 8 x 12 dots each into 2 x 2 and 2 x 3 smaller blocks respectively. In SG4 each block is created from 4 x 6 dots and in SG6 each block consists of 4 x 4 dots. In addition the SG4 and SG6 modes can each be displayed in 8 and 4 colors plus black.

Display switching from alphanumerics to semigraphics modes or vice versa during a raster display is called minor mode switching and can take place on a character basis.

Graphics Modes

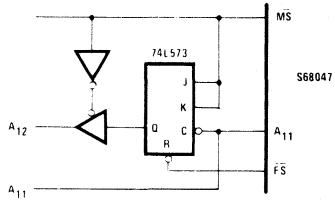
The eight full graphics modes are divided into two major groups, 4 color and 2 color. The 4 color graphics provide 4 display densities ranging from 64 x 64 for Graphics 0 through to 128 x 192 elements for Graphics 6. The 2 color graphics also provide 4 display densities ranging from 128 x 64 for Graphics 1 through to 256 x 192 elements for Graphics 7. The latter display has the highest density of the eight graphics modes. The amount of display memory increases proportionately with increasing density of display to a maximum of 6K bytes for Graphics 7. Switching between either the alphanumeric modes or semigraphics modes and any of the full graphics modes is called major mode switch ing. Major mode switching can only occur at the end of every twelfth raster line scan.

Applications

Anywhere data can be more usefully presented graphically on a CRT and for a minimum cost, the VDG in conjunction with a microprocessor based controller can utilize a standard American NTSC compatible TV or monitor for such a purpose. Applications are extremely broad ranging from educational systems, video games, small low cost business/home computers to process control monitors and medical diagnostic displays.

The different modes of operation permit various cost/display presentation tradeoffs. The alphanumerics modes allow use of the TV screen as a video teletype at the most limited level of operation. Only 512 bytes, one for each character, need to be stored, each byte being a minimum of six bits wide per the ASCII code. If video inversion switching or alpha to semigraphics switching is required per character then two extra bits are required in the display RAM as shown in Fig. 1. The semigraphics modes each offer an intermediate range of graphics densities with tradeoffs in density versus color. Typical semigraphics display capabilities are bar graphs, charts, mini displays, etc. which with minor mode switching to alphanumerics modes allow annotation or captioning of the resultant display. The various graphics modes provide greater density displays with greater freedom of display presentations. The tradeoffs in increasing density are with increasing display memory size and color versus density. A minimum Graphics 0 provides a display density of 64 x 64 (4096) elements, each element being composed of a matrix of 12 (4 x 3) dots with a selection of four colors per element. Since each of the even numbered 4 color graphics modes map two bits of the data word to one picture element, each data word of memory provides four picture elements. Thus Graphics 0 requires 4096/4 = 1024 bytes of display

Figure 1.



GRAPHICS 6 AND GRAPHICS 7 REQUIRE CK OF DISPLAY RAM, THUS THIRTEEN ADDRESS LINES. THE VDG PROVIDES A_0 A_{11}. HOWEVER A_{12} MUST BE GENERATED EXTERNALLY AS SHOWN.

Electrical Specifications

Absolute Maximum Ratings

Supply Voltage	7.0V
Input Voltage	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 150°C

RAM, Graphics 2 requires 8192/4 = 2048 and so on. Graphics 1, like all the odd numbered 2 color graphics modes, maps one bit of data word to one picture element. Each data word therefore maps eight elements. Graphics 1 density of 128 x 8 (8192) elements therefore requires 8192/8 = 1024 bytes of display RAM and Graphics 7, the densest display, requires 49, 152/8 = 6144 bytes of RAM. At the higher density graphics displays, the rate of change of elements approaches the maximum dot frequency of 6MHz. This video rate taxes the capabilities of most commercially available television sets and thus the quality of the display system (television or monitor) should be commensurate with the highest video rate to be used.

DC (Static) Characteristics (V_{CC} = 5.0V ± 5% ; T_A = 25°C, unless otherwise specified).

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{IH}	Input Voltage High	2.0		V_{CC}	V	
V_{IH}	Input Voltage High (Color Clock only)	4.0		V_{CC}	V	
V_{IL}	Input Voltage Low	-0.3		+0.6	V	
I_{IN}	Input Leakage Current (all inputs)		1.0	2.5	μA	V_{IN} = 0 - 5.25V; V_{CC} = 0V
$I_{L(TS)}$	Tri-State Output Leakage Current (A0 — A11)			10	μA	V_{CC} = 5.25V; $\overline{MS}$ = 0V; V_{IN} = 0.4 -2.4V
I_{LO}	Output Leakage Current ($\overline{HS}$, $\overline{FS}$, $\overline{RP}$)			10	μA	V_{IN} = 2.4V; V_{CC} = 0V
V_{OH}	Output Voltage High (A0 — A11, $\overline{HS}$, $\overline{FS}$, $\overline{RP}$)	2.4			V	I_{OH} = -100μA ($\overline{HS}$, $\overline{FS}$, $\overline{RP}$); 0μA (A_0 - A_{11}); CL = 30pF
V_{OL}	Output Voltage Low (A0 — A11, $\overline{HS}$, $\overline{FS}$, $\overline{RP}$)			0.4	V	I_{OL} = 1.6mA ($\overline{HS}$, $\overline{FS}$, $\overline{RP}$); 0mA (A_0 - A_{11}); CL = 30pF
I_{CC}	V_{CC} Supply Current		45		mA	V_{CC} = 5V; T_A = 25°C
C_{IN}	Input Capacitance			10	pF	V_{IN} = 0, T_A = 25°C; f = 1.0MHz
C_{OUT}	Output Capacitance			12	pF	V_{IN} = 0, T_A = 25°C; f = 1.0MHz

AC Electrical Characteristics (V_{CC} = 5.0V ± 5%; T_A = 0 - 70°C except where noted).

Alpha Internal Mode (Figure 2)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
f_{vc}	Video Clock Frequency	5.6	6.0	6.4	MHz	
t_{ch}	Character Time	1.43	1.33	1.25	μs	
t_{ACC}	Access-Time of External Refresh RAM			0.7	μs	
t_{dot}	Dot Time	178	166	156	ns	

Alpha External Mode (Figure 2)

NOTE: All parameters are the same as in Alpha Internal Mode except t_{ACC}

t_{ACC}	Access-time of Refresh RAM + Access-time of External ROM			0.7	μs	

Semigraphics Mode (Figure 2)

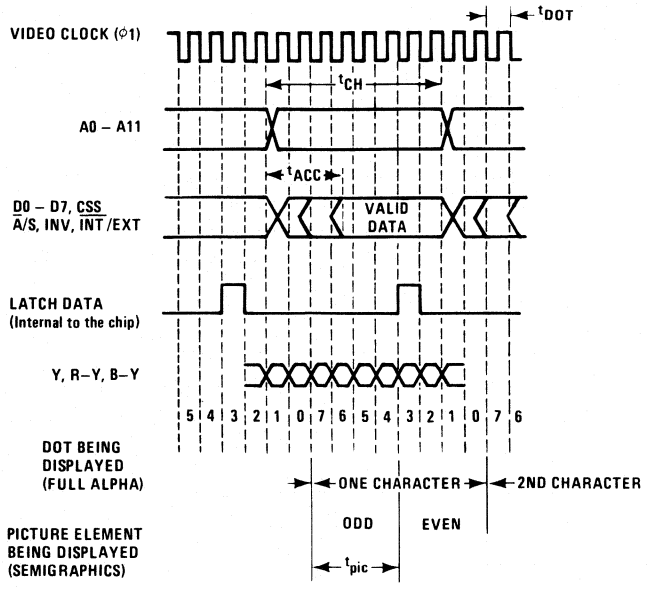
t_{pic}	Picture Element Duration	712	664	624	ns	

NOTE: All other parameters are the same as in Alpha Internal Mode.

Color Sub-carrier Input

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
f_{CC}	Frequency		3.579545 ±10 Hz		MHz	
t_r	Rise Time			10	ns	
t_f	Fall Time			10	ns	
PW_{CC}	Pulse Width		140		ns	
V_{IL}	Zero Level			0.6	V	
V_{IH}	One Level	4.0			V	
DR	Duty Ratio	40%	50%	60%		

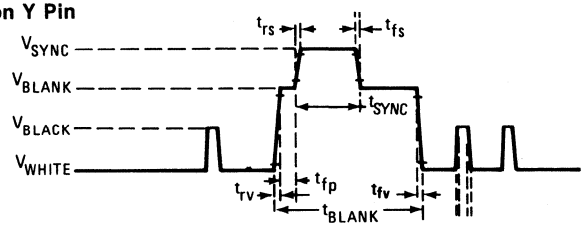
Figure 2. Refresh RAM Interface Timing



Composite Video Timing (Figure 3)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
t_{SYNC}	Sync duration		4.888889		μs	
t_{fp}	Front Porch duration		1.536508		μs	
t_{BLANK}	Horizontal Blank Duration			11.44	μs	
t_{rs}, t_{fs}	Rise time and Fall time of Horizontal Sync			250	ns	
t_{rv}, t_{fv}	Rise time and Fall time of Horizontal Blank			340	ns	

Figure 3. Composite Video Timing on Y Pin



Chroma R and Chroma B Output Timing; C_L = 10pF; 1K Load (Figure 4)

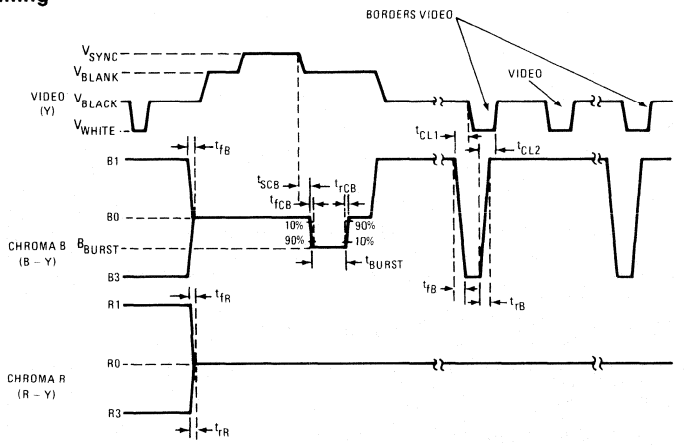
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
t_{rB}, t_{fB} t_{rR}, t_{fR}	Color Signals rise and fall time		50		ns	Load = R-Y, B-Y input of LM1889
t_{scB}	Color Burst to Sync lag		410		ns	
t_{BURST}	Color Burst Duration		2.45		μs	
t_{fcB}, t_{rcB}	Color Burst rise and fall times		175		ns	
t_{cL1}, t_{cL2}	Video to color signals lag		75		ns	

Voltage Levels

Video (Y) and Chroma (R—Y,B—Y) Output Levels (Figure 4) C_L = 10pF; Video Clock = 5.6MHz; T_A = 25°C; C_L = 10pF; Video Clock = 5.6MHz; T_A = 25°C; V_{CC} = 5V ± 5%

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{SYNC}	Sync Voltage	0	0.1	0.5	V	
V_{BLANK}	Blanking Level		1.5		V	
V_{BLACK}	Black Level		1.7		V	
V_{WHITE}	White level	2.4	4.0	V_{CC}	V	
V_{B1}, V_{R1}		2.4	4.0	V_{CC}	V	
V_{B0}, V_{R0}			2.0		V	
V_{B3}, V_{R3}		0	0.1	0.5	V	
V_{BURST}			0.4		V	
$V_{CHROMA\ BIAS}$			2.0		V	

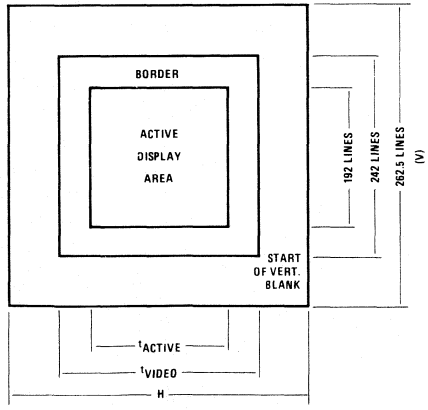
Figure 4. Chroma Timing



Video Display Format Timing (Figure 5)

Symbol	Parameter	Typ.	Units	Conditions
H	Horizontal Scan Time	63.55557	μs	
V	Field Time	16.683337	ms	
F	Frame Time	33.366674	ms	
I/V	Field Rate	59.94004	sec^{-1}	
t_{ACTIVE}	Active Display Duration	41	μs	
t_{VIDEO}	Active Display + Border Duration	52.8	μs	
t_{RP}	Row Preset Period (12 Horizontal Scans)	762.66684	μs	

Figure 5. Video Display Format



S6800

Pin Description

V_{CC}	+5V
V_{SS}	0V
CC	(Color Burst Clock 3.579545 MHz)
VC	(Video Clock Oscillator ≅ 6MHz)
A0 — A11	(Address Lines to Display Memory; high-impedance during $\overline{MS}$ low)
D0 — D5	(Data from Display Memory RAM or ROM; D4 — D6 — Color Data in Semigraphics)
D6, D7	(Data from Display Memory in GRAPHIC Mode; Data also in ALPHANUMERIC Mode; Color Data in ALPHA SEMIGRAPHIC — 6)
R — Y, B — Y, Y	(Color and Composite Video)
CHB	(Chroma Bias; References R — Y and B — Y Levels)
$\overline{RP}$	(Row Preset in any ALPHA Mode; goes low in all modes every 12 lines)
$\overline{HS}$	(Horizontal Sync)
INV	(Inverts Video in all FULL ALPHA Modes; no effect in Semigraphics or Graphics Mode)
EXT/$\overline{INT}$	(Switches to External ROM in ALPHA Mode; between SEMIG — 4 and SEMIG — 6 in Semigraphics; no effect in all Graphics Modes)
$\overline{A}$/S	(Alpha/Semigraphics: Selects between FULL ALPHA and SEMIGRAPHICS in ALPHA Modes; no effect in all Graphics Modes)
$\overline{MS}$	(Memory Select; forces VDG Address Buffers to high-impedance state; also used as a strobe in TEST and RESET functions). The TV screen is forced black when $\overline{MS}$ = low
$\overline{A}$/G	(Switches between ALPHA and GRAPHIC Modes)
$\overline{FS}$	(Field Synchronization; LOW during vertical blanking time)
CSS	(Color Set Select: Selects between two ALPHA Display Colors; between two Color Sets in SEMIGRAPHICS — 6 and FULL GRAPHICS: selects Border Color in 8 Graphic Modes)
GM1, GM2 GM4	(Graphics Mode Select; select one of eight Graphic Modes; no affect in Alpha and Semigraphic Modes; GM1, GM2 select TEST and RESET mode when $\overline{A}$/G = 0 and $\overline{MS}$ pin is strobed low)

Internal Description

Internally the VDG is the combination of four integrated subsystems (timing and control, MUX, address buffers and shift registers to form the VDG function. A block diagram of the VDG is shown on Page 1. Each subsystem is described below.

Timing and Control

The timing and control subsystem of the VDG uses the 3.58MHz color frequency to generate timing information. It accepts the color clock (generated off-chip) (CC) input and generates timing for the horizontal sync, horizontal blank, field sync, vertical blank and row preset signal ($\overline{RP}$) for external character generator ROM. The video clock is generated on-chip by external RC and generates addresses A0 — A11 to address the external refresh RAM.

The color-set-select (CSS) input to the Timing and Control subsystem of the VDG is used to determine the color-set of the display.

The EXT/$\overline{INT}$ input has two functions. In the full alphanumeric mode, it is used to select either internal ROM or external ROM. It is also used to select between semigraphic 4 and semigraphic 6 mode in semigraphic modes ($\overline{A}$/S = 1).

The INV input is utilized by the timing and control subsystem to invert the display while in full alpha mode.

Internal Description (Continued)

$\overline{A}$/G, $\overline{A}$/S, GM1, GM2, GM4 inputs to the timing and control subsystem determine which of the fourteen VDG modes is to be used (Table 1).

MUX

The MUX provides the function of selecting the data source to be displayed. The source can be either internal ROM or external ROM or RAM. For the internal alphanumeric mode, the data source is the internal ROM. For all other modes (semigraphic and graphics) the data source is external ROM/RAM.

Address Buffers

The address buffers provide the buffering required for external drive (ROM/RAM). The buffers are tri-stated when the $\overline{MS}$ pin goes low and tri-states the buffers so that VDG does not interfere with the MPU operation. The $\overline{FS}$ pin (output) from the VDG signals to the MPU that the TV is in the vertical retrace mode and the MPU can directly change the data in the display memory during that time with no interruption to displayed data.

Shift Registers

The two shift registers serialize bytes coming from internal/external ROM/RAM for conversion to data on the TV screen. The shift registers output also goes to the chroma encoder circuitry to determine the color of each individual dot. Each shift register has 4-bits.

VDG

The VDG has fourteen modes, grouped in three sets. They are:

4 Alphanumerics Modes
- ☐ Normal internal alpha
- ☐ Inverted internal alpha
- ☐ Normal external alpha
- ☐ Inverted external alpha

2 Semigraphics Modes
- ☐ Semigraphics 4
- ☐ Semigraphics 6

8 Full-graphics Modes
- ☐ 4 Graphics four-color modes
- ☐ 4 Graphics two-color modes

The six alphanumeric modes can be switched among themselves on a character-by-character basis. Switching within the six alphanumeric modes is referred to as minor-mode switching. All other mode switching is referred to as major-mode switching.

The display can be major-mode switched on after any multiple of twelve rows have been completed. This is signalled to the MPU by $\overline{RP}$ output going low. Switching among the full-graphics modes is permitted at the end of every twelfth row just as in major-mode switching.

Table 1 tabulates the modes of the VDG. The data structures for each mode are listed in Table 7. Table 2 and Table 3 show the Alpha Select Mode and Graphic Select Mode configurations respectively. Table 4 gives the Two-color Graphics and Full-alpha Color Specification. Table 5 shows the semigraphics and Four-color Graphics Color Specification.

Table 1. VDG Modes

	Mode	Description	Memory
I.	ALPHA INTERNAL	32 x 16 BOXES: 5 x 7 CHARACTER	512 x 7 – 8
II.	ALPHA INTERNAL INVERTED	IN 8 x 12 BOX	
III.	ALPHA EXTERNAL	32 x 16 BOXES: 5 x 7 OR 7 x 9 CHARACTERS	512 x 7 – 8
IV.	ALPHA EXTERNAL INVERTED	IN 8 x 12 BOX OR FULL 8 x 12 LIMITED GRAPHICS	
V.	ALPHA SEMIGRAPHICS 4	32 x 16 BOXES: 2 x 2 ELEMENTS PER BOX; EIGHT COLORS PLUS BLACK	512 x 4 – 7
VI.	ALPHA SEMIGRAPHICS 6	32 x 16 BOXES 2 x 3 ELEMENTS PER BOX; FOUR COLORS PLUS BLACK	512 x 6 – 8
VII.	GRAPHICS 0	64 x 64 ELEMENTS: FOUR COLORS PER ELEMENT	1K x 8
VIII.	GRAPHICS 1	128 x 64 ELEMENTS: TWO COLORS PER ELEMENT	1K x 8
IX.	GRAPHICS 2	128 x 64 ELEMENTS: FOUR COLORS PER ELEMENT	2K x 8
X.	GRAPHICS 3	128 x 96 ELEMENTS: TWO COLORS PER ELEMENT	1.5K x 8
XI.	GRAPHICS 4	128 x 96 ELEMENTS: FOUR COLORS PER ELEMENT	3K x 8
XII.	GRAPHICS 5	256 x 96 ELEMENTS: TWO COLORS PER ELEMENT	3K x 8
XIII.	GRAPHICS 6	128 x 192 ELEMENTS: FOUR COLORS PER ELEMENT	6K x 8
XIV.	GRAPHICS 7	256 x 192 ELEMENTS: TWO COLORS PER ELEMENT	6K x 8

Table 7. Detailed Description of VDG Model

VDG PINS								COLOR			TV SCREEN			
A/G	A/S	INT/EXT	GM4	GM2	GM1	CSS	INV	CHARACTER COLOR	BACK-GROUND	BORDER	DISPLAY MODE	DETAIL	VDG DATA BUS	COMMENTS
0	0	0	X	0	0	0	0	Green	Black	Black	32 Characters in columns 16 Characters in rows	8 DOTS, 12 DOTS, 7, 5	NOT USED, ASCII INPUT	ALPHANUMERIC INTERNAL mode uses internal character generator with on-chip 64 ASCII character ROM to display each character in 5x7 dot matrix font.
							1	Black	Green					
						1	0	Blue	Black	Black				
							1	Black	Blue					
0	0	1	X	0	0	0	0	Green	Black	Black	32 Characters in columns 16 Characters in rows		ONE ROW OF CUSTOM CHARACTERS	ALPHANUMERIC EXTERNAL mode uses external ROM or RAM to display 512 characters in custom fonts each in 8x12 dot matrix.
							1	Black	Green					
						1	0	Green	Black	Black				
							1	Black	Green					
0	1	0	X	0	0	X	X	L_X C_2 C_1 C_0 Color 0 X X X Black 1 0 0 0 Green 1 0 0 1 Yellow 1 0 1 0 Cyan 1 0 1 1 Red 1 1 0 0 Blue 1 1 0 1 Cyan/ Blue 1 1 1 0 Magenta 1 1 1 1 Orange		Black	64 Display elements in columns 32 Display elements in rows	L1 L0 / L3 L2	NOT USED, C2 C1 C0 L3 L2 L1 L0, COLOR, LUMINENCE	SEMIGRAPHICS 4 mode subdivides each of the 512 (32x16) character blocks of 8x12 dots into four equal parts. The dominance of each block is determined by the corresponding bit (L0-L3) on the VDG data bus. Color of each block is determined by 3 bits (C0-C2).
0	1	1	X	0	0	0	X	L_X C_1 C_0 0 0 0 Black 1 0 0 Green 1 0 1 Yellow 1 1 0 Cyan 1 1 1 Red 1 0 0 Blue 1 0 1 Cyan/ Blue 1 1 0 Magenta 1 1 1 Orange		Black	64 Display elements in columns 48 Display elements in rows	L1 L0 / L3 L2 / L5 L4	C1 C0 L5 L4 L3 L2 L1 L0, COLOR, LUMINENCE	SEMIGRAPHICS 6 mode subdivides each of the 512 (32x16) character blocks of 8x12 dots into six equal parts. The luminance of each part is determined by the corresponding bits (L0-L5) on the VDG bus. Color of each block is determined by 2 bits (C0, C1).
1	X	X	0	0	0	0	X	C_1 C_0 0 0 Green 0 1 Yellow 1 0 Cyan 1 1 Red 0 0 Blue 0 1 Cyan/ Blue 1 0 Magenta 1 1 Orange		Green Cyan/ Blue	64 Display elements in columns 64 Display elements in rows	E3 E2 E1 E0 WHERE EX = CYCX	C1 C0 C1 C0 C1 C0 C1 C0	GRAPHICS 0 mode uses a maximum of 1024 bytes of display RAM in which one pair of bits (C0, C1) specifies on picture element. (Ex.).
1	X	X	0	0	1	0	X	L_X 0 Color Black 1 Green		Green	128 Display elements in columns 64 Display elements in rows	L7 L6 L5 L4 L3 L2 L1 L0	L7 L6 L5 L4 L3 L2 L1 L0	GRAPHICS 1 mode uses a maximum of 1024 bytes of display RAM in which one bit (Lx) specifies one picture element.
						1		0 Black 1 Cyan/ Blue		Cyan/ Blue				
1	X	X	1	0	0	0	X	Same color as Graphics 0		Green Cyan/ Blue	128 Display elements in columns 64 Display elements in rows	E3 E2 E1 E0	C1 C0 C1 C0 C1 C0 C1 C0	GRAPHICS 2 mode uses a maximum of 2048 bytes of display RAM in which one pair of bits (C0, C1) specifies one picture element (Ex.).
						1								
1	X	X	0	1	1	0	X	Same color as Graphics 1		Green Cyan/ Blue	128 Display elements in columns 96 Display elements in rows	L7 L6 L5 L4 L3 L2 L1 L0	L7 L6 L5 L4 L3 L2 L1 L0	GRAPHICS 3 mode uses a maximum of 1536 bytes of display RAM in which one bit (Lx) specifies one picture element.
						1								
1	X	X	0	1	0	0	X	Same color as Graphics 0		Green Cyan/ Blue	128 Display elements in columns 96 Display elements in rows	E3 E2 E1 E0	C1 C0 C1 C0 C1 C0 C1 C0	GRAPHICS 4 mode uses a maximum of 3072 bytes of display RAM in which one pair of bits (C0, C1 specifies one picture element (Ex.)
						1								
1	X	X	1	0	1	0	X	Same color as Graphics 1		Green Cyan/ Blue	256 Display elements in columns 96 Display elements in rows	L7 L6 L5 L4 L3 L2 L1 L0	L7 L6 L5 L4 L3 L2 L1 L0	GRAPHICS 5 mode uses a maximum of 3072 bytes of display RAM in which one bit (Lx) specifies one picture element.
						1								
1	X	X	1	1	0	0	X	Same color as Graphics 0		Green Cyan/ Blue	128 Display elements in columns 192 Display elements in rows	E3 E2 E1 E0	C1 C0 C1 C0 C1 C0 C1 C0	GRAPHICS 6 mode uses a maximum of 6144 bytes of display RAM in which one pair of bits (C0, C1) specifies one picture element (Ex.).
						1								
1	X	X	1	1	1	0	X	Same color as Graphics 1		Green Cyan/ Blue	256 Display elements in columns 192 Display elements in rows	L7 L6 L5 L4 L3 L2 L1 L0	L7 L6 L5 L4 L3 L2 L1 L0	GRAPHICS 7 mode uses a maximum of 6144 bytes of display RAM in which one bit (Lx) specifies one picture element.
						1								

ASYNCHRONOUS COMMUNICATION INTERFACE ADAPTER (ACIA)

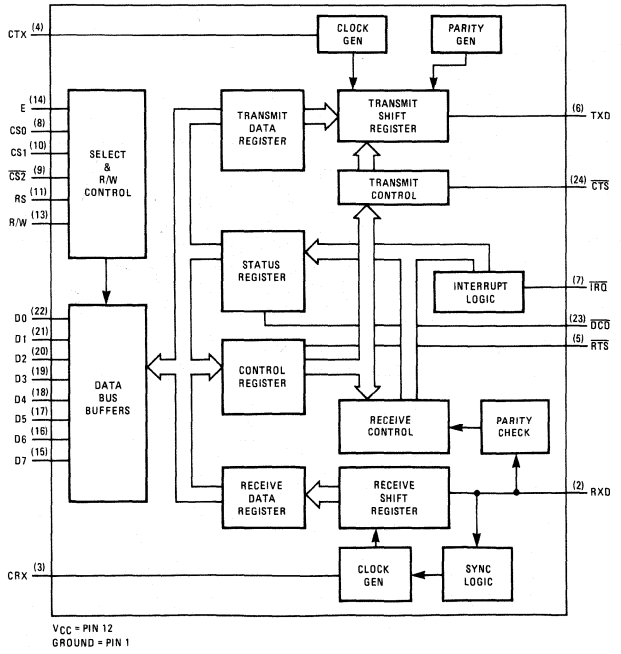
Features

- 8 Bit Bidirectional Data Bus for Communication with MPU
- False Start Bit Deletion
- Peripheral/Modem Control Functions
- Double Buffered Receiver and Transmitter
- One or Two Stop Bit Operation
- Eight and Nine-Bit Transmission with Optional Even and Odd Parity
- Parity, Overrun and Framing Error Checking
- Programmable Control Register
- Optional ÷1, ÷16, and ÷64 Clock Modes
- Up to 500,000 bps Transmission

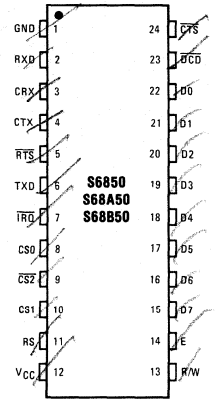
General Description

The S6850/S68A50/S68B50 Asynchronous Communications Interface Adapater (ACIA) provices the data formatting and control to interface serial asynchronous data communications to bus organized systems such as the S6800/S68A00/S68B00 Microprocessing Units.

The S6850/S68A50/S68B50 includes select enable, read/write, interrupt and bus interface logic to allow data transfer over an eight-bit bidirectional data bus. The parallel data of the bus system is serially transmitted and received by the asynchronous data interface, with proper formatting and error checking. The functional configuration of the ACIA is programmed via the data bus during system initialization. Word lengths, clock division ratios and transmit control through the Request-to-Send output may be programmed. For modem operation three control lines are provided.



Pin Configuration



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Absolute Maximum Ratings

Supply Voltage	-0.3V to +7.0V
Input Voltage	-0.3V to +7.0V
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	-55°C to +150°C

Note:
This device contains circuitry to protect the inputs against damage due to high static voltages or electrical fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Electrical Characteristics (V_{CC} = +5.0V ±5%, V_{SS} = 0, T_A = 0°C to +70°C unless otherwise noted.)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{IH}	Input High Voltage (normal operating level)	V_{SS}+2.0		V_{CC}	Vdc	
V_{IL}	Input Low Voltage (normal operating level)	V_{SS}-0.3		V_{SS}+0.8	Vdc	
I_{IN}	Input Leakage Current R/W, ES, CS0, CS1, $\overline{CS2}$, Enable		1.0	2.5	μAdc	V_{IN} = 0Vdc to 5.25Vdc
I_{TSI}	Three-State (Off State) Input Current D0-D7		2.0	10	μAdc	V_{IN} = 0.4Vdc to 2.4Vdc
V_{OH}	Output High Voltage (all outputs except IRQ)					
	D0-D7	V_{SS}+2.4			Vdc	I_{LOAD} = -205μAdc, Enable Pulse Width <25μs
	Tx Data, $\overline{RTS}$	V_{SS}+2.4			Vdc	I_{LOAD} = -100μAdc, Enable Pulse Width <25μs
V_{OL}	Output Low Voltage (Enable pulse width < 25μs)			V_{SS}+0.4	Vdc	I_{LOAD} = 1.6mAdc, Enable Pulse Width <25μs
I_{LOH}	Output Leakage Current (Off State) $\overline{IRQ}$		1.0	10	μAdc	V_{OH} = 2.4Vdc
P_D	Power Dissipation		300	525	mW	
C_{IN}	Input Capacitance					
	D0-D7		10	12.5	pF	
	E,Tx,CLK,Rx Clk,R/W,RS,Rx Data, CS0,$\overline{CS1}$,$\overline{CS2}$,RXD,CTS,$\overline{DCD}$,CTX,CRX		7.0	7.5	pF	V_{IN} = 0, T_A = 25°C, f = 1.0MHz
C_{OUT}	Output Capacitance $\overline{RTS}$,Tx Data			10	pF	
	$\overline{IRQ}$			5.0	pF	
PW_{CL}	Minimum Clock Pulse Width, Low ÷16, ÷64 Modes	600			ns	
PW_{CH}	Minimum Clock Pulse Width, High ÷16, ÷64 Modes	600			ns	
f_C	Clock Frequency ÷1 Mode			500	kHz	
	÷16, ÷64 Modes			800	kHz	
t_{TDD}	Clock-to-Data Delay for Transmitter			1.0	μs	
t_{RDSU}	Receive Data Setup Time ÷1 Mode	500			ns	
t_{RDH}	Receive Data Hold Time ÷1 Mode	500			ns	
t_{IR}	$\overline{Interrupt\ Request}$ Release Time			1.2	μs	
t_{RTS}	$\overline{Request\text{-}to\text{-}Send}$ Delay Time			1.0	μs	
t_r,t_f	Input Transition Times (Except Enable)			1.0*	μs	

*1.0μ or 10% of the pulse width, whichever is smaller.

Bus Timing Characteristics (V_{CC} = +5.0V ±5%, V_{SS} = 0, T_A = 0°C to +70°C unless otherwise noted.)

Read

Symbol	Characteristic	S6850		S68A50		S68B50		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYCF}	Enable Cycle Time	1.0		0.666		0.50		μs
PW_{EH}	Enable Pulse Width, High	0.45		0.28		0.22	25	μs
PW_{EL}	Enable Pulse Width, Low	0.43		0.28		0.21		μs
t_{AS}	Setup Time, Address and R/W Valid to Enable Positive Transition	160		140		70		ns
t_{DDR}	Data Delay Time		320		220		180	ns
t_H	Data Hold Time	10		10		10		ns
t_{AH}	Address Hold Time	10		10		10		ns
t_{Er}, t_{Ef}	Rise and Fall Time for Enable Input		25		25		25	ns

Write

Symbol	Characteristic	S6850		S68A50		S68B50		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYCE}	Enable Cycle Time	1.0		0.666		0.50		μs
PW_{EH}	Enable Pulse Width, High	0.45		0.28		0.22	25	μs
PW_{EL}	Enable Pulse Width, Low	0.43		0.28		0.21		μs
t_{AS}	Setup Time, Address and R/W Valid to Enable Positive Transition	160		140		70		ns
t_{DSW}	Data Setup Time	195		80		60		ns
t_H	Data Hold Time	10		10		10		ns
t_{AH}	Address Hold Time	10		10		10		ns
t_{Er}, t_{Ef}	Rise and Fall Time for Enable Input		25		25		25	ns

Figure 1. Clock Pulse Width, Low State

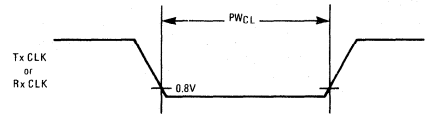


Figure 2. Clock Pulse Width, High State

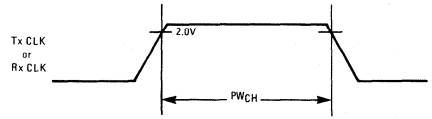


Figure 3. Transmit Data Output Delay

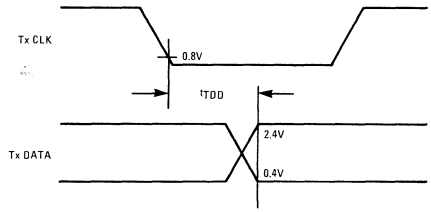


Figure 4. Receive Data Setup Time (÷1 Mode)

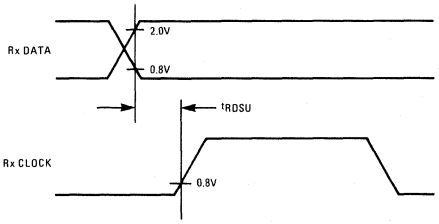


Figure 5. Receive Data Hold Time (÷1 Mode)

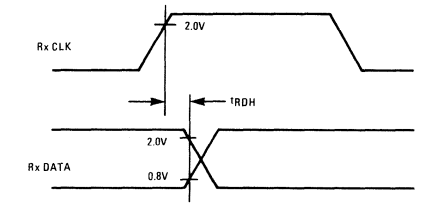


Figure 6. Request-to Send Delay and Interrupt-Request Release Times

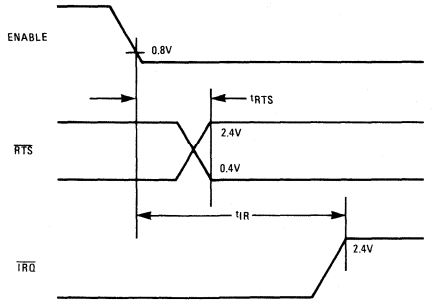


Figure 7. Bus Read Timing Characteristics (Read Information from ACIA)

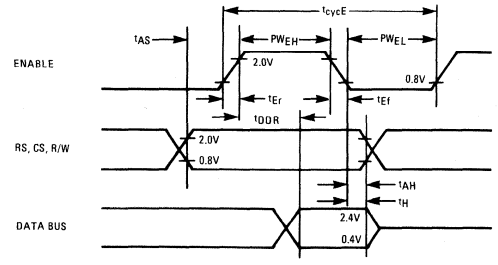
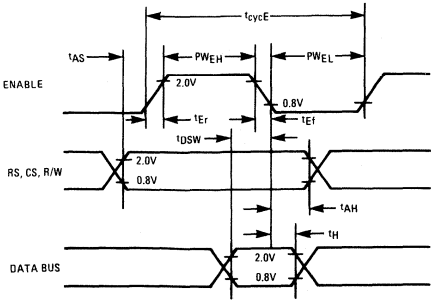
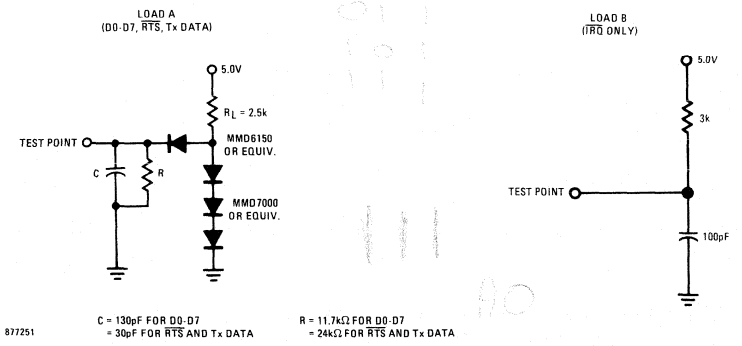


Figure 8. Bus Write Timing Characteristics (Write Information into ACIA)



Bus Timing Test Loads

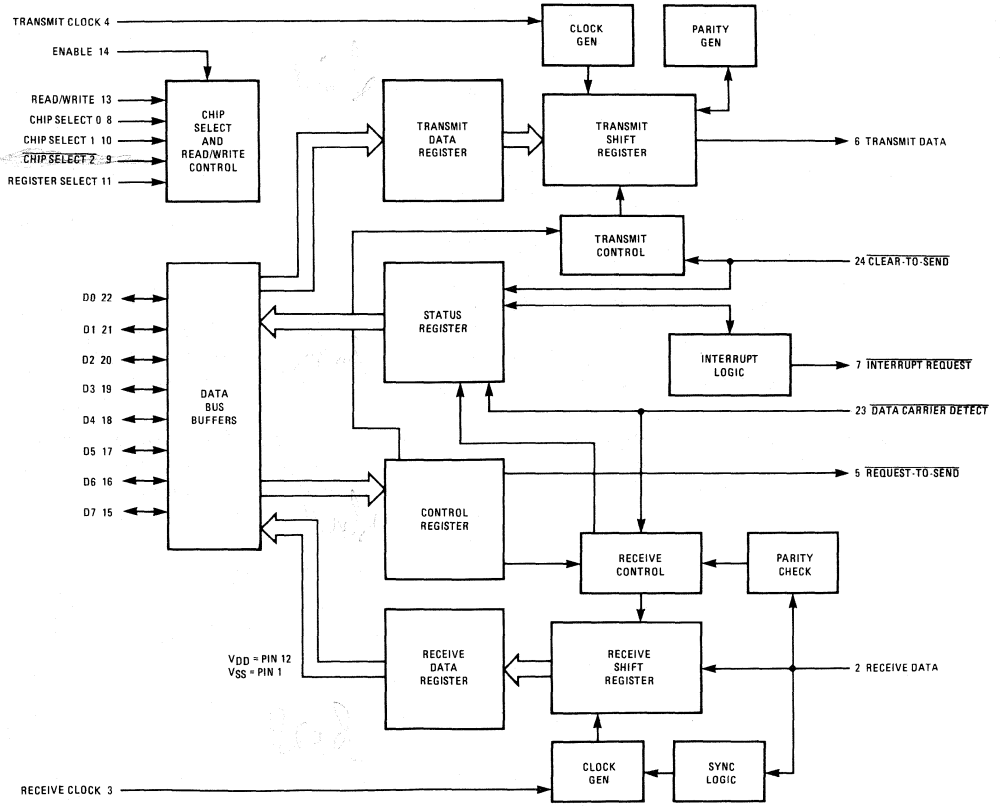


877251

C = 130pF FOR D0-D7
= 30pF FOR RTS AND Tx DATA

R = 11.7kΩ FOR D0-D7
= 24kΩ FOR RTS AND Tx DATA

Expanded Block Diagram



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MPU/ACIA Interface

Pin	Label	Function
(22)	D0	**ACIA Bidirectional Data Lines** — The bidirectional data lines (D0-D7) allow for data transfer between the ACIA and the MPU. The data bus output drivers are three-state devices that remain in the high impedance (off) state except when the MPU performs an ACIA read operation. The Read/Write line is in the read (high) state when the ACIA is selected for a read operation.
(21)	D1	
(20)	D2	
(19)	D3	
(18)	D4	
(17)	D5	
(16)	D6	
(15)	D7	
(14)	E	**ACIA Enable Signal** — The Enable signal (E) is a high impedance TTL compatible input that enables the bus input/output data buffers and clocks data to and from the ACIA. This signal will normally be a derivative of the S6800 $\phi 2$ clock.
(13)	R/W	**Read/Write Control Signal** — The Read/Write line is a high impedance input that is TTL compatible and is used to control the direction of data flow through the ACIA's input/output data bus interface. When Read/Write is high (MPU Read cycle), the ACIA output driver is turned on and a selected register is read. When it is low, the ACIA output driver is turned off and the MPU writes into a selected register. Thus, the Read/Write signal is used to select the Read Only or Write Only registers within the ACIA.
(8)	CS0	**Chip Select Signals** — These three high impedance TTL compatible input lines are used to address an ACIA. A particular ACIA is selected when CS0 and CS1 are high and $\overline{CS2}$ is low. Transfers of data to and from ACIA are then performed under the control of Enable, Read/Write and Register Select.
(10)	CS1	
(9)	$\overline{CS2}$	
(11)	RS	**Register Select Signal** — The Register Select line is a high impedance input that is TTL compatible and is used to select the Transmit/Receive Data or Control/Status registers in the ACIA. The Read/Write signal line is used in conjunction with Register Select to select the Read Only or Write Only register in each register pair.
(7)	$\overline{IRQ}$	**Interrupt Request Signal** — Interrupt request is a TTL compatible, open drain active low output that is used to interrupt the MPU. The Interrupt Request remains low as long as the cause of the interrupt is present and the appropriate interrupt enable within the ACIA is set.

ACIA/Modem or Peripheral Interface

Pin	Label	Function
(4)	CTX	**Transmit Clock** — The Transmit Clock is a high impedance TTL compatible input used for the clocking of transmitted data. The transmitter initiates data on the negative transition of the clock. Clock frequency of 1, 16, or 64 times the data rate may be selected.
(3)	CRX	**Receive Clock** — The Receive Clock is a high impedance TTL compatible input used for synchronization of received data. (In the ÷1 mode, the clock and data must be synchronized externally.) The receiver strobes the data on the positive transition of the clock. Clock frequency of 1, 16, or 64 times the data rate may be selected.
(2)	RXD	**Received Data** — The Received Data line is a high impedance TTL compatible input through which data is received in a serial NRZ (Non Return to Zero) format. Synchronization with a clock for detection of data is accomplished internally when clock rates of 16 or 64 times the bit rate are used. Data rates are in the range of 0 to 500 Kbps when external synchronization is utilized.
(6)	TXD	**Transmit Data** — The Transmit Data output line transfers serial NRZ data to a modem or other peripheral device. Data rates are in the range of 0 to 500 Kbps when external synchronization is utilized.
(24)	$\overline{CTS}$	**Clear-to-Send** — This high impedance TTL compatible input provides automatic control of the transmitting end of a communications link via the modem's "clear-to-send" active low output by inhibiting the Transmitter Data Register Empty status bit (TDRE).
(5)	$\overline{RTS}$	**Request-to-Send** — The Request-to-Send output enables the MPU to control a peripheral or modem via the data bus. The active state is low. The Request-to-Send output is controlled by the contents of the ACIA control register.
(23)	$\overline{DCD}$	**Data Carrier Detected** — This high impedance TTL compatible input provides automatic control of the receiving end of a communications link by means of the modem "Data-Carrier-Detect" or "Received-Line-Signal Detect" output. The $\overline{DCD}$ input inhibits and initializes the receiver section of the ACIA when high. A low to high transition of the Data Carrier Detect initiates an interrupt to the MPU to indicate the occurrence of a loss of carrier when the Receiver Interrupt Enable (RIE) is set.
(12)	V_{CC}	+5volts ±5%
(1)	GND	Ground

AMERICAN MICROSYSTEMS, INC.

S6852/S68A52/S68B52

SYNCHRONOUS SERIAL DATA ADAPTER (SSDA)

Features

- ☐ Programmable Interrupts from Transmitter, Receiver, and Error Detection Logic
- ☐ Character Synchronization on One or Two Sync Codes
- ☐ External Synchronization Available for Parallel-Serial Operation
- ☐ Programmable Sync Code Register
- ☐ Up to 600kbps Transmission
- ☐ Peripheral/Modem Control Functions
- ☐ Three Bytes of FIFO Buffering on Both Transmit and Receive
- ☐ Seven, Eight, or Nine Bit Transmission
- ☐ Optional Even and Odd Parity
- ☐ Parity, Overrun, and Underflow Status
- ☐ **Clock Rates:**
  1.0MHz
  1.5MHz
  2.0MHz

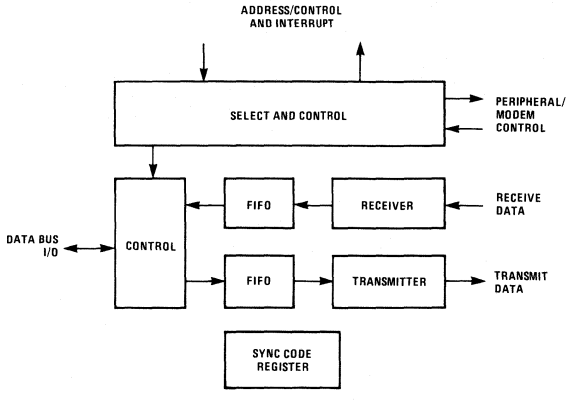
General Description

The S6852 Synchronous Serial Data Adapter provides a bi-directional serial interface for synchronous data information interchange. It contains interface logic for simultaneously transmitting and receiving standard synchronous communications characters in bus organized systems such as the S6800 Microprocessor systems.

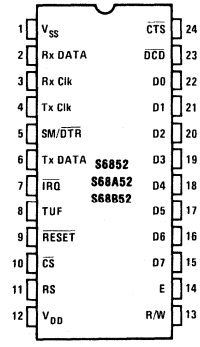
The bus interface of the S6852 includes select, enable, read/write, interrupt, and bus interface logic to allow data transfer over an 8-bit bi-directional data bus. The parallel data of the bus system is serially transmitted and received by the synchronous data interface with synchronization, fill character insertion/deletion, and error checking. The functional configuration of the SSDA is programmed via the data bus during system initialization. Programmable control registers provide control for variable word lengths, transmit control, receive control, synchronization control, and interrupt control. Status, timing and control lines provide peripheral or modem control.

Typical applications include floppy disk controllers, cassette or cartridge tape controllers, data communications terminals, and numerical control systems.

Block Diagram



Pin Configuration



Absolute Maximum Ratings:

Supply Voltage	−0.3 to +7.0
Input Voltage	−0.3 to +7.0V
Operating Temperature Range	0° to +70°C
Storage Temperature Range	−55° to +150°C
Thermal Resistance	+70°C/W

Note:
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Electrical Characteristics (V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = 0°C to 70°C unless otherwise noted.)

Symbol	Characteristic		Min.	Typ.	Max.	Unit
V_{IH}	Input High Voltage		V_{SS}+2.0			Vdc
V_{IL}	Input Low Voltage				V_{SS}+0.8	Vdc
I_{IN}	Input Leakage Current (V_{IN}=0 to 5.25Vdc)	TxClk, Rx Clk, Rx Data, Enable $\overline{Reset}$, RS, R/$\overline{W}$, $\overline{CS}$, $\overline{DCD}$, $\overline{CTS}$		1.0	2.5	μAdc
I_{TSI}	Three State (Off State) Input Current (V_{IN}=0.4 to 2.4Vdc, V_{CC}=5.25Vdc)	D0-D7		2.0	10	μAdc
V_{OH}	Output High Voltage I_{LOAD}=−205μAdc, Enable Pulse Width < 25μs I_{LOAD}=−100μAdc, Enable Pulse Width < 25μs	D0-D7 Tx Data, $\overline{DTR}$, TUF	 V_{SS}+2.4 V_{SS}+2.4			Vdc Vdc Vdc
V_{OL}	Output Low Voltage I_{LOAD}=1.6mAdc, Enable Pulse Width < 25μs				V_{SS}+0.4	Vdc
I_{LOH}	Output Leakage Current (Off State) V_{OH}=2.4Vdc	$\overline{IRQ}$		1.0	10	μAdc
P_D	Power Dissipation			300	525	mW
C_{IN}	Input Capacitance (V_{IN}=0, T_A=25°C, f=1.0MHz)	D0-D7 All Other Inputs			 12.5 7.5	pF
C_{OUT}	Output Capacitance (V_{IN}=0, T_A=25°C, f=1.0MHz)	Tx Data, SM/$\overline{DTR}$, TUF $\overline{IRQ}$			10 5.0	pF

Electrical Characteristics (V_{CC} = 5.0V ± 5%, T_A = T_L to T_H unless otherwise noted.)

		S6852		S68A52		S68B52		
Symbol	Characteristic	Min.	Max.	Min.	Max.	Min.	Max.	Unit
PW_{CL}	Minimum Clock Pulse Width, Low (Figure 1)	700		400		280		ns
PW_{CH}	Minimum Clock Pulse Width, High (Figure 2)	700		400		280		ns
f_C	Clock Frequency		600		1000		1500	kHz
t_{RDSU}	Receive Data Setup Time (Figure 3, 7)	350		200		160		ns
t_{RDH}	Receive Data Hold Time (Figure 3)	350		200		160		ns
t_{SM}	Sync Match Delay Time (Figure 3)		1.0		0.666		0.500	μs
t_{TDD}	Clock-to-Data Delay for Transmitter (Figure 4)		1.0		0.666		0.500	μs

*10μs or 10% of the pulse width, whichever is smaller.

Figure 1. Clock Pulse Width, Low-State

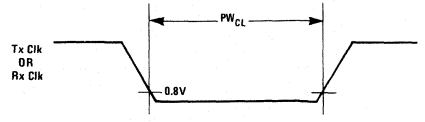
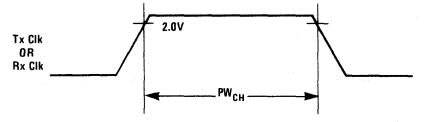


Figure 2. Clock Pulse Width, High-State



Electrical Characteristics-Continued (V_{CC} = 5.0V ± 5%, $T_A = T_L$ to T_H unless otherwise noted.)

Symbol	Characteristic	S6852 Min.	S6852 Max.	S68A52 Min.	S68A52 Max.	S68B52 Min.	S68B52 Max.	Unit
t_{TUF}	Transmitter Underflow (Figure 4, 6)		1.0		0.666		0.500	μs
t_{DTR}	$\overline{DTR}$ Delay Time (Figure 5)		1.0		0.666		0.500	μs
t_{IR}	$\overline{Interrupt\ Request}$ Release Time (Figure 5)		1.2		0.800		0.600	μs
t_{Res}	$\overline{Reset}$ Minimum Pulse Width	1.0		0.666		0.500		μs
t_{CTS}	$\overline{CTS}$ Setup Time (Figure 6)	200		150		120		ns
t_{DCD}	$\overline{DCD}$ Setup Time (Figure 7)	500		350		250		ns
t_r, t_f	Input Rise and Fall Times (except Enable) (0.8V to 2.0V)		1.0		1.0		1.0	μs

Bus Timing Characteristics

Symbol	Characteristic	S6852 Min.	S6852 Max.	S68A52 Min.	S68A52 Max.	S68B52 Min.	S68B52 Max.	Unit
Read								
t_{CYCE}	Enable Cycle Time	1.0		0.666		0.5		μs
PW_{EH}	Enable Pulse Width, High	0.45	25	0.28	25	0.22	25	μs
PW_{EL}	Enable Pulse Width, Low	0.43		0.28		0.21		μs
t_{AS}	Setup Time, Address and R/W Valid to Enable Positive Transition	160		140		70		ns
t_{DDR}	Data Delay Time		320		220		180	ns
t_H	Data Hold Time	10		10		10		ns
t_{AH}	Address Hold Time	10		10		10		ns
t_{Er}, t_{Ef}	Rise and Fall Time for Enable Input		25		25		25	ns
Write								
t_{CYCE}	Enable Cycle Time	1.0		0.666		0.5		μs
PW_{EH}	Enable Pulse Width, High	0.45	25	0.28	25	0.22	25	μs
PW_{EL}	Enable Pulse Width, Low	0.43		0.28		0.21		μs
t_{AS}	Setup Time, Address and R/W Valid to Enable Positive Transition	160		140		70		ns
t_{DSW}	Setup Time	195		80		60		ns
t_H	Data Hold Time	10		10		10		ns
t_{AH}	Address Hold Time	10		10		10		ns
t_{Er}, t_{Ef}	Rise and Fall Time for Enable Input		25		25		25	ns

Figure 3. Receive Data Setup and Hold Times and Sync Delay Time

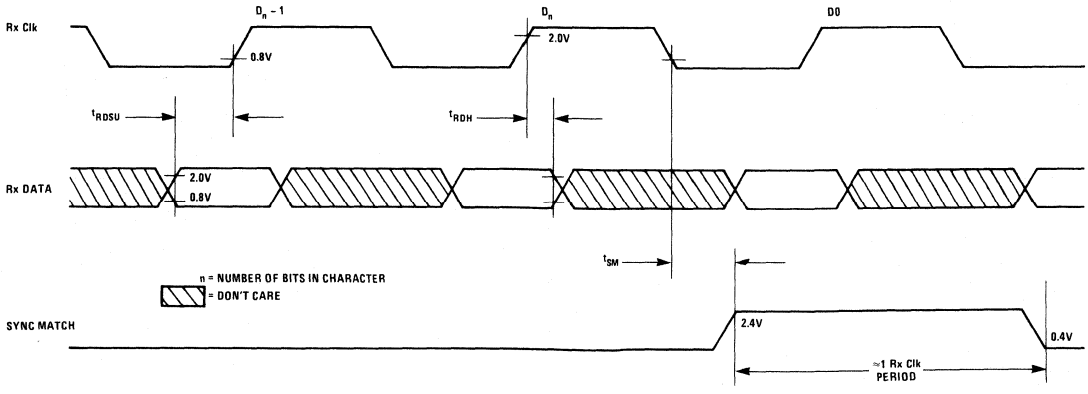


Figure 4. Transmit Data Output Delay and Transmitter Underflow Delay Time

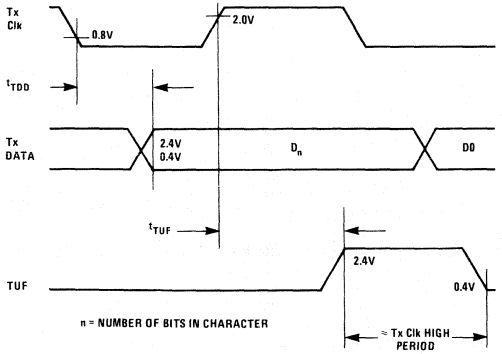


Figure 5. Data Terminal Ready and Interrupt Request Release Times

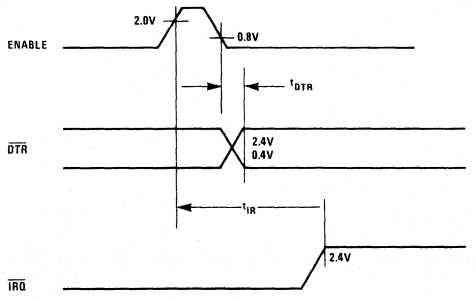


Figure 6. Clear-To-Send Setup Time

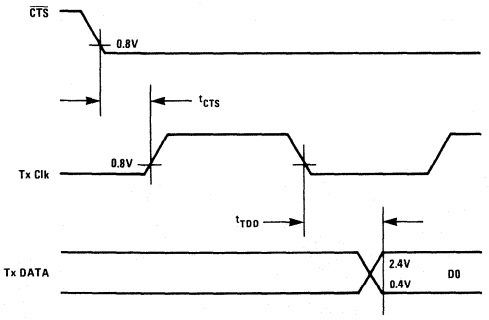


Figure 7. Data Carrier Detect Setup Time

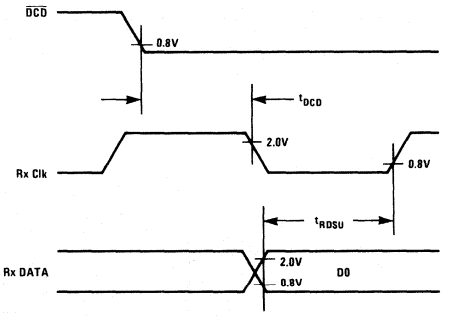


Figure 8. Bus Read Timing Characteristics (Read Information from SSDA)

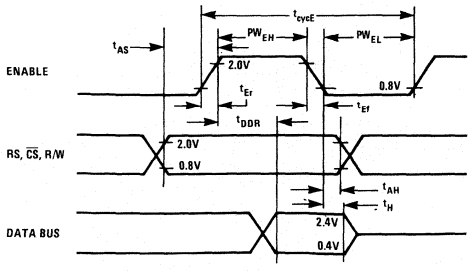


Figure 9. Bus Write Timing Characteristics (Write Information into SSDA)

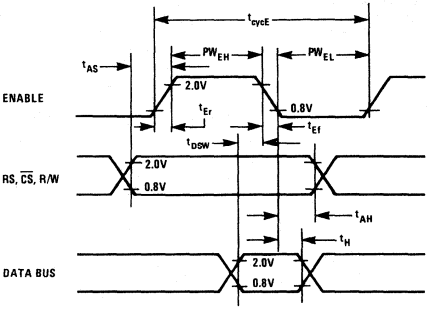
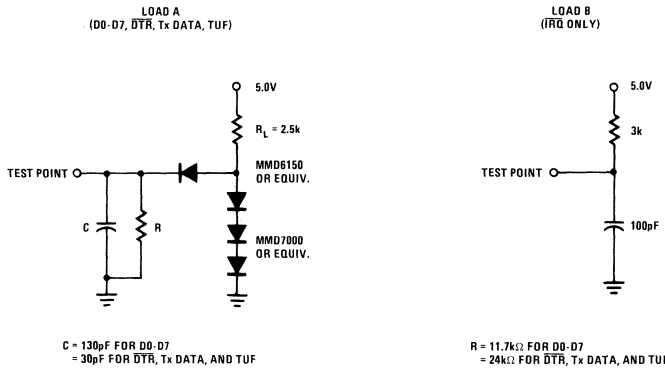
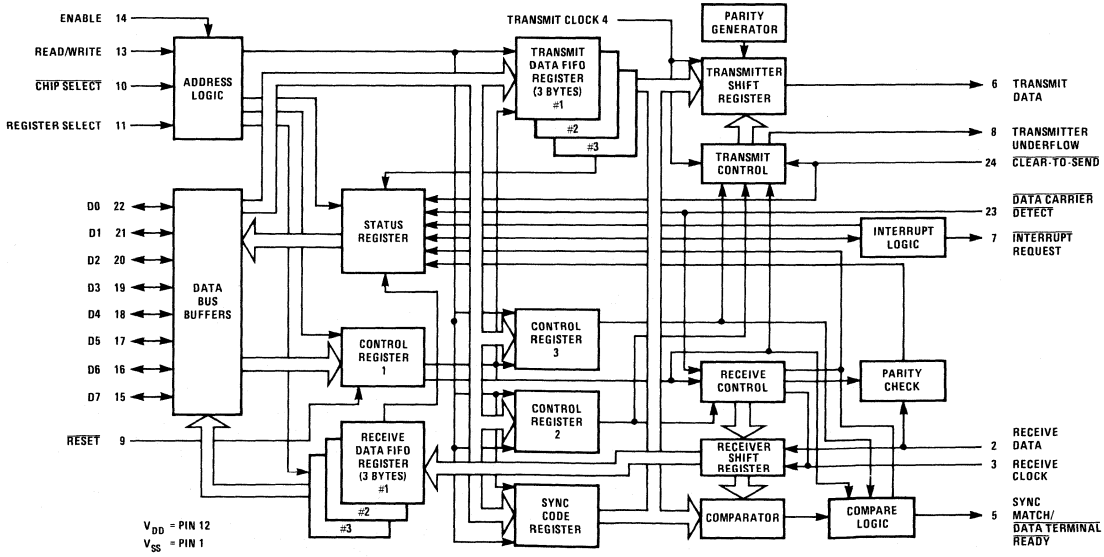


Figure 10. Bus Timing Test Loads



Expanded Block Diagram



Device Operation

At the bus interface, the SSDA appears as two addressable memory locations. Internally, there are seven registers: two read-only and five write-only registers. The read-only registers are Status and Receive Data; the write-only registers are Control 1, Control 2, Control 3, Sync Code and Transmit Data. The serial interface consists of serial input and output lines with independent clocks, and four peripheral/modem control lines.

Data to be transmitted is transferred directly into the 3-byte Transmit Data First-In First-Out (FIFO) Register from the data bus. Availability of the input to the FIFO is indicated by a bit in the Status Register; once data is entered, it moves through the FIFO to the last empty location. Data at the output of the FIFO is automatically transferred from the FIFO to the Transmitter Shift Register as the shift register becomes available to transmit the next character. If data is not available from the FIFO (underflow condition), the Transmitter Shift Register is automatically loaded with either a sync code or an all "1"s character. The transmit section may be programmed to append loaded with either a sync code or an all "1"s character. The transmit section may be programmed to append even, odd, or no parity to the transmitted word. An external control line ($\overline{\text{Clear-to-Send}}$) is provided to inhibit the transmitter without clearing the FIFO.

Serial data is accumulated in the receiver based on the synchronization mode selected. In the external sync mode, used for parallel-serial operation, the receiver is synchronized by the $\overline{\text{DCD}}$ ($\overline{\text{Data Carrier Detect}}$) input and transfers successive bytes of data to the input of the Receiver FIFO. The single-sync-character mode requires that a match occur between the Sync Code Register and one incoming character before data transfer to the FIFO begins. The two-sync-character mode requires that two sync codes be received in sequence to establish synchronization. Subsequent to synchronization in any mode, data is accumulated in the shift register, and parity is optionally checked. An indication of parity error is carried through the Receiver FIFO with each character to the last empty location. Availability of a word at the FIFO output is indicated by a bit in the Status Register, as is a parity error.

The SSDA and its internal registers are selected by the address bus, Read/Write (R/W) and Enable control lines. To configure the SSDA, Control Registers are selected and the appropriate bits set. The Status Register is addressable for reading status.

Other I/O lines, in addition to $\overline{\text{Clear-to-Send}}$ ($\overline{\text{CTS}}$) and $\overline{\text{Data Carrier Detect}}$ ($\overline{\text{DCD}}$), include SM/$\overline{\text{DTR}}$ (Sync Match/$\overline{\text{Data Terminal Ready}}$) and Transmitter Underflow (TUF). The transmitter and receiver each have individual clock inputs allowing simultaneous operation under separate clock control. Signals to the microprocessor are the Data bus and $\overline{\text{Interrupt}}$ Request ($\overline{\text{IRQ}}$).

Initialization

During a power-on sequence, the SSDA is reset via the $\overline{\text{Reset}}$ input and internally latched in a reset condition to prevent erroneous output transitions. The Sync Code Register, Control Register 2, and Control Register 3 should be programmed prior to the programmed release of the Transmitter and/or Receiver Reset bits; these bits in Control Register 1 should be cleared after the Reset line has gone high.

Transmitter Operation

Data is transferred to the transmitter section in parallel form by means of the data bus and Transmit Data FIFO. The Transmit Data FIFO is a 3-byte register whose status is indicated by the Transmitter Data Register Available status bit (TDRA) and its associated interrupt enable bit. Data is transferred through the FIFO on Enable (E) pulses. Two data transfer modes are provided in the SSDA. The 1-byte transfer mode provides for writing data to the transmitter section (and reading from the receiver section) one byte at a time. The 2-byte transfer mode provides for writing two data characters in succession.

Data will automatically transfer from the last register location in the Transmit Data FIFO (when it contains data) to the Transmitter Shift Register during the last half of the last bit of the previous character. A character is transferred into the Shift Register by the Transmitter Clock. Data is transmitted *LSB first*, and odd or even parity can be optionally appended. The unused bit positions in short word length characters from the data bus are "don't cares." (Note: The data bus inputs may be reversed for applications requiring the MSB to be transferred first, e.g., IBM format for floppy disks; however, care must be taken to properly program the control registers — Table 1 will have its bit positions reversed.)

When the Shift Register becomes empty and data is *not* available for transfer from the Transmit Data FIFO, an "underflow" occurs, and a character is inserted into the transmitter data stream to maintain

character synchronization. The character transmitted on underflow will be either a "Mark" (all "1"s) or the contents of the Sync Code Register, depending upon the state of the Transmit Sync Code on Underflow control bit. The underflow condition is indicated by a pulse (≈1 Tx Clk high period) on the Underflow output (when in Tx Sync on underflow mode). The Underflow output occurs coincident with the transfer of the last half of the last bit preceding the underflow character. The Underflow status bit is set until cleared by means of the Clear Underflow control bit. This output may be used in floppy disk systems to synchronize write operations and for appending CRCC.

Transmission is initiated by clearing the Transmitter Reset bit in Control Register 1. When the Transmitter Reset bit is cleared, the first *full* positive half-cycle of the Transmit Clock will initiate the transmit cycle, with the transmission of data or underflow characters beginning on the negative edge of the Transmit Clock pulse which started the cycle. If the Transmit Data FIFO was not loaded, an underflow character will be transmitted (see Figure 4).

The Clear-to-Send ($\overline{CTS}$) input provides for automatic control of the transmitter by means of external system hardware; e.g., the modem $\overline{CTS}$ output provides the control in a data communications system. The $\overline{CTS}$ input resets and inhibits the transmitter section when high, but does not reset the Transmit Data FIFO. The TDRA status bit is inhibited by $\overline{CTS}$ being high in either the one-sync-character or two-sync-character mode of operation. In the external sync mode, TDRA is unaffected by $\overline{CTS}$ in order to provide Transmit Data FIFO status for preloading and operating the transmitter under the control of the $\overline{CTS}$ input. When the Transmitter Reset bit (Tx Rx) is set, the Transmit Data FIFO becomes available for new data with TDRA inhibited.

Receiver Operation

Data and a presynchronized clock are provided to the SSDA receiver section by means of the Receive Data (Rx Data) and Receive Clock (Rx Clk) inputs. The data is a continuous stream of binary data bits without means for identifying character boundaries within the stream. It is, therefore, necessary to achieve character synchronization for the data at the *beginning* of the data block. Once synchronization is achieved, it is assumed to be retained for all successive characters within the block.

Data communications systems utilize the detection of sync codes during the initial portion of the preamble to establish character synchronization. This requires the detection of a single code or two successive sync codes. Floppy disk and cartridge tape units require sixteen bits of defined preamble and cassettes require eight bits of preamble to establish the reference for the start of record. All three are functionally equivalent to the detection of sync codes. Systems which do not utilize code detection techniques require custom logic external to the SSDA for character synchronization and use of the parallel-to-serial (external sync) mode. (Note: The Receiver Shift Register is set to ones when reset.)

Synchronization

The SSDA provides three operating modes with respect to character synchronization: one-sync-character mode, two-sync-character mode, and external sync mode. The external sync mode requires synchronization and control of the receiving section through the Data Carrier Detect ($\overline{DCD}$) input (see Figure 7). This external synchronization could consist of direct line control from the transmitting end of the serial data link or from external logic designed to detect the start of the message block. The one-sync-character mode searches on a bit-by-bit basis until a match is achieved between the data in the Shift Register and the Sync Code Register. The match indicates character synchronization is complete and will be retained for the message block. In the two-sync-character mode, the receiver searches for the first sync code match on a bit-by-bit basis and then looks for a second *successive* sync code character prior to establishing character synchronization. If the second sync code character is not received, the bit-by-bit search for the first sync code is resumed.

Sync codes received prior to the completion of synchronization (one or two character) are not transferred to the Receive Data FIFO. Redundant sync codes during the preamble or sync codes which occur as "fill characters" can automatically be stripped from the data, when the Strip Sync control bit is set, to minimize system loading. The character synchronization will be retained until cleared by means of the Clear Sync bit, which also inhibits synchronization search when set.

Receiving Data

Once synchronization has been achieved, subsequent characters are automatically transferred into the Receive Data FIFO and clocked through the FIFO to the last empty location by E pulses (MPU System $\phi 2$).

The Receiver Data Available status bit (RDA) indicates when data is available to be read from the last FIFO location (#3) when in the 1-byte transfer mode. The 2-byte transfer mode causes the RDA status bit to indicate data is available when the last two FIFO register locations are full. Data being available in the Receive Data FIFO causes an interrupt request if the Receiver Interrupt Enable (RIE) bit is set. The MPU will then read the SSDA Status Register, which will indicate that data is available for the MPU read from the Receive Data FIFO register. The IRQ and RDA status bits are reset by a read from the FIFO. If more than one character has been received and is resident in the Receive Data FIFO, subsequent E clocks will cause the FIFO to update and the RDA and IRQ status bits will again be set. The read data operation for the 2-byte transfer mode requires an intervening E clock between reads to allow the FIFO data to shift. Optional parity is automatically checked as data is received, and the parity status condition is maintained with each character until the data is read from the Receive Data FIFO. Parity errors will cause an interrupt request if the Error Interrupt Enable (EIE) has been set. The parity bit is not transferred to the data bus but must be checked in the Status Register. NOTE: In the 2-byte transfer mode, parity should be checked prior to reading the second byte, since a FIFO read clears the error bit.

Other status bits which pertain to the receiver section are Receiver Overrun and Data Carrier Detect ($\overline{DCD}$). The Overrun status bit is automatically set when a transfer of a character to the Receive Data FIFO occurs and the first register of the Receive Data FIFO is full. Overrun causes an interrupt if Error Interrupt Enable (EIE) has been set. The transfer of the overrunning character into the FIFO causes the previous character in the FIFO input register location to be lost The Overrun status bit is cleared by reading the Status Register (when the overrun condition is present), followed by a Receive Data FIFO Register read. Overrun cannot occur and be cleared without providing an opportunity to detect its occurrence via the Status Register.

A positive transition on the $\overline{DCD}$ input causes an interrupt if the EIE control bit has been set. The interrupt caused by $\overline{DCD}$ is cleared by reading the Status Register when the $\overline{DCD}$ status bit is high, followed by a Receive Data FIFO read. The $\overline{DCD}$ status bit will subsequently follow the state of the $\overline{DCD}$ input when it goes low.

Input/Output Functions

SSDA Interface Signals for MPU

The SSDA interfaces to the S6800 MPU with an 8-bit bi-directional data bus, a chip select line, a register select line, an interrupt request line, read/write line, an enable line, and a reset line. These signals, in conjunction with the S6800 VMA output, permit the MPU to have complete control over the SSDA.

SSDA Bi-Directional Data (D0-D7)—The bi-directional data lines (D0-D7) allow for data transfer between the SSDA and the MPU. The data bus output drivers are three-state devices that remain in the high-impedance (off) state except when the MPU performs an SSDA read operation.

SSDA Enable (E) — The Enable signal, E, is a high impedance TTL compatible input that enables the bus input/output data buffers, clocks data to and from the SSDA, and moves data through the FIFO Registers. This signal is normally the continuous S6800 System $\phi 2$ clock, so that incoming data characters are shifted through the FIFO.

Read/Write (R/W) — The Read/Write line is a high impedance input that is TTL compatible and is used to control the direction of data flow through the SSDA's input/output data bus interface. When Read/Write is high (MPU read cycle), SSDA output drivers are turned on if the chip is selected and a selected register is read. When it is low, the SSDA output drivers are turned off and the MPU writes into a selected register. The Read/Write signal is also used to select read-only or write-only registers within the SSDA.

Chip Select ($\overline{CS}$) — This high impedance TTL compatible input line is used to address the SSDA. The SSDA is selected when $\overline{CS}$ is low. VMA should be used in generating the $\overline{CS}$ input to insure that false selects will not occur. Transfers of data to and from the SSDA are then performed under the control of the Enable signal, Read/Write, and Register Select.

Register Select (RS) — The Register Select line is a high impedance input that is TTL compatible. A high level is used to select Control Registers C2 and C3, the Sync Code Register, and the Transmit/Receive Data Registers. A low level selects the Control 1 and Status Registers (see Table 1).

Table 1. SSDA Programming Model

REGISTER	CONTROL INPUTS		ADDRESS CONTROL		REGISTER CONTENT							
	RS	R/W	AC2	AC1	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
STATUS (S)	0	1	X	X	INTERRUPT REQUEST (IRQ)	RECEIVER PARITY ERROR (PE)	RECEIVER OVERRUN (Rx Ovrn)	TRANS-MITTER UNDERFLOW (TUF)	CLEAR-TO-SEND (CTS)	DATA CARRIER DETECT (DCD)	TRANS-MITTER DATA REGISTER AVAILABLE (TDRA)	RECEIVER DATA AVAILABLE (RDA)
CONTROL 1 (C1)	0	0	X	X	ADDRESS CONTROL 2 (AC2)	ADDRESS CONTROL 1 (AC1)	RECEIVER INTERRUPT ENABLE (RIE)	TRANS-MITTER INTERRUPT ENABLE (TIE)	CLEAR SYNC	STRIP SYNC CHARACTERS (STRIP SYNC)	TRANS-MITTER RESET (Tx Rs)	RECEIVER RESET (Rx Rs)
RECEIVE DATA FIFO	1	1	X	X	D7	D6	D5	D4	D3	D2	D1	D0
CONTROL 2 (C2)	1	0	0	0	ERROR INTERRUPT ENABLE (EIE)	TRANSMIT SYNC CODE ON UNDERFLOW (Tx Sync)	WORD LENGTH SELECT 3 (WS3)	WORD LENGTH SELECT 2 (WS2)	WORD LENGTH SELECT 1 (WS1)	1-BYTE/ 2-BYTE TRANSFER (1-BYTE/ 2-BYTE)	PERIPHERAL CONTROL 2 (PC2)	PERIPHERAL CONTROL 1 (PC1)
CONTROL 3 (C3)	1	0	0	1	NOT USED	NOT USED	NOT USED	NOT USED	CLEAR TRANS-MITTER UNDERFLOW STATUS (CTUF)	CLEAR CTS STATUS (CLEAR CTS)	ONE-SYNC-CHARACTER/ TWO-SYNC-CHARACTER MODE CONTROL (1 Sync/ 2 Sync)	EXTERNAL/ INTERNAL SYNC MODE CONTROL (E/I Sync)
SYNC CODE	1	0	1	0	D7	D6	D5	D4	D3	D2	D1	D0
TRANSMIT DATA FIFO	1	0	1	1	D7	D6	D5	D4	D3	D2	D1	D0

X = DON'T CARE

Status Register

IRQ Bit 7 — The IRQ flag is cleared when the source of the IRQ is cleared. The source is determined by the enables in the Control Registers: TIE, RIE, EIE.

Bits 6-0 indicate the SSDA status at a point in time, and can be *reset* as follows:

PE — Bit 6 — Read Rx Data FIFO, or a "1" into Rx Rs (C1 Bit 0).

Rx Ovrn — Bit 5 — Read Status and then Rx Data FIFO, or a "1" into Rx Rs (C1 Bit 0).

TUF — Bit 4 — A "1" into CTUF (C3 Bit 3) or into Tx Rs (C1 Bit 1).

$\overline{CTS}$ — Bit 3 — A "1" into Clear $\overline{CTS}$ (C3 Bit 2) or a "1" into Tx Rs (C1 Bit 1)

$\overline{DCD}$ — Bit 2 — Read Status and then Rx Data FIFO or a "1" into Rx Rs (C1 Bit 0)

TDRA — Bit 1 — Write into Tx Data FIFO.

RDA — Bit 0 — Read Rx Data FIFO.

Control Register 1

AC2, AC1 — Bits 7, 6 — Used to access other registers, as shown above.

RIE — Bit 5 — When "1", enables interrupt on RDA (S Bit 0).

TIE — Bit 4 — When "1", enables interrupt on TDRA (S Bit 1).

Clear Sync — Bit 3 — When "1", clears receiver character synchronization.

Strip Sync — Bit 2 — When "1", strips all sync codes from the received data stream.

Tx Rs — Bit 1 — When "1", resets and inhibits the transmitter section.

Rx Rs — Bit 0 — When "1", resets and inhibits the receiver section.

Control Register 3

CTUF — Bit 3 — When "1", clears TUF (S Bit 4), and IRQ if enabled.

Clear $\overline{CTS}$ — Bit 2 — When "1", clears $\overline{CTS}$ (S Bit 3), and IRQ if enabled.

1 Sync/2 Sync — Bit 1 — When "1", selects the one-sync-character mode; when "0", selects the two-sync-character mode.

E/I Sync — Bit 0 — When "1", selects the external sync mode; when "0", selects the internal sync mode.

Control Register 2

EIE — Bit 7 — When "1", enables the PE, Rx Ovrn, TUF, $\overline{CTS}$, and $\overline{DCD}$ interrupt flags (S Bits 6 through 2).

Tx Sync — Bit 6 — When "1", allows sync code contents to be transferred on underflow, and enables the TUF Status bit and output. When "0", an all mark character is transmitted on underflow.

WS3, 2, 1 — Bits 5-3 Word Length Select

BIT 5 WS3	BIT 4 WS2	BIT 3 WS1	WORD LENGTH
0	0	0	6 BITS + EVEN PARITY
0	0	1	6 BITS + ODD PARITY
0	1	0	7 BITS
0	1	1	8 BITS
1	0	0	7 BITS + EVEN PARITY
1	0	1	7 BITS + ODD PARITY
1	1	0	8 BITS + EVEN PARITY
1	1	1	8 BITS + ODD PARITY

1-Byte/2-Byte — Bit 2 — When "1", enables the TDRA and RDA bits to indicate when a 1-byte transfer can occur; when "0", the TDRA and RDA bits indicate when a 2-byte transfer can occur.

PC2, PC1 — Bits 1-0 — SM/$\overline{DTR}$ Output Control

BIT 1 PC2	BIT 0 PC1	SM/$\overline{DTR}$ OUTPUT AT PIN 5
0	0	1
0	1	PULSE ⎍ 1-BIT WIDE ON SM
1	0	0
1	1	SM INHIBITED, 0

Note: When the SSDA is used in applications requiring the MSB of data to be received and transmitted first, the data bus inputs to the SSDA may be reversed (D0 to D7, etc.) Caution must be used when this is done since the bit positions in this table will be reversed, and the parity should not be selected.

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Interrupt Request ($\overline{IRQ}$) — $\overline{Interrupt\ Request}$ is a TTL compatible, open-drain (no internal pullup), active low output that is used to interrupt the MPU. The $\overline{Interrupt\ Request}$ remains low until cleared by the MPU.

$\overline{Reset}$ Input — The $\overline{Reset}$ input provides a means of resetting the SSDA from an external source. In the low state, the $\overline{Reset}$ input causes the following:

1. Receiver Reset (Rx Rs) and Transmitter Reset (Tx Rs) bits are set causing both the receiver and transmitter sections to be held in a reset condition.
2. Peripheral Control bits PC1 and PC2 are reset to zero, causing the SM/$\overline{DTR}$ output to be high.
3. The Error Interrupt Enable (EIE) bit is reset.
4. An internal synchronization mode is selected.
5. The Transmitter Data Register Available (TDRA) status bit is cleared and inhibited.

When $\overline{Reset}$ returns high (the inactive state), the transmitter and receiver sections will remain in the reset state until the Receiver Reset and Transmitter Reset bits are cleared via the bus under software control. The control Register bits affected by $\overline{Reset}$ (Rx Rs, Tx Rs, PC1, PC2, EIE, and E/I Sync) cannot be changed when $\overline{Reset}$ is low.

Clock Inputs

Separate high impedance TTL compatible inputs are provided for clocking of transmitted and received data.

Transmit Clock (Tx Clk) — The Transmit Clock input is used for the clocking of transmitted data. The transmitter shifts data on the negative transition of the clock.

Receive Clock (Rx Clk) — The Receive Clock input is used for clocking in received data. The clock and data must be synchronized externally. The receiver samples the data on the positive transition of the clock.

Serial Input/Output Lines

Receive Data (Rx Data) — The Receive Data line is a high impedance TTL compatible input through which data is received in a serial format. Data rates are from 0 to 600 kbps.

Transmit Data (Tx Data) — The Transmit Data output line transfers serial data to a modem or other peripheral. Data rates are from 0 to 600 kbps.

Peripheral/Modem Control

The SSDA includes several functions that permit limited control of a peripheral or modem. The functions included are $\overline{Clear\text{-}to\text{-}Send}$, Sync Match/$\overline{Data}$

Terminal Ready, Data Carrier Detect, and Transmitter Underflow.

Clear-to-Send ($\overline{CTS}$) — The $\overline{CTS}$ input provides a real-time inhibit to the transmitter section (the Tx Data FIFO is not disturbed). A positive $\overline{CTS}$ transition resets the Tx Shift Register and inhibits the TDRA status bit and its associated interrupt in both the one-sync-character and two-sync-character modes of operation. TDRA is not affected by the $\overline{CTS}$ input in the external sync mode.

The positive transition of $\overline{CTS}$ is stored within the SSDA to insure that its occurrence will be acknowledged by the system. The stored $\overline{CTS}$ information and its associated $\overline{IRQ}$ (if enabled) are cleared by writing a "1" in the Clear $\overline{CTS}$ bit in Control Register 3 or in the Transmitter Reset bit. The $\overline{CTS}$ status bit subsequently follows the $\overline{CTS}$ input when it goes low.

The $\overline{CTS}$ input provides character timing for transmitter data when in the external sync mode. Transmission is initiated on the negative transition of the first *full* positive clock pulse of the transmitter clock (Tx Clk) after the release of $\overline{CTS}$ (see Figure 6).

Data Carrier Detect ($\overline{DCD}$) — The $\overline{DCD}$ input provides a real-time inhibit to the receiver section (the Rx FIFO is not disturbed). A positive $\overline{DCD}$ transition resets and inhibits the receiver section except for the Receive FIFO and the RDRA status bit and its associated $\overline{IRQ}$.

The positive transition of $\overline{DCD}$ is stored within the SSDA to insure that its occurrence will be acknowledged by the system. The stored $\overline{DCD}$ information and its associated $\overline{IRQ}$ (if enabled) are cleared by reading the Status Register and then the Receiver FIFO, or by writing a "1" into the Receiver Reset bit. The $\overline{DCD}$ status bit subsequently follows the $\overline{DCD}$ input when it goes low. The $\overline{DCD}$ input provides character synchronization timing for the receiver during the external sync mode of operation. The receiver will be initialized and data will be sampled on the positive transition of the first *full* Receive Clock cycle after release of $\overline{DCD}$ (see Figure 7).

Sync Match/Data Terminal Ready (SM/$\overline{DTR}$) — The SM/DTR output provides four functions (see Table 1) depending on the state of the PC1 and PC2 control bits. When the Sync Match mode is selected (PC1 = "1", PC2 = "0"), the output provides a one-bit-wide pulse when a sync code is detected. The SM output is inhibited when PC2 = "1". The $\overline{DTR}$ mode (PC1 = "0") provides an output level corresponding to the complement of PC2 ($\overline{DTR}$ = "0" when PC2 = "1"). (See Table 1.)

Transmitter Underflow (TUF) — The Underflow output indicates the occurrence of a transfer of a "fill character" to the Transmitter Shift Register when the last location (#3) in the Transmit Data FIFO is empty. The Underflow output pulse is approximately a Tx Clk high period wide and occurs during the last half of the last bit of the character preceding the "Underflow" (see Figure 4). The Underflow output does not respond to underflow conditions when the Tx Sync bit is in the reset state.

ADVANCED DATA LINK CONTROLLER

Features

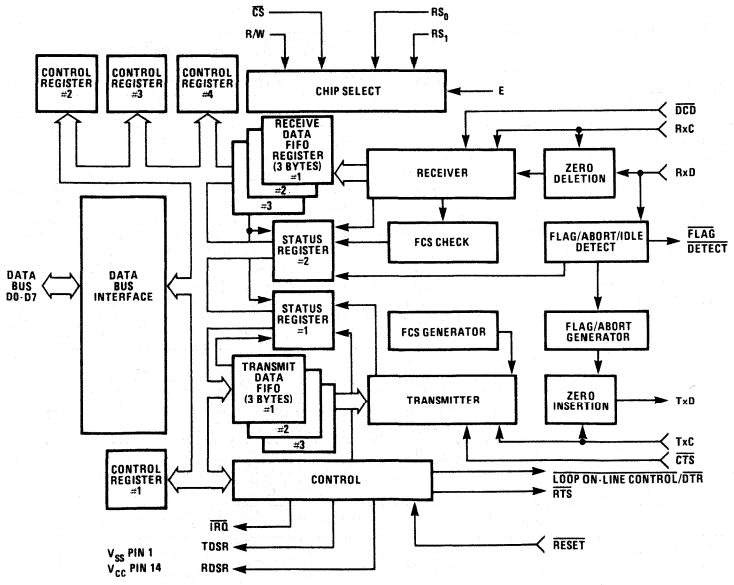
- ☐ S6800 Compatible
- ☐ Protocol Features
  - ☐ Automatic Flag Detection and Synchronization
  - ☐ Zero Insertion and Deletion
  - ☐ Extendable Address, Control and Logical Control Fields (Optional)
  - ☐ Variable Word Length Info Field — 5, 6, 7, or 8-bits
  - ☐ Automatic Frame Check Sequence Generation and Check
  - ☐ Abort Detection and Transmission
  - ☐ Idle Detection and Transmission
- ☐ Loop Mode Operation
- ☐ Loop Back Self-Test Mode
- ☐ NRZ/NRZI Modes
- ☐ Quad Data Buffers for Each Rx and Tx
- ☐ Prioritized Status Register (Optional)
- ☐ MODEM/DMA/Loop Interface

General Description

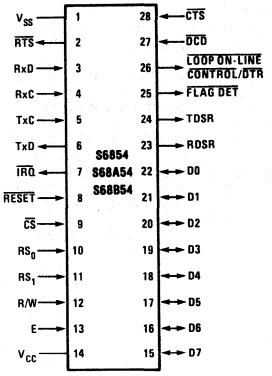
The S6854 ADLC performs the complex MPU/data communication link function for the "Advanced Data Communication Control Procedure" (ADCCP). High Level Data Link Control (HDLC) and Synchronous Data Link Control (SDLC) standards. The ADLC provides key interface requirements with improved software efficiency. The ADLC is designed to provide the data communications interface for both primary and secondary stations in stand-alone, polling, and loop configurations.

S6800

Block Diagram



Pin Configuration



Absolute Maximum Ratings*

Supply Voltage	−0.3 to +7.0V
Input Voltage	−0.3 to +7.0V
Operating Temperature Range	0° to +70°C
Storage Temperature Range	−55° to +150°C
Thermal Resistance	70°C/W

*This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Electrical Characteristics (V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = 0°C to +70°C unless otherwise noted.)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{IH}	Input High Voltage	V_{SS}+2.0		Vdc		
V_{IL}	Input Low Voltage			V_{SS}+0.8	Vdc	
I_{IN}	Input Leakage Current All Inputs Except D0—D7		1.0	2.5	μAdc	V_{IN}=0 to 5.25 Vdc
I_{TSI}	Three State (Off State) Input Current D0—D7		2.0	10	μAdc	V_{IN}=0.4 to 2.4Vdc V_{CC}=5.25Vdc
V_{OH}	Output High Voltage D0-D7 All Others	 V_{SS}+2.4 V_{SS}+2.4			 Vdc Vdc	 I_{LOAD}=−205μAdc I_{LOAD}=−100μAdc
V_{OL}	Output Low Voltage			V_{SS}+0.4	Vdc	I_{LOAD}=1.6mAdc
I_{LOH}	Output Leakage Current (Off State) $\overline{IRQ}$		1.0	10	μAdc	V_{OH}=2.4Vdc
P_D	Power Dissipation			850	mW	
C_{IN}	Capacitance D0-D7 All Other Inputs			12.5 7.5	pF pF	V_{IN}=0, T_A=+25°C, f=1.0MHz
C_{OUT}	$\overline{IRQ}$ All Others			5.0 10	pF pF	

Symbol	Characteristic	S6854 Min.	S6854 Max.	S68A54 Min.	S68A54 Max.	S68B54 Min.	S68B54 Max.	Unit
PW_{CL}	Minimum Clock Pulse Width, Low	700		450		280		ns
PW_{CH}	Minimum Clock Pulse Width, High	700		450		280		ns
f_C	Clock Frequency		0.66		1.0		1.5	MHz
t_{RDSU}	Receive Data Setup Time	250		200		120		ns
t_{RDH}	Receive Data Hold Time	120		100		60		ns
t_{RTS}	Request-to-Send Delay Time		680		460		340	ns
t_{TDD}	Clock-to-Data Delay for Transmitter		460		320		250	ns
t_{FD}	Flag Detect Delay Time		680		460		340	ns
t_{DTR}	DTR Delay Time		680		460		340	ns
t_{LOC}	Loop On-Line Control Delay Time		680		460		340	ns
t_{RDSR}	RDSR Delay Time		540		400		340	ns
t_{TDSR}	TDSR Delay Time		540		400		340	ns
t_{IR}	Interrupt Request Release Time		1.2		0.9		0.7	μs
t_{RES}	Reset Minimum Pulse Width	1.0		0.65		0.40		μs
t_r, t_f	Input Rise and Fall Times except Enable (0.8V to 2.0V)		1.0*		1.0*		1.0*	μs

*1.0μs or 10% of the pulse width, whichever is smaller.

Bus Timing Characteristics (V_{CC} = +5.0V ±5%, V_{SS} = 0, T_A = 0°C to +70°C unless otherwise noted.)

Read

Symbol	Characteristic	S6854		S68A54		S68B54		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYC}	Enable Cycle Time	1.0		0.666		0.50		μs
PW_{EH}	Enable Pulse Width, High	0.45		0.28		0.22	25	μs
PW_{EL}	Enable Pulse Width, Low	0.43		0.28		0.21		μs
t_{AS}	Setup Time, Address and R/W Valid to Enable Positive Transition	160		140		70		ns
t_{DDR}	Data Delay Time		320		220		180	ns
t_H	Data Hold Time	10		10		10		ns
t_{AH}	Address Hold Time	10		10		10		ns
t_{Er}, t_{Ef}	Rise and Fall Time for Enable Input		25		25		25	ns

Write

Symbol	Characteristic	S6850		S68A50		S68B50		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYCE}	Enable Cycle Time	1.0		0.666		0.50		μs
PW_{EH}	Enable Pulse Width, High	0.45		0.28		0.22		μs
PW_{EL}	Enable Pulse Width, Low	0.43		0.28		0.21		μs
t_{AS}	Setup Time, Address and R/W Valid to Enable Positive Transition	160		140		70		ns
t_{DSW}	Data Setup Time	195		80		60		ns
t_H	Data Hold Time	10		10		10		ns
t_{AH}	Address Hold Time	10		10		10		ns
t_{Er}, t_{Ef}	Rise and Fall Time for Enable Input		25		25		25	ns

Figure 1. Bus Timing Test Loads

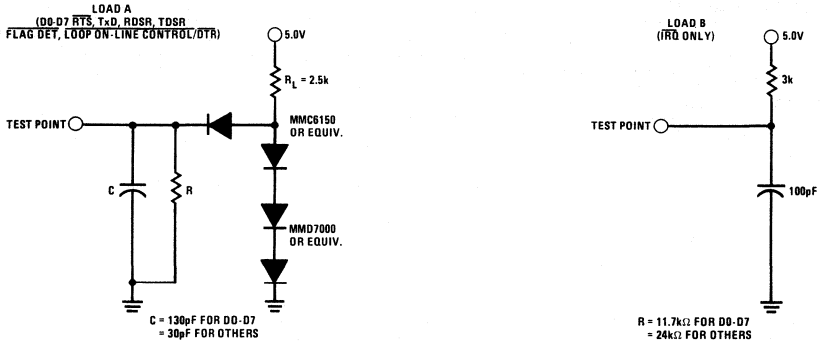


Figure 2. Receiver Data Setup/Hold, Flag Detect and Loop On-Line Control Delay Timing

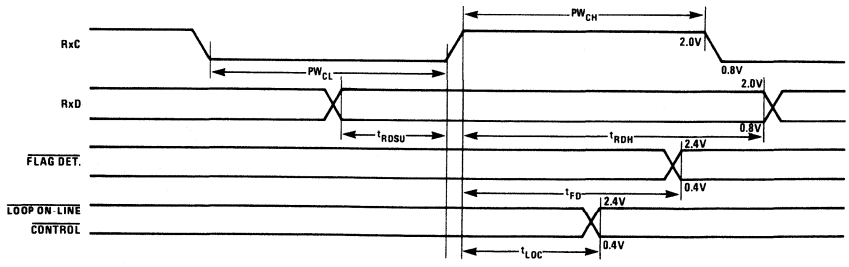


Figure 3. Transmit Data Output Delay and Request to Send Delay Timing

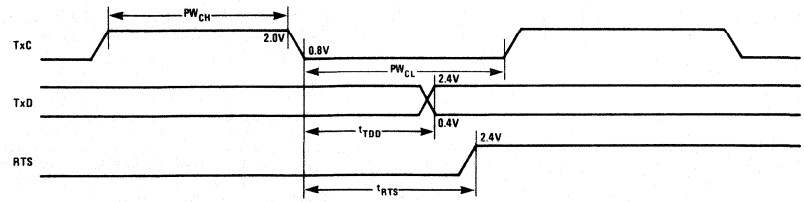


Figure 4. TDSR/RDSR Delays, IRQ Release Delay, RTS and DTR Delay Timing

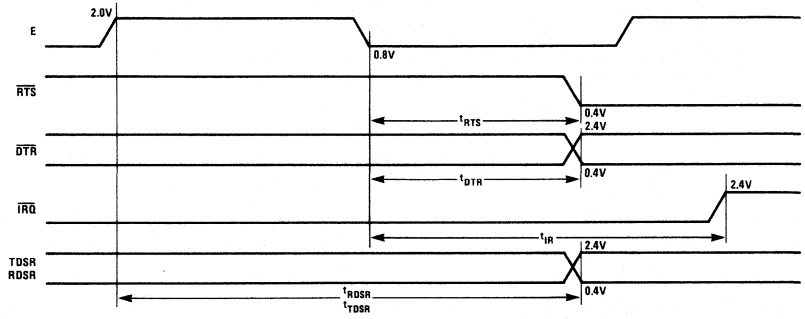
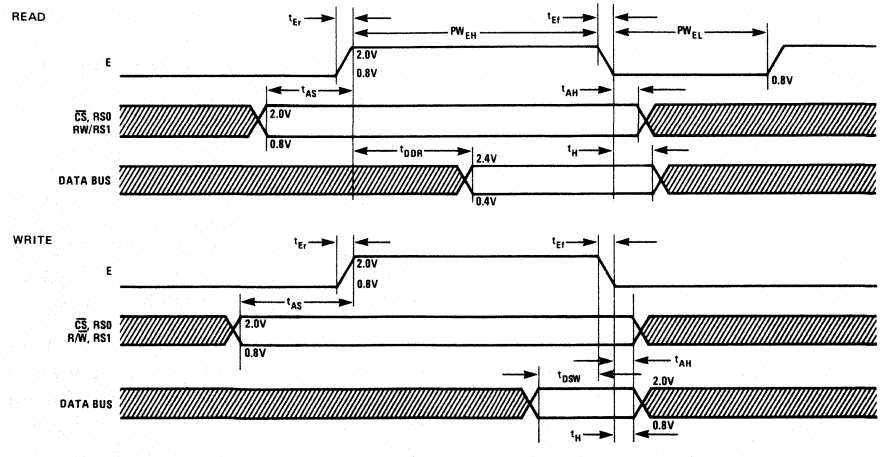


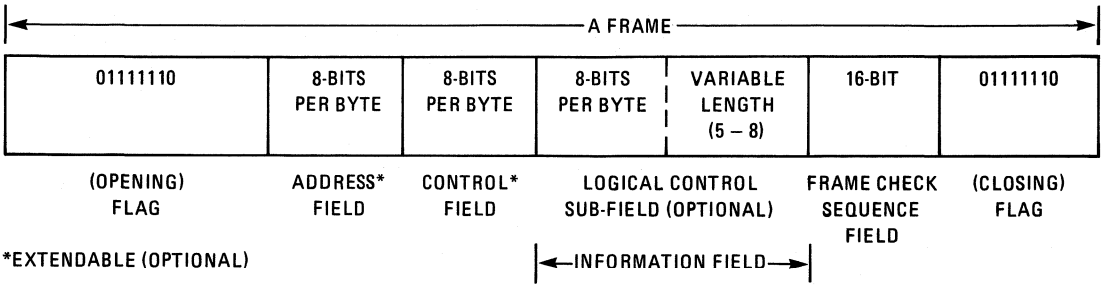
Figure 5. Bus Read/Write Timing Characteristics



Frame Format

The ADLC transmits and receives data (information or control) in a format called a frame. All frames start with an opening flag (F) and end with a closing flag (F). Between the opening flag and closing flag, a frame contains an address field, control field, information field, and frame check sequence field.

Figure 6. Data Format of a Frame



Flag (F) — The flag is the unique binary pattern (01111110). It provides the frame boundary and a reference for the position of each field of the frame.

The ADLC transmitter generates a flag pattern internally and the opening flag and closing flags are appended to a frame automatically. Two successive frames can share one flag for a closing flag of the first frame and for the opening flag of the next frame, if the "FF/F" control bit in the control register is reset.

The receiver searches for a flag on a bit by bit basis and recognizes a flag at any time. The receiver establishes the frame synchronization with every flag. The flags mark the frame boundary and reference for each field but they are not transferred to the Rx FIFO. The detection of a flag is indicated by the Flag Detect output and by a status bit in the status register.

Order of Bit Transmission — Address, control and information field bytes are transferred between the MPU and the ADLC in parallel by means of the data bus. The bit on D0 (data bus bit 0, pin 22) is serially transmitted first, and the first serially received bit is transferred to the MPU on D0. The FCS field is transmitted and receives MSB first.

Address (A) Field — The 8 bits following the opening flag are the address (A) field. The A-field can be extendable if the Auto-Address Extend Mode is selected in control register #3. In the Address Extend Mode, the first bit (bit 0) in every address octet becomes the extend control bit. When the bit is "0", the ADLC assumes another address octet will follow, and when the bit is "1", the address extension is terminated. A "null" address (all "0's") does not extend. In the receiver, the Address Present status bit distinguishes the address field from other fields. When an address byte is available to be read in the receive FIFO register, the Address Present status bit is set and causes an interrupt (if enabled). The Address Present bit is set for every address octet when the Address Extend Mode is used.

Control (C) Field — The 8 bits following the address field is the control (link control) field. When the Extended Control Field bit in control register #3 is selected, the C-field is extended to 16 bits.

Information (I) Field — The I-field follows the C-field and precedes the FCS field. The I-field contains "data" to be transferred but is not always necessarily contained in every frame. The word length of the I-field can be selected from 5 to 8 bits per byte by control bits in control register #4. The I-field will continue until it is terminated by the FCS and closing flag. The receiver has the capability to handle a "partial" last byte. The last information byte can be any word length between 1 and 8 bits. If the last byte in the I-field is less than the selected word length, the receiver will right justify the received bits, fill the remaining bits of the receiver shift register with zeros, and transfer a full byte to the Rx FIFO. Regardless of selected byte length, the ADLC will transfer 8 bits of data to the data bus. Unused bits for word lengths of 5, 6, and 7 will be zeroed.

Logical Control (LC) Field — When the Logical control Field Select bit in control register #3 is selected, the ADLC separates the I-field into two sub-fields. The first sub-field is the Logical Control field and the following sub-field is the "data" portion of the I-field. The logical control field is 8 bits and

follows the C-field, which is extendable by octets, if it is selected. The last bit (bit 7) is the extend control bit, and if it is a "1", the LC-field is extended one octet.

Note: Hereafter the word "Information Field" or "I-field" is used as the data portion of the information field, and excludes the logical control field. This is done in order to keep the consistency of the meaning of "Information Field" as specified in SDLC, HDLC, and ADCCP standards.

Frame Check Sequence (FCS) Field — The 16 bits preceding the closing flag is the FCS field. The FCS is the "cyclic redundancy check character (CRCC)". The poly-nomial $x^{16} + x^{12} + x^5 + 1$ is used both for the transmitter and receiver. Both the transmitter and receiver poly-nominal registers are initialized to all "1"s prior to calculation of the FCS. The transmitter calculates the FCS on all bits of the address, control, logical control (if selected), and information fields, and transmits the complement of the resulting remainder as FCS. The receiver performs the similar computation on all bits of the address, control, logical control (if selected), information, and received FCS fields and compares the result to F0B8 (Hexadecimal). When the result matches F0B8, the Frame Valid status bit is set in the status register. If the result does not match, the Error status bit is set. The FCS generation, transmission, and checking are performed automatically by the ADLC transmitter and receiver. The FCS field is not transferred to the Rx FIFO.

Invalid Frame — Any valid frames should have at least the A-field, C-field and FCS field between the opening flag and the closing flag. When invalid frames are received, the ADLC handles them as follows:

1) A short frame which has less than 25 bits between flags — The ADLC ignores the short frame and its reception is not reported to the MPU.
2) A frame less than 32 bits between the flags, or a frame 32 bits or more with an extended A-field or C-field that is not completed. — This frame is transferred into the Rx FIFO. The FCS/IF Error status bit indicates the reception of the invalid frame at the end of the frame.
3) Aborted Frame— The frame which is aborted by receiving an abort or DCD failure is also an invalid frame. Refer to "Abort" and "DCD status bit."

Zero Insertion and Zero Deletion — The Zero insertion and deletion, which allows the content of the frame to be transparent, are performed by the ADLC automatically. A binary 0 is inserted by the transmitter after any succession of 5 1's within a frame (A, C, LC, I, and FCS field). The receiver deletes a binary 0 that follows successive 5 continuous 1's within a frame.

Abort — The function of prematurely terminating a data link is called "abort". The transmitter aborts a frame by sending at least 8 consecutive 1's immediately after the Tx Abort control bit in control register #4 is set to a "1". (Tx FIFO is also cleared by the Tx Abort control bit at the same time.) The abort can be extended up to (at least) 16 consecutive 1's, if the Abort Extend control bit in the control register #4 is set when an abort is sent. This feature is useful to force mark idle transmission. Reception of 7 or more consecutive 1's is interpreted as an abort by the receiver. The receiver responds to a received abort as follows:

1) An abort in an "out of frame" condition — An abort during the idle or time fill has no meaning. The abort reception is indicated in the status register as long as the abort condition continues; but neither an interrupt nor a stored condition occurs. The abort indication is suppressed after 15 or more consecutive 1's are received (Received Idle status is set).
2) An abort "in frame" after less than 26 bits are received after an opening flag — Under this condition, any field of the aborted frame has not transferred to the MPU yet. The ADLC clears the aborted frame data in the FIFO and clears flag synchronization. Neither an interrupt nor a stored status occurs. The status indication is the same as (1) above.
3) An abort "in frame" after 26 bits or more are received after an opening flag — Under this condition, some fields of the aborted frame might have been transferred onto the data bus. The abort status is stored in the receiver status register and the data of the aborted frame in the ADLC is cleared. The synchronization is also cleared.

Idle and Time Fill — When the transmitter is in an "out of frame" condition (the transmitter is not transmitting a frame), it is in an idle state. Either a series of contiguous flags (time fill) or a mark idle

(consecutive 1's on a bit by bit basis) is selected for the transmission in an idle state by the Flag/Mark Idle control bit. When the receiver receives 15 or more consecutive 1's, the Receive Idle status bit is set and causes an interrupt. The flags and mark idle are not transferred to the Rx FIFO.

Operation

Initialization — During a power-on sequence, the ADLC is reset via the $\overline{\text{RESET}}$ input and internally latched in a reset condition to prevent erroneous output transitions. The four control registers must be programmed prior to the release of the reset condition. The release of the reset condition is performed via software by writing a "0" into the Rx RS control bit (receiver) and/or Tx RS control bit (transmitter). The release of the reset condition must be done after the $\overline{\text{RESET}}$ input has gone high.

At any time during operation, writing a "1" into the Rx RS control bit or TX RS control causes the reset condition of the receiver or the transmitter.

Transmitter Operation — The Tx FIFO register cannot be pre-loaded when the transmitter is in a reset state. After the reset release, the Flag/Mark Idle control bit selects either the mark idle state (inactive idle) or the Flag "time fill' (active idle) state.This active or inactive mark idle state will continue until data is loaded into the Tx FIFO.

The availability of the Tx FIFO is indicated by the TDRA status bit under the control of the 2-Byte/1-Byte control bit. TDRA status is inhibited by the Tx RS bit or $\overline{\text{CTS}}$ input being high. When the 1-Byte mode is selected, one byte of the FIFO is available for data transfer when TDRA goes high. When the 2-Byte mode is selected, two successive bytes can be transferred when TDRA goes high.

The first byte (Address field) should be written into the Tx FIFO at the "Frame Continue" address. Then the transmission of a frame automatically starts. If the transmitter is in a mark idle state, the transfer of an address causes an opening flag within two or three transmitter clock cycles. If the transmitter has been in a time fill state, the current time fill flag being transmitted is assumed as an opening flag and the address field will follow it.

A frame continues as long as data is written into the Tx FIFO at the "Frame Continue" address. The ADLC internally keeps track of the field sequence in the frame. The frame format is described in the "FRAME FORMAT" section.

The frame is terminated by one of two methods. The most efficient way to terminate the frames from a software standpoint is to write the last data character into the Transmit FIFO "Frame Terminate" address (RS1, RS0 = 11) rather than the Transmit FIFO "Frame Continue" address (RS1, RS0 = 10). An alternate method is to follow the last write of data in the Tx FIFO "Frame Continue" address with the setting of the Transmit Last Data control bit. Either method causes the last character to be transmitted and the FCS field to automatically be appended along with a closing flag. Data for a new frame can be loaded into the Tx FIFO immediately after the old frame data, if TDRA is high. The closing Flag can serve as the opening Flag of the next frame or separate opening and closing Flags may be transmitted. If a new frame is not ready to be transmitted, the ADLC will automatically transmit the Active (Flag) or Inactive (Mark) Idle condition.

If the Tx FIFO becomes empty at any time during frame transmission (the FIFO has no data to transfer into transmitter shift register during transmission of the last half of the next to last bit of a word), an underrun will occur and the transmitter automatically terminates the frame by transmitting an abort. The underrun state is indicated by the Tx Underrun status bit.

Any time the Tx ABORT Control bit is set, the transmitter immediately aborts the frame (transmits at least 8 consecutive 1's) and clears the Tx FIFO. If the abort Extend Control bit is set at the time, an idle (at least 16 consecutive 1's) is transmitted. An abort or idle in an "out of frame" condition can be useful to gain 8 or 16 bits of delay. (For an example, see "Programming Considerations.")

The $\overline{\text{CTS}}$ ($\overline{\text{Clear-To-Send}}$) input and $\overline{\text{RTS}}$ ($\overline{\text{Request-To-Send}}$) output are provided for a MODEM or other hardware interface.

The TDRA/FC status bit (when selected to be Frame Complete Status) can cause an interrupt upon frame completion (i.e., a flag or abort completion).

Details regarding the inputs and outputs, status bits, control bits, and FIFO operation are described in their respective sections.

Receiver Operation — Data and a pre-synchronized clock are provided to the ADLC receiver section by means of the Receive Data (RxD) and Receive Clock (RxC) inputs. The data is a continuous stream of binary bits with the characteristic that a maximum of five "1's" can occur in succession unless Abort, Flag,

Figure 7A. ADLC Transmitter State Diagram
C_1b_1 refers to control register bit

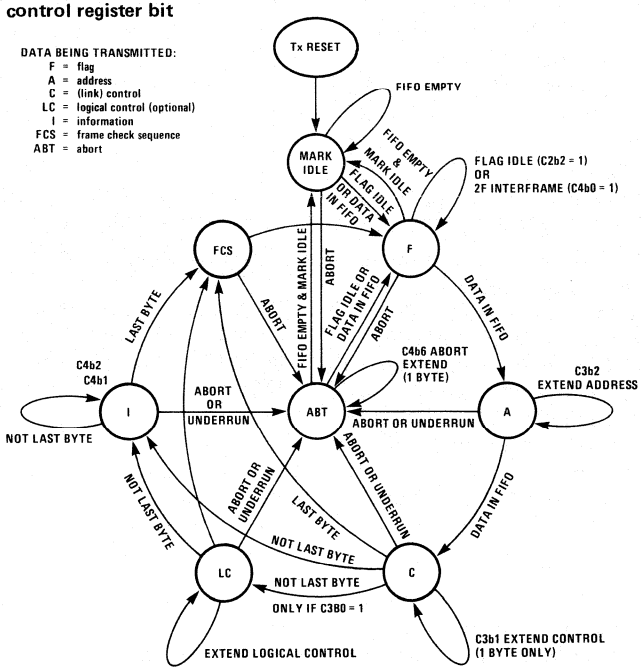
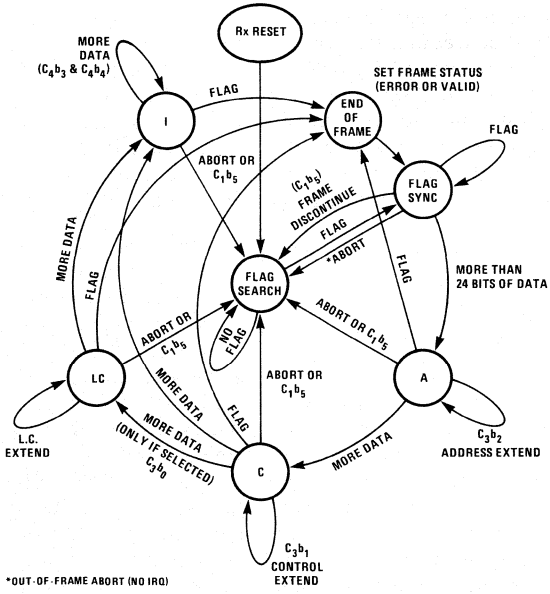


Figure 7B. ADLC Receiver State Diagram



Operation (Continued)

or Idling condition occurs. The receiver continuously (on a bit-by-bit basis) searches for Flags and Aborts.

When a flag is detected, the receiver establishes frame synchronization to the flag timing. If a series of flags is received, the receiver resynchronizes to each flag.

If the frame is terminated before the internal buffer time expires (the frame data is less than 25 bits after an opening flag), the frame is simply ignored. Noise on the data input (RxD) during time fill can cause this kind of invalid frame.

Once synchronization has been achieved and the internal buffer time (24 bit times) expires data will automatically transfer to the Rx Data FIFO. The Rx Data FIFO is clocked by E to cause received data to move through the FIFO to the last empty register location. The Receiver Data Available status bit (RDA) indicates when data is present in the last register (Reg. #3) for the 1 Byte Transfer Mode. The 2 Byte Transfer Mode causes the RDA status bit to indicate data is available when the last two FIFO register locations (Reg. #2 and #3) are full. If the data character present in the FIFO is an address octet the status register will exhibit an Address Present status condition. Data being available in the Rx Data FIFO causes an interrupt to be initiated (assuming the receiver interrupt is enabled, RIE = "1"). The MPU will read the ADLC Status Register as a result of the interrupt or in its turn in a polling sequence. RDA or Address Present will indicate that receiver data is available and the MPU should subsequently read the Rx Data FIFO register. The interrupt and status bit will then be reset automatically. If more than one character had been received and was resident in the Rx Data FIFO, subsequent E clocks will cause the FIFO to update and the RDA status bit and interrupt will again be SET. In the two byte transfer mode both data bytes may be read on consecutive E cycles. Address Present provides for 1 byte transfers only.

The sequence of each field in the received frame is automatically handled by the ADLC. The frame format is described in the "FRAME FORMAT" section.

When a closing flag is received, the frame is terminated. The 16 bits preceding the closing flag are regarded as the FCS and are not transferred to the MPU. Whatever data is present in the most significant byte portion of the receiver buffer register is right justified and transferred to the Rx FIFO. The frame boundary pointer, which is explained in the "Rx FIFO REGISTER" section, is set simultaneously in the Rx FIFO. The frame boundary pointer sets the Frame Valid status bit (when the frame was completed with no error) or the FCS/IF Error Status bit (when the frame was completed with error) when the last byte of the frame appears at the last location of the Rx FIFO. As long as the Frame Valid or FCS/IF Error status bit is set, the data transfer from the second location of the Rx FIFO to the last location of the Rx FIFO is inhibited.

Any time the Frame Discontinue control bit is set, the ADLC discards the current frame data in the ADLC without dropping flag synchronization. This feature can be used to ignore a frame which is addressed to another station.

The reception of an abort or idle is explained in the "FRAME FORMAT" section. The details regarding the inputs, outputs, status bits, control bits, and Rx FIFO operation are described in their respective sections.

Loop Mode Operation — The ADLC in the loop mode not only performs the transmission and receiving of data frames in the manner previously described but also has additional features for gaining and relinquishing loop control. In Figure 8a, a configuration is shown which depicts loop mode operation. The system configuration shows a primary station and several secondary stations. The loop is always under control of the primary station. When the primary wants to receive data, it transmits a Poll sequence and allows frame transmission to secondary stations on the loop. Each secondary is in series and adds one bit of delay to the loop. Secondary A in the figure receives data from the primary via its Rx Data Input, delays the data 1 bit, and transmits it to secondary B via its Tx Data Output. Secondaries B, C, and D operate in a similar manner. Therefore, data passes through each secondary and is received back by the primary controller.

Certain protocol rules must be followed in the manner by which the secondary station places itself on-loop (connects its transmitter output to the loop), goes active on the loop (starts transmitting its own stations' data on the loop), and goes off the loop (disconnects its transmitter output). Otherwise loop data to other stations down loop would be interfered. The data stream always flows the same way and the order in which secondary terminals are serviced is determined by the hardware configuration. The primary controller times the delay through the loop. Should it exceed n + 1 bit times, where n is the number of secondary terminals on the loop, it will indicate a loop failure. Control is transferred to a secondary by transmitting

Figure 8A. Typical Loop Configuration

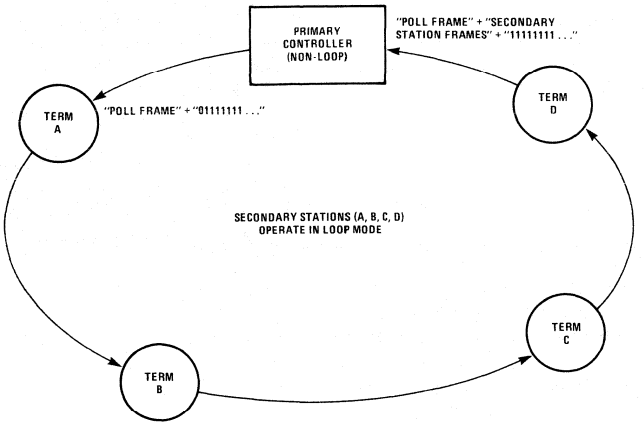
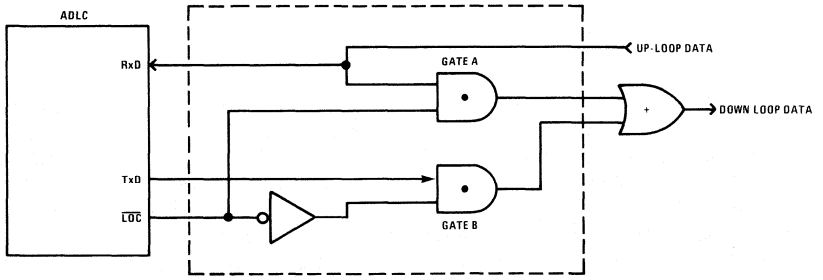


Figure 8B. Example of External Loop Logic



a "Go Ahead" signal following the closing Flag of a polling frame (request for a response from the secondary) from the primary station. The "Go Ahead" from the primary is a "0" and 7 "1's" followed by mark idling. The primary can abort its response request by interrupting its idle with flags. The secondary should immediately stop transmission and return control back to the primary. When the secondary completes its frame, a closing flag is transmitted followed by all "1"s. The primary detects the final 01111111 . . . ("Go Ahead" to the primary) and control is given back to the primary. Note that, if a down-loop secondary (e.g., station D) needs to insert information following an up-loop station (e.g., station A), the go ahead to station D is the last "0" of the closing flag from station A followed by "1's".

The ADLC in the primary station should operate in a non-loop, full duplex mode. The ADLC in the secondaries should operate in a loop mode, monitoring up-loop data on its receiver data input. The ADLC can recognize the necessary sequences in the data stream to automatically go on/off the loop and to insert its own station data. The procedure is the following and is summarized in Table 1.

Table 1. Summary of Loop Mode Operation

STATE	RX SECTION	TX SECTION	LOOP STATUS BIT
OFF-LOOP	Rx section receives data from loop and searches for 7 "1's" (when On-Loop Control bit set) to go ON-LOOP.	Inactive 1) NRZ MODE Tx data output is maintained "high" (mark). 2) NRZI MODE Tx data output reflects the Rx data input state delayed by one bit time. (Not normally connected to loop.) The NRZI data is internally decoded to provide error-free transitions to On-Loop mode.	"0"
ON-LOOP	1) When Go-Active on poll bit is set, Rx section searches for 01111111 pattern (the EOP or 'Go Ahead') to become the active terminal on the loop. 2) When On-Loop control bit is reset, Rx section searches of 8 "1's" to go OFF-LOOP.	Inactive 1) NRZ MODE Tx data output reflects Rx data input state delayed one bit time. 2) NRZI MODE Tx data output reflects Rx data input state delayed 2 bit times.	"1"
ACTIVE	Rx section searches for flag (an interrupt from the loop controller) at Rx data input. Received flag causes $\overline{FD}$ output to go low. IRQ is generated if $\overline{RIE}$ and FDSE control bits are set.	Tx data originates within ADLC until Go Active on Poll bit is reset and a flag or Abort is completed. Then returns to ON-LOOP state.	"0"

(1) Go On-loop — when the ADLC powers up, the terminal station will be off line. The first task is to become an active terminal on the loop. The ADLC must be connected to a Loop Link via an external switch as shown in Figure 8b. After hardware reset, the ADLC $\overline{LOC}/\overline{DTR}$ Output will be in the high state and the up-loop receive data repeated through gate A to the down Loop stations. Any Up-Loop transmission will be received by the ADLC. The Loop/Non-Loop Mode Control bit (bit 5 in Control Register 3) must be set to place the ADLC in the Loop Mode. The ADLC now monitors its Rx Data input for a string of seven consecutive "1's" which will allow a station to go on line. The Loop operation may be monitored by use of the Loop Status bit in Status Register 1. After power up and reset, this bit is a zero. When seven consecutive ones are received by the ADLC the $\overline{LOC}/\overline{DTR}$ output will go to a low level, disabling gate A (refer to Figure 8b), enabling gate B and connecting the ADLC Tx Data output to the down Loop stations. The up Loop data is now repeated to the down Loop stations via the ADLC. A one bit delay is inserted in the data (in NRZI mode, there will be a 2 bit delay) as it circulates through the ADLC. The ADLC is now on-line and the Loop Status bit in Status Register 1 will be at a one.

(2) Go Active after Poll — The receiver section will monitor the up link data for a general or addressed poll command and the Tx FIFO should be loaded with data so that when the go-ahead sequence of a zero followed by seven ones (01111111 ---) is detected, transmission can be initiated immediately. When the polling frame is detected, the Go-Active-On-Poll control bit must be set (bit 6 in Control Register 3). A minimum of seven bit times are available to set this control bit after the closing flag of the poll. When the Go-Ahead is detected by the receiver, the ADLC will automatically change the seventh one to a zero so that repeated sequence out gate B in Figure 8b is now opening flag sequence (01111110). Transmission now continues from the Tx FIFO with data (address, control, etc.) as previously described. When the ADLC has gone active-on-poll, the Loop Status bit in Status Register 1 will go to a zero. The receiver searches for a flag, which indicates that the primary station is interrupting the current operation.

(3) Go Inactive when On-Loop — The Go-Active-On Poll control bit may be RESET at any time during transmission. When the frame is complete (the closing Flag or abort is transmitted), the Loop is automatically released and the station reverts back to being

just a one bit delay in the Loop, repeating up link data. If the Go-Active-On-Poll control bit is not reset by software and the final frame is transmitted (Flag/Mark Idle bit = 0), then the transmitter will mark idle and will not release the loop to up-loop data. A Tx Abort command would have to be used in this case in order to go inactive when on the loop. Also, if the Tx FIFO was not preloaded with data (address, control, etc.) prior to changing the "Go Ahead Character" to a Flag, the ADLC will either transmit flags (active idle character) until data is loaded (when Flag/Mark Idle Control bit is high) or will go into an underrun condition and transmit an Abort (when Flag/Mark Idle control bit is low). When an abort is transmitted, the Go-Active-on-Poll control bit is reset automatically and the ADLC reverts to its repeating mode, (TxD = delayed RxD). When the ADLC transmitter lets go of the loop, the Loop Status bit will return to a "1", indicating normal on-loop retransmission of up-loop data.

4) Go Off-Loop — The ADLC can drop-off the Loop (go off-line) similar to the way it went on-line. When the Loop On-Line control bit is reset the ADLC receiver section looks for 8 successive "1's" before allowing the $\overline{LOC}/\overline{DTR}$ output to return high (the inactive state). Gate A in Figure 8b will be enabled and Gate B disabled allowing the loop to maintain continuity without disturbance. The Loop Status bit will show an off-line condition (logical zero).

Input/Output Functions

All inputs of ADLC are high impedance and TTL compatible level inputs. All outputs of the ADLC are compatible with standard TTL. Interrupt Request (IRQ), however, is an open drain output (no internal pull-up).

Interface for MPU

D0-D7

Bidirectional Data Bus — These data bus I/O ports allow the data transfer between ADLC and system bus. The data bus drivers are three-state devices that remain in the high impedance (off) state except when the MPU performs an ADLC read operation.

E

Enable Clock — E activates the address inputs ($\overline{CS}$, RS0 and RS1) and R/W input and enables the data transfer on the data bus. E also move data through the Tx FIFO and Rx FIFO. E should be a free running clock such as the S6800 MPU system clock.

$\overline{CS}$

Chip Select — An ADLC read or write operation is enabled only when the $\overline{CS}$ input is low and the E clock input is high. (E • $\overline{CS}$).

RS0
RS1

Register Selects — When the Register Select inputs are enabled by (E • $\overline{CS}$), they select internal registers in conjunction with the Read/Write input and Address Control bit (control register 1, bit 0). Register addressing is defined in Table 2.

R/W

Read/Write Control Line — The R/W input controls the direction of data flow on the data bus when it is enabled by (E · CS). When R/W is high, the I/O Buffer acts as an output driver and as an input buffer when low. It also selects the Read Only and Write Only registers within the ADLC.

$\overline{RESET}$

Reset Input — The $\overline{RESET}$ Input provides a means of resetting the ADLC from a hardware source. In the "low state," the $\overline{RESET}$ Input causes the following:

- ☐ Rx Reset and Tx Reset are SET causing both the Receiver and Transmitter sections to be held in a reset condition.
- ☐ Resets the following control bits: Transmit Abort, RTS, Loop Mode, and Loop On-Line/DTR.
- ☐ Clears all stored status condition of the status registers.
- ☐ Outputs: $\overline{RTS}$ and $\overline{LOC}/\overline{DTR}$ go high. TxD goes to the mark state ("1's" are transmitted).

When $\overline{RESET}$ returns "high" (the inactive state) the transmitter and receiver sections will remain in the reset state until Tx Reset and Rx Reset are cleared via the data bus under software control. The Control Register bits affected by $\overline{RESET}$ cannot be changed when $\overline{RESET}$ is "low".

$\overline{IRQ}$

Interrupt Request Output — $\overline{IRQ}$ will be low if an interrupt situation exists and the appropriate interrupt enable has been set. The interrupt remains as long as the cause for the interrupt is present and the enable is set.

Clock and Data of Transmitter and Receiver

TxC

Transmitter Clock Input — The transmitter shifts data

on the negative transition of the TxC clock input. When the Loop Mode or Test Mode is selected, TxC should be the same frequency and phase as the RxC clock. The data rate of the transmitter should not exceed the E frequency.

RxC

Receiver Clock Input — The receiver samples the data on the positive transition of the TxC clock. RxC should be synchronized with receive data externally.

TxD

Transmit Data Output — The serial data from the transmitter is coded in NRZ or NRZI (Zero Complement) data format.

RxD

Receiver Data Input — The serial data to be received by the ADLC can be coded in NRZ or NRZI (Zero Complement) data format. The data rate of the receiver should not exceed the E frequency. If a partial byte reception is possible at the end of a frame, the maximum data rate of the receiver is indicated by the following relationship:

$$f_{RxC} \leqslant \frac{1}{2t_E + 300ns}$$

where t_E is the period of E.

Peripheral/Modem Control

$\overline{RTS}$

Request to Send Output — The Request-to-Send output is controlled by the Request-to-Send control bit in conjunction with the state of the transmitter section. When the RTS bit goes high, the $\overline{RTS}$ output is forced low. When the RTS bit returns low, the $\overline{RTS}$ output remains low until the end of the frame. The positive transition of $\overline{RTS}$ occurs after the completion of a Flag, an Abort, or when the RTS control bit is reset during a mark idling state. When the $\overline{RESET}$ input is low, the $\overline{RTS}$ output goes high.

$\overline{CTS}$

Clear to Send Input — The $\overline{CTS}$ input provides a real-time inhibit to the TDRA status bit and its associated interrupt. The positive transition of $\overline{CTS}$ is stored within the ADLC to insure its occurrence will be acknowledged by the system. The stored CTS information and its associated IRQ (if enabled) are cleared by writing a "1" in the Clear Tx Status bit or in the Transmitter Reset bit.

$\overline{DCD}$

Data Carrier Detect Input — The $\overline{DCD}$ input provides a real-time inhibit to the receiver section. A high level on the $\overline{DCD}$ input resets and inhibits the receiver register, but data in the Rx FIFO from a previous frame is not disturbed. The positive transition of $\overline{DCD}$ is stored within the ADLC to insure that its occurrence will be acknowledged by the system. The stored DCD information and its associated IRQ (if enabled) are cleared by means of the Clear Rx Status Control bit or by the Rx Reset bit.

$\overline{LOC}/\overline{DTR}$

Loop On Line Control/Data Terminal Ready output — The $\overline{LOC}/\overline{DTR}$ output serves as a $\overline{DTR}$ output in the non-loop mode or as a Loop Control output in the loop mode. When $\overline{LOC}/\overline{DTR}$ output performs the $\overline{DTR}$ function, it is turned on and off by means of the LOC/DTR control bit. When the Loc/DTR control bit is high the $\overline{DTR}$ output will be low. In the loop mode the $\overline{LOC}/\overline{DTR}$ output provides the means of controlling the external loop interface hardware to go On-line or Off-line. When the LOC/DTR control bit is SET and the loop has "idled" for 7 bit times or more (RxD) = 01111111 . . .), the $\overline{LOC}/\overline{DTR}$ output will go low (on-line). When the LOC/DTR control bit is low and the loop has "idled" for 8 bit times or more, the $\overline{LOC}/\overline{DTR}$ output will return high (off-line). The $\overline{RESET}$ input being low will cause the $\overline{LOC}/\overline{DTR}$ output to be high.

$\overline{FD}$

Flag Detect Output — An output to indicate the reception of a flag and initiate an external time-out counter for the loop mode operation. The $\overline{FD}$ output goes low for one bit time beginning at the last bit of the flag character, as sampled by the receiver clock (RxC).

DMA Interface

RDSR

Receiver Data Service Request Output — The RDSR Output is provided primarily for use in DMA Mode operation and indicates (when high) that the Rx FIFO requests service (RSDR output reflects the RDA status bit). If the prioritized Status Mode is selected, RDSR will be inhibited when any other receiver status conditions are present. RDSR goes low when the Rx FIFO is read.

TDSR

Transmitter Data Service Request Output — The TDSR Output is proivded for DMA mode operation and indicates (when high) that the Tx FIFO requests

service (TDSR reflects the TDRA status bit). TDSR goes low when the Tx FIFO is loaded. TDSR is inhibited by: The Tx Rs control bit being SET, $\overline{\text{RESET}}$ being low, or $\overline{\text{CTS}}$ being high. If the prioritized status mode is used, Tx underrun also inhibits TDSR.

AMERICAN MICROSYSTEMS, INC.

ADVANCED PRODUCT DESCRIPTION

S68488

GENERAL PURPOSE INTERFACE ADAPTER

Features

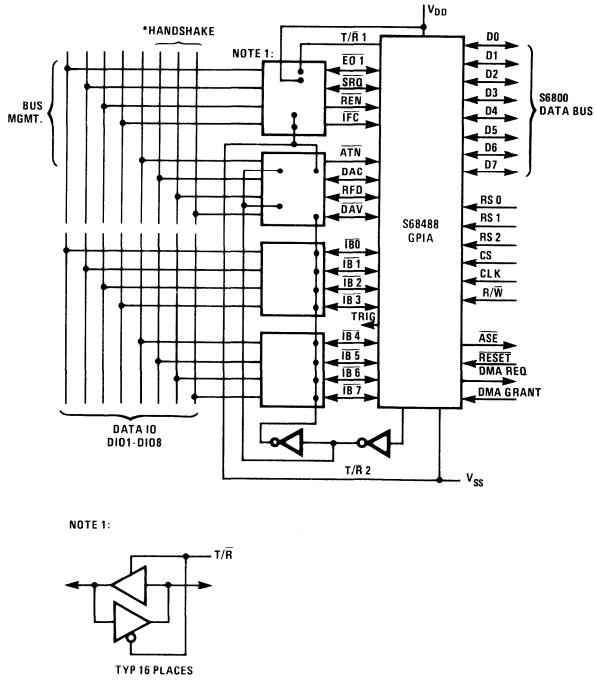
- ☐ Single or Dual Primary Address Recognition
- ☐ Secondary Address Capability
- ☐ Complete Source and Acceptor Handshakes
- ☐ Programmable Interrupts
- ☐ RFD Holdoff to Prevent Data Overrun
- ☐ Operates with DMA Controller
- ☐ Serial and Parallel Polling Capability
- ☐ Talk-Only or Listen-Only Capability
- ☐ Selectable Automatic Features to Minimize Software
- ☐ Synchronization Trigger Output
- ☐ S6800 Bus Compatible

General Description

The S68488 GPIA provides the means to interface between the IEEE488 standard instrument bus and the S6800. The 488 instrument bus provides a means for controlling and moving data from complex systems of multiple instruments.

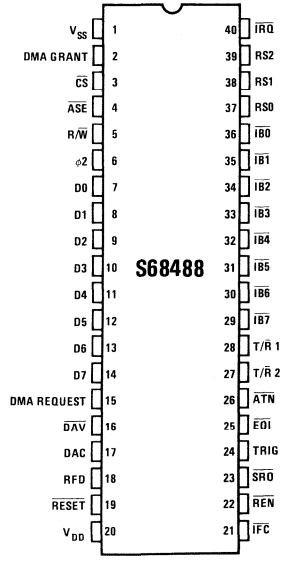
The S68488 will automatically handle all handshake protocol needed on the instrument bus.

Block Diagram



*The 3-wire handshake described is the subject of patents owned by Hewlett-Packard Co.

Pin Configuration



Functional Description

The IEEE 488 instrument bus standard is a bit-parallel, byte-serial bus structure designed for communiation to and from intelligent instruments. Using this standard, many instruments may be interconnected and remotely and automatically controlled or programmed. Data may be taken from, sent to, or transferred between instruments. A bus controller dictates the role of each device by making the attention line true and sending talk or listen addresses on the instrument bus data lines; those devices which have matching addresses are activated. Device addresses are set into each GPIA from switches or jumpers on a PC board by a microprocessor as a part of the initialization sequence.

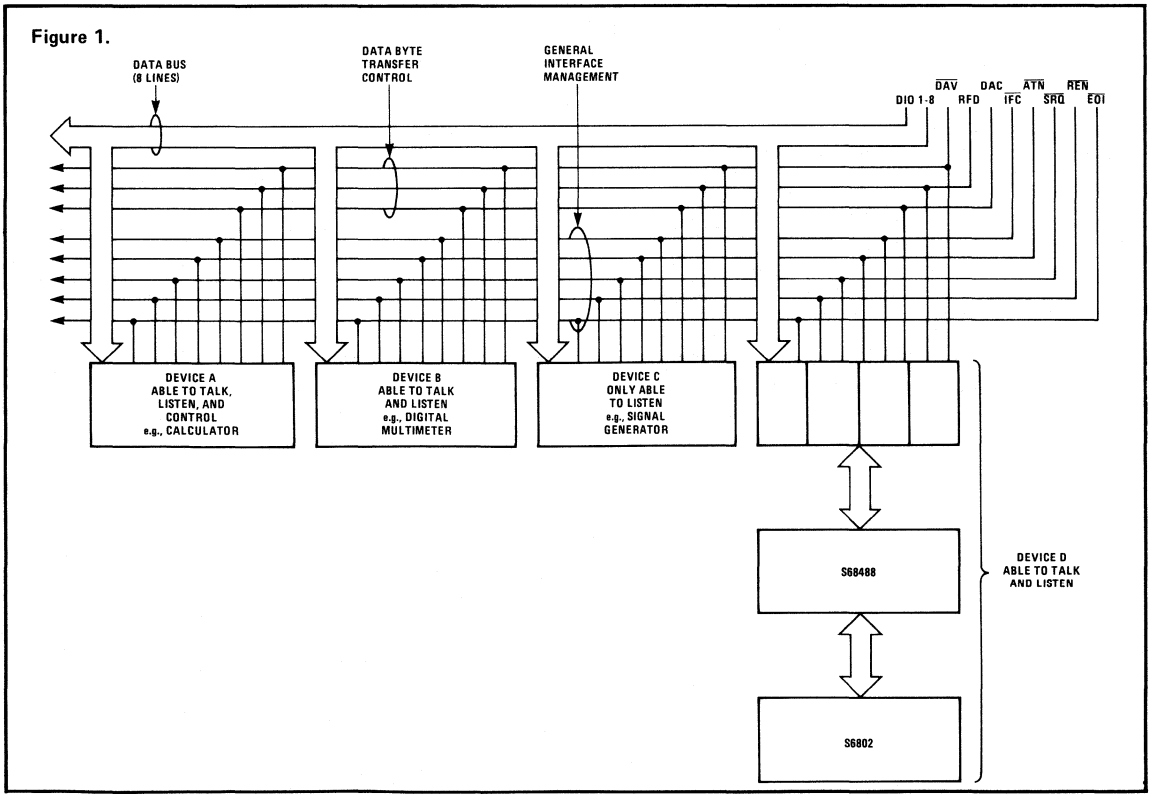
When the controller makes the attention line true, instrument bus commands may also be sent to single or multiple GPIAs.

Information is transmitted on the instrument bus data lines under sequential control of the three handshake lines. No step in the sequence can be initiated until the previous step is completed. Information transfer can proceed as fast as the devices can respond, but no faster than the slowest device presently addressed as active. This permits several devices of different speeds to receive the same data concurrently.

The GPIA is designed to work with standard 488 bus driver Ics (S3448As) to meet the complete electrical specifications of the IEEE488 bus. Additionally, a powered-off instrument may be powered-on without disturbing the 488 bus. With some additional logic, the GPIA could be used with other microprocessors.

The S68488 GPIA has been designed to interface between the S6800 microprocessor and the complex protocol of the IEEE488 instrument bus. Many instrument bus protocol functions are handled automatically by the GPIA and require no additional MPU action. Other functions require minimum MPU response due to a large number of internal registers conveying information on the state of the GPIA and the instrument bus.

Figure 1.



Maximum Ratings

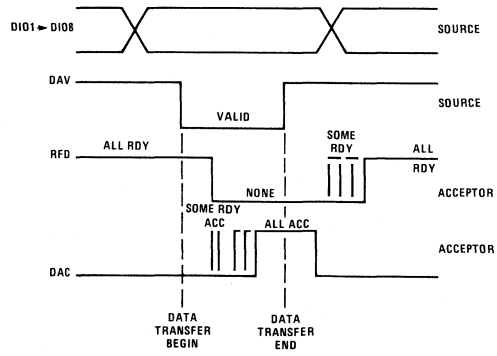
Supply Voltage	-0.3Vdc to +7.0Vdc
Input Voltage	-0.3Vdc to +7.0Vdc
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	-55°C to +150°C
Thermal Resistance	+82.5°C/W

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

Electrical Characteristics (V_{CC} = 5.0V ±5%, V_{SS} = 0, T_A = 0°C to +70°C unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{IH}	Input High Voltage	V_{SS} + 2.0		V_{CC}	Vdc	
V_{IL}	Input Low Voltage	V_{SS} - 0.3		V_{SS} + 0.8		
I_{IN}	Input Leakage Current		1.0	2.5	μAdc	V_{IN} = 0 to 5.25V
I_{TSI}	Three-State (Off State) Input Current D0-D7		2.0	10	μAdc	V_{IN} = 0.4 to 2.4V
V_{OH}	Output High Voltage D0-D7	V_{SS} + 2.4			Vdc	I_{load} = -205μA
V_{OL}	Output Low Voltage D0-D7 $\overline{IRQ}$			V_{SS} + 0.4 V_{SS} + 0.4	Vdc	I_{load} = 1.6mA I_{load} = 3.2mA
I_{LOH}	Output Leakage Current (Off State) $\overline{IRQ}$		1.0	10	μAdc	V_{OH} = 2.4Vdc
P_D	Power Dissipation		600		mW	
C_{IN}	Input Capacitance D0-D7 All Others			12.5 7.5	pF	V_{IN} = 0, T_A = 25°C, f = 1.0MHz

Figure 2. Source and Acceptor Handshake



Bus Timing Characteristics

Read (See Figure 3)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{cycE}	Enable Cycle Time	1.0			μs	See Figure 3
PW_{EH}	Enable Pulse Width, High	0.45			μs	
PW_{EL}	Enable Pulse Width, Low	0.43			μs	
t_{AS}	Setup Time, Address and R/$\overline{W}$ valid to enable positive transition	160			ns	
t_{DDR}	Data Delay Time			320	ns	
t_H	Data Hold Time	10			ns	
t_{AH}	Address Hold Time	10			ns	
t_{Er}, t_{Ef}	Rise and Fall Time for Enable input			25	ns	

Write (See Figure 4)

t_{cycE}	Enable Cycle Time	1.0			μs	See Figure 4
PW_{EH}	Enable Pulse Width, High	0.45			μs	
PW_{EL}	Enable Pulse Width, Low	0.43			μs	
t_{AS}	Setup Time, Address and R/$\overline{W}$ valid to enable positive transition	160			ns	
t_{DSW}	Data Setup Time	195			ns	
t_H	Data Hold Time	10			ns	
t_{AH}	Address Hold Time	10			ns	
t_{Er}, t_{Ef}	Rise and Fall Time for Enable input			25	ns	

Output (See Figure 5)

t_{HD}	Output Delay Time			400	ns	$\overline{DAV}$, DAC, RFD, $\overline{EOI}$, $\overline{ATN}$ valid
$t_{T/\overline{R1}, 2D}$				400	ns	T/$\overline{R}$1, T/$\overline{R}$2 valid

Figure 3. Bus Read Timing Characteristics (Read Information from GPIA)

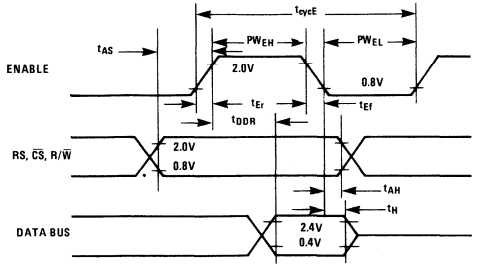


Figure 4. Bus Write Timing Characteristics (Write Information into GPIA)

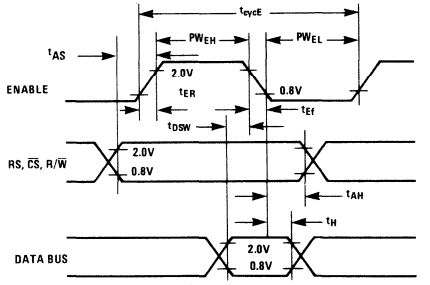
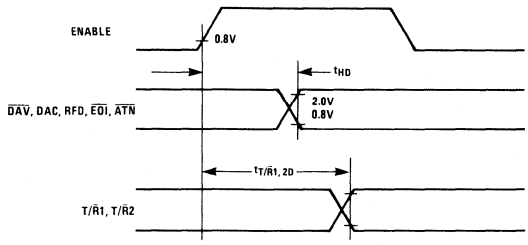


Figure 5. Output Bus Timing



A.C. Time Values

Symbol*	Parameter		Min.	Typ.	Max.	Unit	Conditions
T_1	Settling Time for Multiple Message	SH		⩾2		μs**	
t_2	Response to $\overline{ATN}$	SH, AH, T, L		⩽200		ns	
T_3	Interface Message Accept Time †	AH		>0		ϕ	
t_4	Response to $\overline{IFC}$ or $\overline{REN}$ False	T, TE, L, LE		<100		μs	
t_5	Response to $\overline{ATN} \bullet \overline{EOI}$	PP		⩽200		ns	

* Time values specified by a lower case t indicate the maximum time allowed to make a state transition. Time values specified by an upper case T indicate the minimum time that a function must remain in a state before exiting.

** If three-state drivers are used on the $\overline{DIO}$ – $\overline{DAV}$ and $\overline{EOI}$ lines, T_1 may be:
(1) ⩾1100ns
(2) Or ⩾700ns if it is known that within the controller $\overline{ATN}$ is driven by a three-state driver.
(3) Or ⩾500ns for all subsequent bytes following the first sent after each false transition of $\overline{ATN}$ [the first byte must be sent in accordance with (1) or (2)].

† Time required for interface functions to accept, not necessarily respond to interface messages.

ϕ Implementation dependent.

MPU bus clock rate – The current 6800 bus clock is ⩽ 1MHz but part should operate at 1.5MHz (design goal), with appropriate settling times (T1).

AMERICAN MICROSYSTEMS, INC.

ADVANCED PRODUCT DESCRIPTION

S6894

DATA ENCRYPTION UNIT

Features

- ☐ **Full Implementation of the NBS DES Algorithm**
- ☐ **A Complete Set of Operations, Including Encrypt Data, Decrypt Data, Enter New Key, Return Status, and Partial and Full Resets**
- ☐ **High-Speed Operation — Full Encryption or Decryption of a 64-Bit Data Block, Including All Command and Data Transfers, in 14.0ms.**
- ☐ **64-Bit Key Entry and Processing in 11.0ms, Including Odd Parity Checking of 8-Bit Key Data Bytes**
- ☐ **Simple Interface Through a General Purpose 8-Bit Paralled Digital I/O Port**

General Description

In addition, the AMI S6894 DEU offers an on-chip clock circuit, TTL-compatible I/O, single +5V power supply, in a two-chip set.

The 14.0ms data encryption/decryption time provided by the AMI DEU corresponds to a data rate in excess of 4600 bits-per-second in sustained operation. Allowing only 5% overhead for communications protocol control and checksum bits, this data rate is adequate to support a 4800 baud synchronous data link operated at 100% utilization. For start-stop asynchronous communications, the S6894 data rate is adequate to support lines with an aggregate transmission capacity in excess of 5700 baud. Two or more S6894 DEUs can be operated in parallel where higher data rates are required.

The encryption key is processed separately at the time it is entered. Once entered into S6894 DEU, an encryption key cannot be accessed by external means in either its original or processed form. Thus, security of the encryption key is fully protected. Each encryption key is entered only once — following a DEU reset, at DEU initialization, or when the key is to be changed. The entered key is then used for all subsequent data encryption and decryption operations.

Interface to the S6894 DEU is through a conventional general purpose 8-bit parallel I/O port. This allows the unit to be used with a wide range of host processors having different bus structures.

Other DEU Products

Although the S6894 DEU is the primary AMI NBS DES hardware product, other versions can be supplied at customer request. These include:

S6894-2 — Features and performance are identical to the S6894 DEU except that two encryption keys are accommodated. DEU encrypt and decrypt commands explicitly designate which key is to be used. Thus, the DEU-2 can serve two data paths having different encryption keys, can be used in the Master Key/Session Key mode, and so forth. Two new commands — Enter and Decrypt New Key, and Process New Key — are provided. These allow a new encrypted key to be decrypted under control of either existing key and then to replace either key, while prohitibing external access to the intermediate decrypted key value. The S6894-2 is implemented as a three-chip set that includes an S6810 RAM.

S6894-3 — Features and performances are identical to the S6894-2 DEU except that three encryption keys are accommodated. The S6894-3 consists of a four-chip set that includes two S5101 CMOS RAMs. An added feature is low power key data retention. During power-down conditions, all three encryption key values can be preserved using battery backup with only 0.1mW power drain. Preserved encryption keys are restored during power-on reset processing.

S6894-3A — Features are identical to the S6894-3 DEU in a two-chip set implementation. Data encryption and decryption times are 22.5ms, corresponding to a data rate in excess of 2800 bits-per-second in sustained operation. Low power data retention power requirements are less than 40mW.

Prices and delivery for all of the above DEUs will be quoted on request.

Customized Data Encryption Units

AMI DEU products can be customized to specific customer requirements in a number of ways. Protocols and conventions for transfer of data and command words between the controlling host processor and the DEU can be modified, and commands can be added or modified. For example, commands can be modified and added to facilitate Master/Session Key and/or Cypher Feedback (CFB) modes of operation. Further, the hardware interface can be modified or customized to meet specific application requirements. For example, the general purpose 8-bit parallel I/O port interface can be replaced — e.g., by a DMA interface or a custom LSI circuit — to precisely match the bus interface requirements of a particular host processor, to simplify DEU control and minimize host processor overhead, and/or to achieve maximum efficiency and speed in data and command word transfers.

AMI can also make available high-speed versions of any of the above DEUs. Because the object of such an implementation of the NBS DES is high performance, AMI plans at this time to offer high speed DEU products only in versions specifically customized to individual user requirements.

AMI will be pleased to work with interested customers in specifying and implementing customized versions of DEU products that meet requirements of specific applications.

AMERICAN MICROSYSTEMS, INC.

ADVANCED PRODUCT DESCRIPTION

S2811

SIGNAL PROCESSING PERIPHERAL

Features

- ☐ High Speed VMOS Technology
- ☐ Programmable for Digital Processing of Signals in Voice-Grade Communications Systems and Other Applications with Signals in the Audio Frequency Range
- ☐ Extremely Fast 12-Bit Parallel Multiplier On-Chip (300ns Max. Multiplication Time)
- ☐ Built-in Program ROM (256x17)*, 3-Port Data Memory (256x16) and Add/Subtract Unit (ASU)
- ☐ Pipeline Structure for High Speed Instruction Execution (300ns Max. Cycle Time)
- ☐ Bus-Oriented Parallel I/O for Easy Microprocessor Interface
- ☐ Additional Double Buffered I/O for Ease of Asynchronous Serial Interface
- ☐ On-Chip Crystal Oscillator (20MHz) Circuit
- ☐ Pre-Programmed Standard Parts to Be Announced Shortly

General Description

The S2811 Signal Processing Peripheral (SPP) is a high speed special purpose arithmetic processor with on-chip ROM, RAM, multiplier, adder/subtractor, accumulator and I/O organized in a pipeline structure to achieve an effective operation of one multiply, add and store of up to 12-bit numbers in 300 nanoseconds.

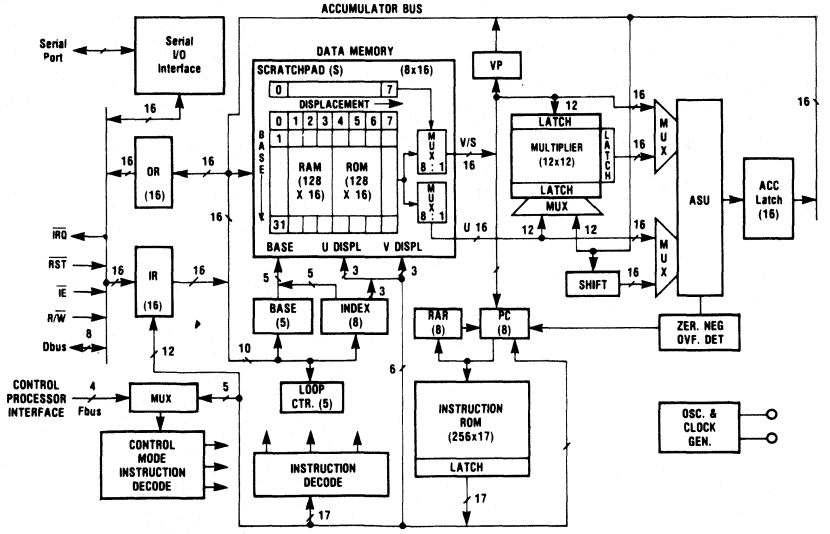
User Support

A real time in circuit emulator, the RTDS2811 is under development. This is a fully compatible hardware emulator with software assembler/disassembler and editor for rapid program development and debugging. An S2811 assembler ASMB2811, and a software simulator program package SSPP2811 are also scheduled for 1981.

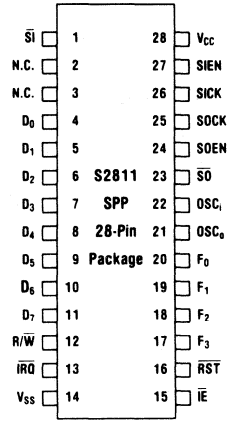
*Out of the 256 instruction locations of the ROM, 250 are usable by the user program. Six instruction locations are reserved for in-house testing.

S6800

Block Diagram



Pin Configuration



AMERICAN MICROSYSTEMS, INC.

ADVANCED PRODUCT DESCRIPTION

S2814A

FAST FOURIER TRANSFORMER

Features

- ☐ Performs 32 Complex Point Forward or Inverse FFT in 1.3msec, Using Decimation in Frequency (DIF)
- ☐ Transform Expandable either by Using Multiple S2814As (for Minimum Processing Time) or by a Single S2814A (for Minimum Hardware)
- ☐ Operates with any 8 or 16 Bit Microprocessor, including S6800 and S9900. Optional DMA Controller Increases Speed
- ☐ All Data I/O Carried Out on Microprocessor Data Bus
- ☐ Basic Resolution of 57dB. Optional Conditional Array Scaling (CAS) Routine Increases Dynamic Range to 70dB
- ☐ Optional Windowing Routine Incorporated to Permit Use of Arbitrary Weighting Function
- ☐ Coefficient Generation On Chip, with Rotation Algorithm for Transform Expansion up to 512 Points
- ☐ Based on AMI's Signal Processing Peripheral Chip (S2811) Using VMOS Technology to Achieve High Speed and Low Power Dissipation
- ☐ Optional Power Spectrum Computation

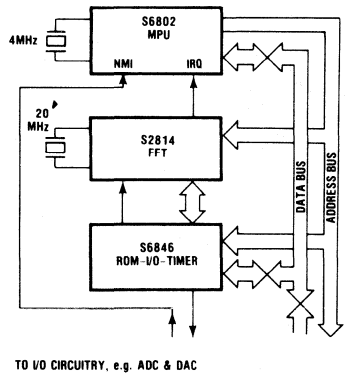
General Description

The AMI S2814A Fast Fourier Transformer is a preprogrammed version of the S2811 Signal Processing Peripheral. For further information on the internal operation of the S2811, please refer to the S2811 Advanced Product Description. It calculates FFTs and IFFTs using a decimation in frequency (DIF) technique for minimum distortion. The S2814A calculates a 32 complex point FFT using internally generated coefficients in a single pass. A coefficient rotation algorithm allows larger FFTs to be implemented (in blocks of 32 points). This implementation may be carried out by successive passes of the data through the two main routines in the S2814A, allowing larger transforms to be carried out with a single S2814A. Alternatively, an array of S2814As may be used to increase the transformation speed by parallel processing.

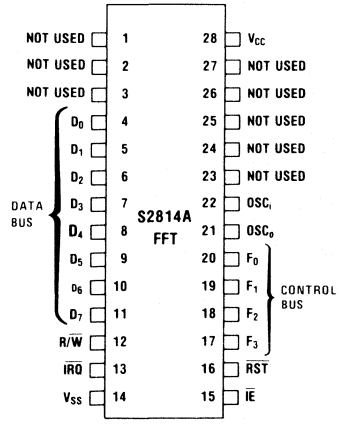
The word length used in the S2814A gives the transformed data a resolution of up to 57dB, but the total dynamic range can be increased up to 70dB by using the Conditional Array Scaling (CAS) routine incorporated.

The S2814A is intended to be used in a microprocessor system (see Block Diagram), using an 8 or 16 bit microprocessor, ROM, RAM and an optional DMA Controller or Address Generator. The S2814A is used as a

Block Diagram: Minimum System Configuration



Pin Configuration



memory mapped peripheral, and should be assigned a block of 16 addresses. It is used as a "hardware subroutine" function. The microprocessor controls the flow of data, including I/O, and calls the routines in the S2814A to cause the FFT to be executed. The S2814A responds to the microprocessor with the $\overline{IRQ}$ line when the processing of each routine is completed. In the case of a 32 point transform this signifies the completion of the transform, and in larger transforms it signifies that the microprocessor should unload the output data, load the next input data and call the next routine to be executed. The data is stored externally in RAM. Input data to be transformed is loaded into displacements 0 and 1 of the S2814A data memory. At the end of the FFT routine output data overwrites the input data. If power spectrum flag (PSF) is set, the S2814A computes the sum of the squares of the real and imaginary components of the output data and places the result in displacement 3 of the data memory. Both complex FFT data and power spectrum data are thus available. Windowing weights may be loaded into the S2814A prior to processing if the windowing routine is to be used. A 6800 compatible source listing of a suitable control program is available to the S2814A user at no charge. This control program will also be made available as a mask programmed ROM.

AMERICAN MICROSYSTEMS, INC.

S6810/S68A10/S68B10

128 X 8 STATIC READ/WRITE MEMORY

Features

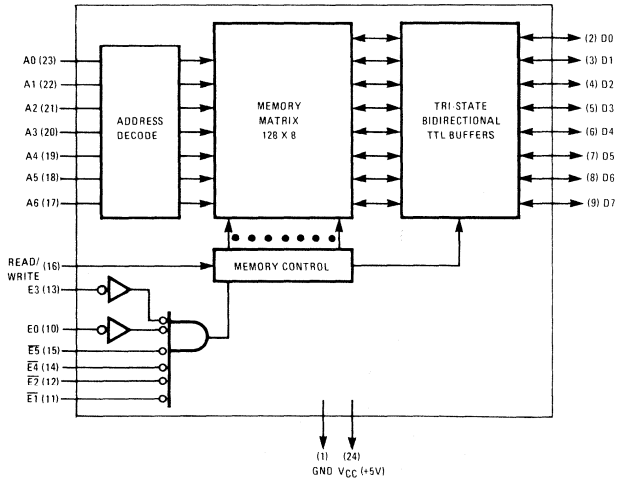
- ☐ **Organized as 128 Bytes of 8 Bits**
- ☐ **Static Operation**
- ☐ **Bidirectional Three-State Data Input/Output**
- ☐ **Six Chip Enable Inputs (Four Active Low, Two Active High**
- ☐ **Single 5 Volt Power Supply**
- ☐ **TTL Compatible**
- ☐ **Maximum Access Time**
  450ns for S6810
  360ns for S68A10
  250ns for S68B10

General Description

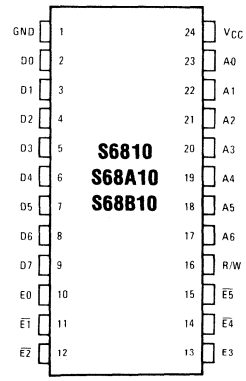
The S6810/S68A10 and S68B10 are static 128x8 Read/Write Memories designed and organized to be compatible with the S6800/S68A00 and S68B00 Microprocessors. Interfacing to the S6810/S68A10 and S68B10 consists of an 8-bit bidirectional data bus, seven address lines, a single Read/Write control line, and six chip enable lines, four negative and two positive.

For ease of use, the S6810/S68A10 and S68B10 are a totally static memory requiring no clocks or cell refresh. The S6810/S68A10 and S68B10 are fabricated with N-channel silicon gate depletion load technology to be fully DTL/TTL compatible with only a single +5 volt power supply required.

Block Diagram



Pin Configuration



Absolute Maximum Ratings

Supply Voltage	−0.3V to +7.0V
Input Voltage	−0.3V to +7.0V
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +150°C

D.C. Characteristics:

(V_{CC} = +5.0V ± 5%, V_{SS} = 0, T_A=0°C to 70°C unless otherwise noted.)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_{IN}	Input Current (A_n, R/W, CS_n, $\overline{CS_n}$)			2.5	μAdc	V_{IN} = 0V to 5.25V
V_{OH}	Output High Voltage	2.4			Vdc	I_{OH} = −205μA
V_{OL}	Output Low Voltage			0.4	Vdc	I_{OL} = 1.0mA
I_{LO}	Output Leakage Current (Three State)			10	μAdc	CS = 0.8V or $\overline{CS}$ = 2.0V, V_{OUT} = 0.4V to 2.4V
I_{CC}	Supply Current S6810 S68A10/S68B10			80 100	mAdc mAdc	V_{CC} = 5.25V, all other pins grounded, T_A = 0°C

A.C. Characteristics:

Read Cycle

(V_{CC} = +5.0V ± 5%, V_{SS} = 0,T_A=0°C to 70°C unless otherwise noted.)

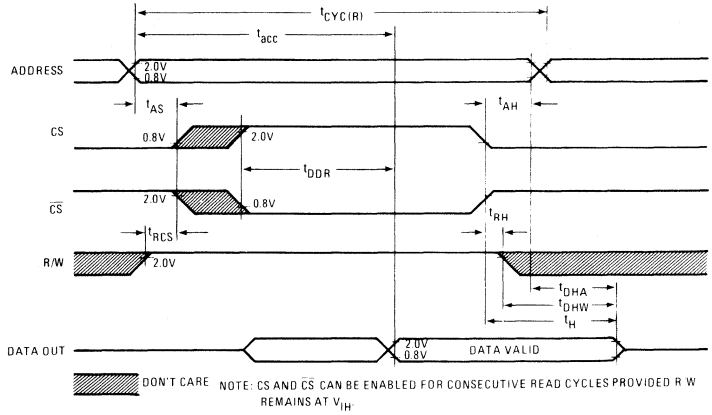
		S6810		S68A10		S68B10		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Units
$t_{cyc(R)}$	Read Cycle Time	450		360		250		ns
t_{acc}	Access Time		450		360		250	ns
t_{AS}	Address Setup Time	20		20		20		ns
t_{AH}	Address Hold Time	0		0		0		ns
t_{DDR}	Data Delay Time (Read)		230		220		180	ns
t_{RCS}	Read to Select Delay Time	0		0		0		ns
t_{DHA}	Data Hold from Address	10		10		10		ns
t_H	Output Hold Time	10		10		10		ns
t_{DHW}	Data Hold from Write	10	60	10	60	10	60	ns
t_{RH}	Read Hold from Chip Select	0		0		0		ns

Write Cycle

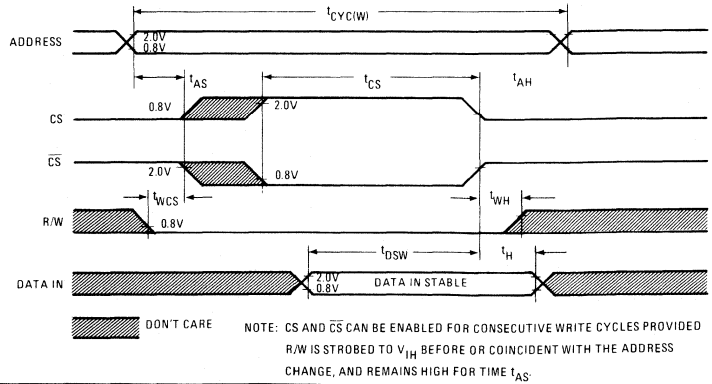
(V_{CC} = +5.0V ± 5%, V_{SS} = 0, T_A=0°C to 70°C unless otherwise noted.)

Symbol	Parameter	S6810		S68A10		S68B10		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{cyc(W)}$	Write Cycle Time	450		360		250		ns
t_{AS}	Address Setup Time	20		20		20		ns
t_{AH}	Address Hold Time	0		0		0		ns
t_{CS}	Chip Select Pulse Width	300		250		210		ns
t_{WCS}	Write to Chip Select Delay Time	0		0		0		ns
t_{DSW}	Data Setup Time (Write)	100		80		60		ns
t_H	Input Hold Time	10		10		10		ns
t_{WH}	Write Hold Time from Chip Select	0		0		0		ns

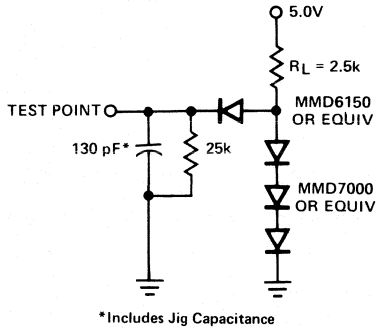
Read Cycle Timing



Write Cycle Timing



AC Test Load



*Includes Jig Capacitance

AMERICAN MICROSYSTEMS, INC.

S9900

High Performance Microprocessor Family

Contact factory for complete data sheet

S9900 Family Selection Guide

MICROPROCESSORS	
S9900	16-Bit Microprocessor
S9940	Single Chip Microcomputer 2K ROM, 128×8 RAM
S9980A/S9981	16-Bit Microprocessor 8-Bit Data Bus (S9981 has Internal Clock)
PERIPHERALS	
S9901	Programmable Systems Interface (PSI)
S9902	UART/Asynchronous Communications Controller (USRT/ACC)

AMERICAN MICROSYSTEMS, INC.

PRELIMINARY DATA SHEET

S9900

16-BIT MICROPROCESSOR

Features

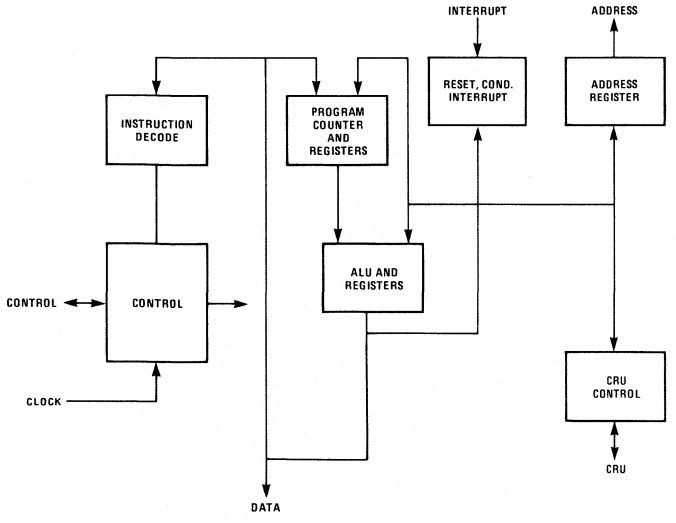
- ☐ **16-Bit Instruction Word**
- ☐ **Full Minicomputer Instruction Set Capability including Multiply and Divide**
- ☐ **Up to 65,536 Bytes of Memory**
- ☐ **3.3MHz Speed**
- ☐ **Advanced Memory-to-Memory Architecture**
- ☐ **Separate Memory, I/O and Interrupt-Bus Structures**
- ☐ **16 General Registers**
- ☐ **16 Prioritized Interrupts**
- ☐ **Programmed and DMA I/O Capability**
- ☐ **N-Channel Silicon-Gate Technology**

General Description

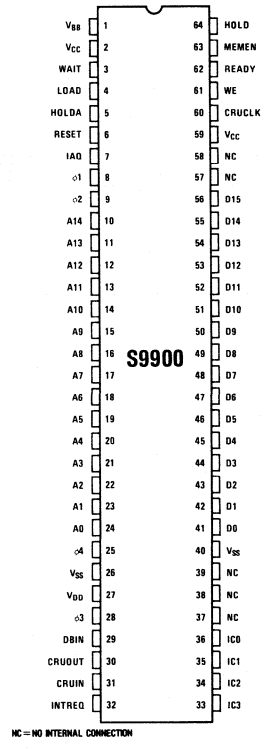
The S9900 microprocessor is a single-chip 16-bit central processing unit (CPU) produced using N-channel silicon-gate MOS technology. The instruction set of the S9900 includes the capabilities offered by full minicomputers. The unique memory-to-memory architecture features multiple register files, resident in memory, which allow faster response to interrupts and increased programming flexibility. The separate bus structure simplifies the system design effort. AMI provides a compatible set of MOS memory and support circuits to be used with an S9900 system. The system is fully supported by software and complete prototyping systems.

S9900

Block Diagram



Pin Configuration



NC = NO INTERNAL CONNECTION

S9900 Electrical and Mechanical Specifications

Absolute Maximum Ratings Over Operating Free-Air Temperature Range (unless otherwise noted)*

Supply Voltage, V_{CC} (See Note 1) ..... −0.3V to +20V
Supply Voltage, V_{DD} (See Note 1) ..... −0.3V to +20V
Supply Voltage, V_{SS} (See Note 1) ..... −0.3V to +20V
All Input Voltages (See Note 1) ..... −0.3V to +20V
Output Voltage (with Respect to V_{SS}) ..... −2V to +7V
Continuous Power Dissipation 1.2W
Operating Free-Air Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −55°C to +150°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Under absolute maximum ratings voltage values are with respect to the most negative supply, V_{BB} (substrate), unless otherwise noted. Throughout the remainder of this section, voltage values are with respect to V_{SS}.

Recommended Operating Conditions

Symbol	Parameter	Min.	Nom.	Max.	Unit	Conditions
V_{BB}	Supply voltage	-5.25	-5	-4.75	V	
V_{CC}	Supply voltage	4.75	5	5.25	V	
V_{DD}	Supply voltage	11.4	12	12.6	V	
V_{SS}	Supply voltage		0		V	
V_{IH}	High-level input voltage (all inputs except clocks)	2.2	2.4	V_{CC}+1	V	
$V_{IH(\phi)}$	High-level clock input voltage	V_{DD}-2		V_{DD}	V	
V_{IL}	Low-level input voltage (all inputs except clocks)	-1	0.4	0.8	V	
$V_{IL(\phi)}$	Low-level clock input voltage	-0.3	0.3	0.6	V	
T_A	Operating free-air temperature	0		70	°C	

Timing Requirements Over Full Range of Recommended Operating Conditions (See Figures 1 and 2)

Symbol	Parameter	Min.	Nom.	Max.	Unit	Conditions
$t_{c(\phi)}$	Clock cycle time	0.3	0.333	0.5	μs	
$t_{r(\phi)}$	Clock rise time	10	12		ns	
$t_{f(\phi)}$	Clock fall time	10	12		ns	
$t_{w(\phi)}$	Pulse width, any clock high	40	45	100	ns	
$t_{\phi 1L, \phi 2L}$	Delay time, clock 1 low to clock 2 low (time between clock pulses)	0	5		ns	
$t_{\phi 2L, \phi 3L}$	Delay time, clock 2 low to clock 3 low (time between clock pulses)	0	5		ns	
$t_{\phi 3L, \phi 4L}$	Delay time, clock 3 low to clock 4 low (time between clock pulses)	0	5		ns	
$t_{\phi 4L, \phi 1L}$	Delay time, clock 4 low to clock 1 low (time between clock pulses)	0	5		ns	
$t_{\phi 1H, \phi 2H}$	Delay time, clock 1 high to clock 2 high (time between leading edges)	73	83		ns	
$t_{\phi 2H, \phi 3H}$	Delay time, clock 2 high to clock 3 high (time between leading edges)	73	83		ns	
$t_{\phi 3H, \phi 4H}$	Delay time, clock 3 high to clock 4 high (time between leading edges)	73	83		ns	
$t_{\phi 4H, \phi 1H}$	Delay time, clock 4 high to clock 1 high (time between leading edges)	73	8		ns	
t_{su}	Data or control setup time before clock 1	30			ns	
t_h	Data hold time after clock 1	10			ns	

Electrical Characteristics Over Full Range of Recommended Operating Conditions (unless otherwise noted)

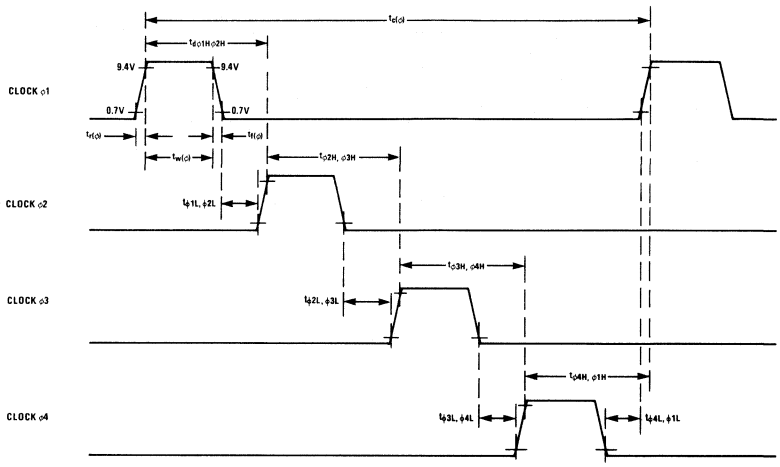
Symbol	Parameter		Min.	Typ.†	Max.	Unit	Conditions
I_I	Input current	Data Bus during DBIN		±50	±100	μA	$V_I = V_{SS}$ to V_{CC}
		$\overline{WE}$, $\overline{MEMEN}$, DBIN, Address bus, Data bus during HOLDA		±50	±100		$V_I = V_{SS}$ to V_{CC}
		Clock*		±25	±75		V_I = -0.3 to 12.6V
		Any other inputs		±1	±10		$V_I = V_{SS}$ to V_{CC}
V_{OH}	High-level output voltage		2.4		V_{CC}	V	I_O = -0.4mA
V_{OL}	Low-level output voltage				0.65 0.50	V	I_O = 32.mA I_O = 2mA
I_{BB}	Supply current from V_{BB}			0.1	1	mA	
I_{CC}	Supply current from V_{CC}			50	75	mA	
I_{DD}	Supply current from V_{DD}			25	45	mA	
C_i	Input capacitance (any inputs except clock and data bus)			10	15	pF	V_{BB} = -5, f = 1MHz, unmeasured pins at V_{SS}
$C_{i(\phi 1)}$	Clock-1 input capacitance			100	150	pF	V_{BB} = -5, f = 1MHz, unmeasured pins at V_{SS}
$C_{i(\phi 2)}$	Clock-2 input capacitance			150	200	pF	V_{BB} = -5, f = 1MHz unmeasured pins at V_{SS}
$C_{i(\phi 3)}$	Clock-3 input capacitance			100	150	pF	V_{BB} = -5, f = 1MHz, unmeasured pins at V_{SS}
$C_{i(\phi 4)}$	Clock-4 input capacitance			100	150	pF	V_{BB} = -5, f = 1MHz, unmeasured pins at V_{SS}
C_{DB}	Data bus capacitance			15	25	pF	V_{BB} = -5, f = 1MHz, unmeasured pins at V_{SS}
C_o	Output capacitance (any output except data bus)			10	15	pF	V_{BB} = -5, f = 1MHz, unmeasured pins at V_{SS}

†All typical values are at $T_A = 25°C$ and nominal voltages.
*D.C. Component of Operating Clock.

Switching Characteristics Over Full Range of Recommended Operating Conditions (See Figure 2)

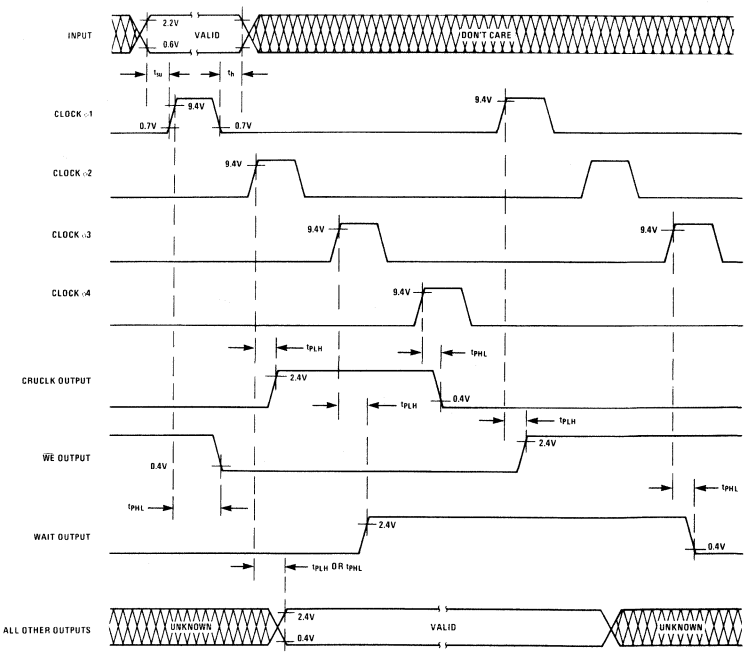
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{PLH} or t_{PHL}	Propagation delay time, clocks to outputs					C_L=200pF
	CRUCLK, WE, MEMEN, WAIT, DBIN			30	ns	
	All other outputs		20	40	ns	

Figure 1. Clock Timing



Note: All timing and voltage levels shown on ϕ1 apply to ϕ2, ϕ3, and ϕ4 in the same manner.

Figure 2. Signal Timing



†The number of cycles over which input/output data must/will remain valid can be determined from the number of wait states required for memory access. Note that in all cases data should not change during ϕ1.

AMERICAN MICROSYSTEMS, INC.

ADVANCED PRODUCT DESCRIPTION

S9901

PROGRAMMABLE SYSTEMS INTERFACE CIRCUIT

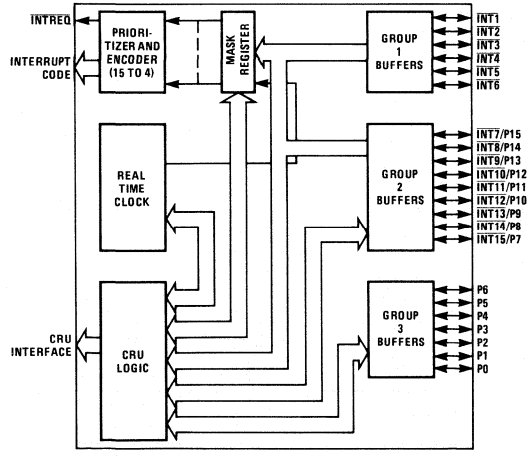
Features

- N-Channel Silicon-Gate Process
- 9900 Series CRU Peripheral
- Performs Interrupt and I/O Interface Functions
  - 6 Dedicated Interrupt Input Lines
  - 7 Dedicated I/O Ports
  - 9 Ports Programmable as Interrupts or I/O
- Easily Stacked for Interrupt and I/O Expansion
- Interval and Event Timer
- Single 5V Supply

General Description

The S9901 Programmable Systems Interface is a multifunctioned component designed to provide low cost interrupts and I/O ports in a 9900/9980 microprocessor system. It is fabricated with N-channel silicon-gate technology and is completely TTL compatible on all inputs including the power supply (+5V) and single-phase clock. Figure 1 is a block diagram of the S9901. The Programmable Systems Interface provides a 9900/9980 system with interrupt control, I/O ports, and a real-time clock as shown in Figure 2.

Figure 1. Block Diagram



S9901 Pin Configuration

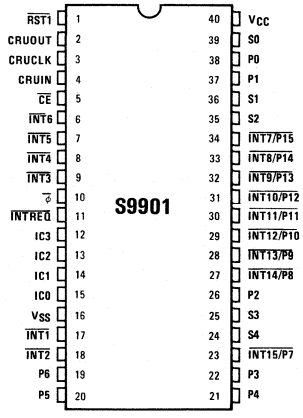
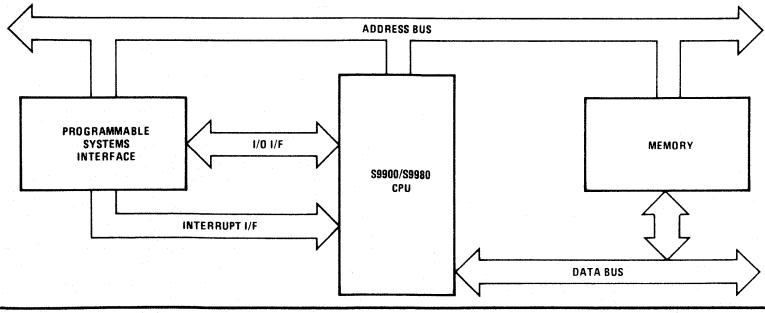


Figure 2. 9900/9980 System



S9901 Electrical Specifications

Absolute Maximum Ratings Over Operating Free Air Temperature Range (Unless Otherwise Noted)*

Supply Voltages, V_{CC} and V_{SS}	-0.3V to +10V
All Input and Output Voltages	-0.3V to +10V
Continuous Power Dissipation	0.75W
Operating Free-Air Temperature Range	0°C to +70°C
Storage Temperature Range	-65°C to +150°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute maximum rated conditions for extended period may affect device reliability.

Recommended Operating Conditions

Parameter	Min.	Nom.	Max.	Unit
Supply Voltage, V_{CC}	4.75	5	5.25	V
Supply Voltage, V_{SS}		0		V
High-Level Input Voltage, V_{IH}		2		V
Low-Level Input Voltage, V_{IL}		0.8		V
Operating Free-Air Temperature, T_A	0		70	°C

Electrical Characteristics Over Full Range of Recommended Operating Conditions (Unless Otherwise Noted)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
I_I	Input Current (Any Input)		±10		μA	V_I = 0V to V_{CC}
V_{OH}	High Level Output Voltage		2.4		V	I_{OH} = 100μA
			2		V	I_{OH} = -400μA
V_{OL}	Low Level Output Voltage		0.4		V	I_{OL} = 3.2mA
I_{CC}	Supply Current from V_{CC}		100		mA	
I_{SS}	Supply Current from V_{SS}		200		mA	
$I_{CC(av)}$	Average Supply Current from V_{CC}		60		mA	$t_{c(\phi)}$ = 333ns, T_A = 25°C
C_i	Capacitance, Any Input		10		pF	f = 1MHz,
C_o	Capacitance, Any Output		20		pF	All Other Pins at 0V

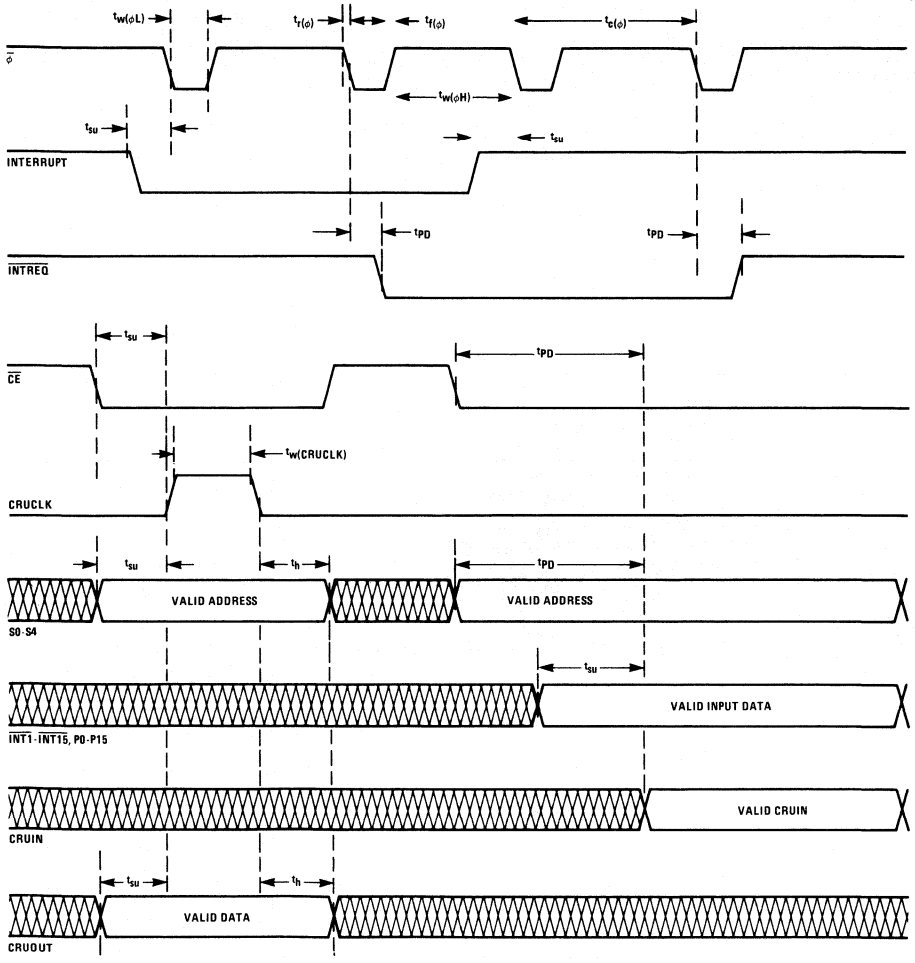
Timing Requirements Over Full Range of Operating Conditions

Symbol	Parameter	Min.	Nom.	Max.	Unit
$t_{c(\phi)}$	Clock Cycle Time		333		ns
$t_{r(\phi)}$	Clock Rise Time		10		ns
$t_{f(\phi)}$	Clock Fall Time		10		ns
$t_{w(\phi L)}$	Clock Pulse Low Width		55		ns
$t_{w(\phi H)}$	Clock Pulse High Width		240		ns
t_{su}	Setup Time for S0-S4, CE, or CRUOUT before CRUCLK		200		ns
t_{su}	Setup Time, Input Before Valid CRUIN		200		ns
t_{su}	Setup Time, Interrupt Before ϕ Low		40		ns
$t_{w(CRUCLK)}$	CRU Clock Pulse Width		100		ns
t_h	Address Hold Time		80		ns

Switching Characteristics Over Full Range of Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
t_{PD}	Propagation Delay, $\overline{\phi}$ Low to Valid $\overline{INTREQ}$, I_{C0}-I_{C3}		80		ns	C_L = 100pF, 2 TTL Loads
t_{PD}	Propagation Delay, S0-S4 or $\overline{CE}$ to Valid CRUIN		400		ns	C_L = 100pF

Figure 3. Switching Characteristics



NOTE 1: ALL TIMING MEASUREMENTS ARE FROM 10% and 90% POINTS

AMERICAN MICROSYSTEMS, INC.

ADVANCED PRODUCT DESCRIPTION

S9902

ASYNCHRONOUS COMMUNICATIONS CONTROLLER (ACC)

Features

- 5- to 8-Bit Character Length
- 1, 1 1/2, or 2 Stop Bits
- Even, Odd, or No Parity
- Fully Programmable Data Rate Generation
- Interval Timer with Resolution from 64 to 16,320 μs
- Fully TTL Compatible, Including Single Power Supply.

General Description

The S9902 Asynchronous Communication Controller (ACC) is a peripheral device for the S9900 family of microprocessors. The ACC provides an interface between the microprocessor and a serial asynchronous communication channel, performing the timing and data serialization and deserialization, thus facilitating the control of the asynchronous channel by the microprocessor.

Figure 1. Block Diagram

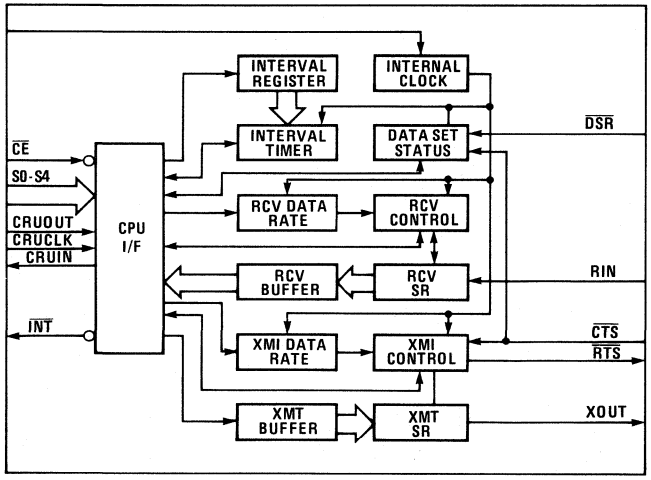
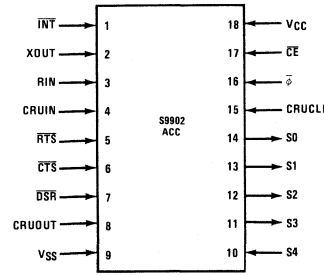


Figure 2. Pin Configuration



S9902 Electrical Specifications

Absolute Maximum Ratings Over Operating Free Air Temperature Range (Unless Otherwise Noted)*

Supply Voltage, V_{CC} ..... -0.3V to +10V
All Inputs and Output Voltages ..... -0.3V to +10V
Continuous Power Dissipation 0.7W
Operating Free-Air Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... -65°C to +150°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to Absolute Maximum Rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Min.	Nom.	Max.	Unit
Supply Voltage, V_{CC}	4.75	5	5.25	V
Supply Voltage, V_{SS}		0		V
High-Level Input Voltage, V_{IH}	2.2	2.4	V_{CC}	V
Low-Level Input Voltage, V_{IL}		0.4	0.8	V
Operating Free-Air Temperature, T_A	0		70	°C

Electrical Characteristics Over Full Range of Recommended Operating Conditions (Unless Otherwise Noted)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
I_I	Input Current (Any Input)			±10	μA	V_I = 0V to V_{CC}
V_{OH}	High-Level Output Voltage	2.2	3.0		V	I_{OH} = -100μA
		2.0	2.5			I_{OH} = -400μA
V_{OL}	Low-Level Output Voltage		0.4	0.85	V	I_{OL} = 3.2mA
$I_{CC(AV)}$	Average Supply Current from V_{CC}		2.5	100	mA	$t_{c(\phi)}$ = 250ns, T_A = 25°C
C_i	Capacitance, Any Input		10		pF	f = 1 MHz,
C_o	Capacitance, Any Output		20			All other pins at 0V

Timing Requirements Over Full Range of Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
$t_{c(\phi)}$	Clock Cycle Time	300	333	2000	ns
$t_{r(\phi)}$	Clock Rise Time		10	12	ns
$t_{f(\phi)}$	Clock Fall Time		10	12	ns
$t_{H(\phi)}$	Clock Pulse Width (High Level)		225	240	ns
$t_{L(\phi)}$	Clock Pulse Width (Low Level)		45	55	ns
$t_{su(ad)}$	Setup Time for Address and CRUOUT Before CRUCLK		220		ns
$t_{su(CE)}$	Setup Time for CE Before CRUCLK		190		ns
t_{HD}	Hold Time for Address, CE and CRUOUT After CRUCLK		90		ns
t_{wcc}	CRUCLK Pulse Width		120		ns

S9902 Pin Description

Table 1 defines the S9902 pin assignments and describes the function of each pin as shown in Figure 2.

Table 1

Signature	Pin	I/O	Description
$\overline{INT}$	1	O	Interrupt — when active (low), the $\overline{INT}$ output indicates that at least one of the interrupt conditions has occured.
XOUT	2	O	Transmitter serial data output line — XOUT remains inactive (high) when S9902 is not transmitting.
RIN	3	I	Receiver serial data input line — RCV — must be held in the inactive (high) state when not receiving data. A transition from high to low will activate the receiver circuitry.
CRUIN	4	O	Serial data output pin from S9902 to CRUIN input pin of the CPU.
$\overline{RTS}$	5	O	Request-to-send output from S9902 to modem. This output is enabled by the CPU and remains active (low) during transmission from the S9902.
$\overline{CTS}$	6	I	Clear-to-send input from modem to S9902. When active (low), it enables the transmitter section of S9902.
$\overline{DSR}$	7	I	Data set ready input from modem to S9902. This input generates an interrupt when going On or Off.
CRUOUT	8	I	Serial data input line to S9902 from CRUOUT line of the CPU.
V_{SS}	9	I	Ground reference voltage.
S4 (LSB)	10	I	
S3	11	I	
S2	12	I	
S1	13	I	Address bus S0-S4 are the lines that are addressed by the CPU to select a
S0	14	I	particular S9902 function.
CRUCLK	15	I	CRU Clock. When active (high), S9902 from CRUOUT line of the CPU.
$\overline{\phi}$	16	I	TTL Clock.
$\overline{CE}$	17	I	Chip enable — when CE is inactive (high), the S9902 address decoding is inhibited which prevents execution of any S9902 command function. CRUIN remains at high-impedance when $\overline{CE}$ is inactive (high).
V_{CC}	18	I	Supply voltage (+5V nominal).

Device Interface

The relationship of the ACC to other components in the system is shown in Figures 4 and 5. The ACC is connected to the asychronous channel through level shifters which translate the TTL inputs and outputs to the appropriate levels (e.g., RS-232C, TTY current loop, etc.). The microprocessor transfers data to and from the ACC via the Communication Register Unit (CRU).

CPU Interface

The ACC interfaces to the CPU through the Communication Register Unit (CRU). The CRU interface consists of five address-select lines (S0-S4), chip enable ($\overline{CE}$), and three CRU control lines (CRUIN, CRUOUT, and CRUCLK). When $\overline{CE}$ becomes active (low), the five select lines address the CRU bit being accessed. When data is being transferred to the ACC from the CPU, CRUOUT contains the valid datum which is strobed by CRUCLK. When ACC data is being read, CRUIN is the datum output by the ACC.

AMERICAN MICROSYSTEMS, INC.

PRELIMINARY DATA SHEET

S9940

MICROCOMPUTER

Features

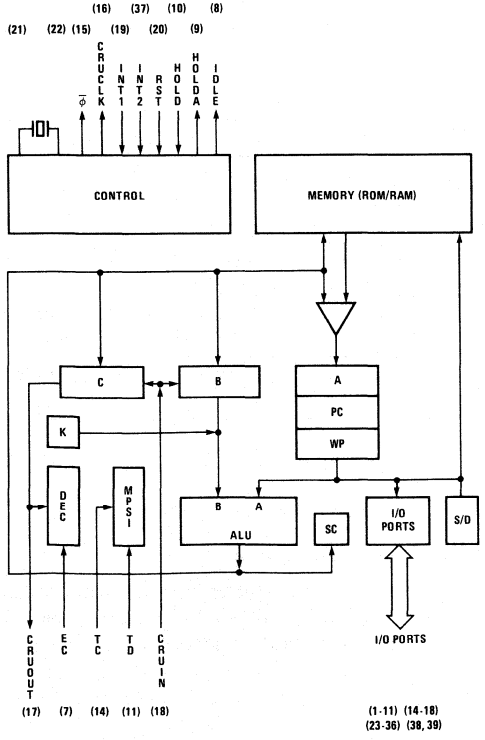
- ☐ **16-Bit Instruction Word**
- ☐ **Minicomputer Instruction Set Including Multiply and Divide**
- ☐ **2048 Bytes of ROM on Chip**
- ☐ **128 Bytes of RAM on Chip**
- ☐ **16 General Purpose Registers**
- ☐ **4 Prioritized Interrupts**
- ☐ **On Chip Timer/Event Counter**
- ☐ **32 Bits General Purpose I/O**
- ☐ **256 Bits I/O Expansion**
- ☐ **Multiprocessor System Interface**
- ☐ **Single 5 Volt Power Supply**
- ☐ **Power Down Capability for Low Stand-by Power**
- ☐ **N-Channel Silicon Gate MOS**

General Description

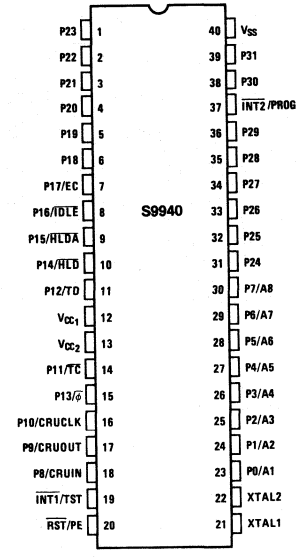
The S9940 is a single-chip, 16-bit microcomputer containing a CPU, memory (RAM and ROM), and extensive I/O. The instruction set of the S9940 is a subset of the S9900 instruction set and includes capabilities offered by minicomputers. The unique memory-to-memory architecture features multiple register files, resident in the RAM, which allow faster response to interrupts, and increased programming flexibility. The memory consists of 128 bytes of RAM and 2048 bytes of ROM. The S9940 implements four levels of interrupts, including an internal decrementer which can be programmed as a timer or an event counter. All members of the S9900 family of peripheral circuits are compatible with the S9940.

S9900

Block Diagram



Pin Configuration



S9940 Electrical Specifications

Absolute Maximum Ratings Over Operating Free-Air Temperature Range (unless otherwise noted)*

Supply Voltage, V_{CC}	−0.3V to +10V
All Input Voltages (1)	−0.3V to +10V
Output Voltage (1)	−2V to +7V
Continuous Power Dissipation	1.5W
Operating Free-Air Temperature Range	0°C to 70°C
Storage Temperature Range	−55°C to +150°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

(1) All voltage values are with respect to V_{SS}

Recommended Operating Conditions

Symbol	Parameter	Min.	Nom.	Max.	Unit	Condition
V_{CC}	Supply Voltage	4.75		5.25	V	
V_{SS}	Supply Voltage		0		V	
V_{IH}	High-Level Input Voltage	2.0			V	
V_{IL}	Low-Level Input Voltage			0.8	V	
T_A	Operating Free-Air Temperature	0		+70	°C	

Electrical Characteristics

Symbol	Parameter	Min.	Nom.	Max.	Unit	Condition
I_I	Input Current, All Inputs		±100		μA	$V_I = V_{SS}$ to V_{CC}
V_{OH}	High-Level Output Voltage, All Inputs		2.4		V	$I_O = -0.4$mA
V_{OL}	Low-Level Output Voltage, All Outputs		0.4		V	$I_O = 2$mA
I_{CC}	Supply Current from I_{CC}		150		mA	
C_1	Input Capacitance, All Inputs		15		pF	f=1MHz unmeasured pins at V_{SS}
C_0	Output Capacitance, All Outputs		15		pF	f=1MHz unmeasured pins at V_{SS}

Clock Characteristics

The S9940 has an internal oscillator and 2-phase clock generator controlled by an external crystal. The user may also disable the oscillator and directly inject a frequency source into the XTAL2 input. The crystal frequency and the external frequency source must be 2 times the desired system frequency.

Internal Clock Option

The internal oscillator is enabled by connecting a crystal across XTAL1 and XTAL2. The system frequency is one-half the crystal frequency.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
	Crystal Frequency		4.0		MHz	0°C≤T≤+70°C

External Clock Options

An external frequency source can be used by injecting the frequency directly into XTAL2 with XTAL1 left unconnected. The external frequency must conform to the following specifications:

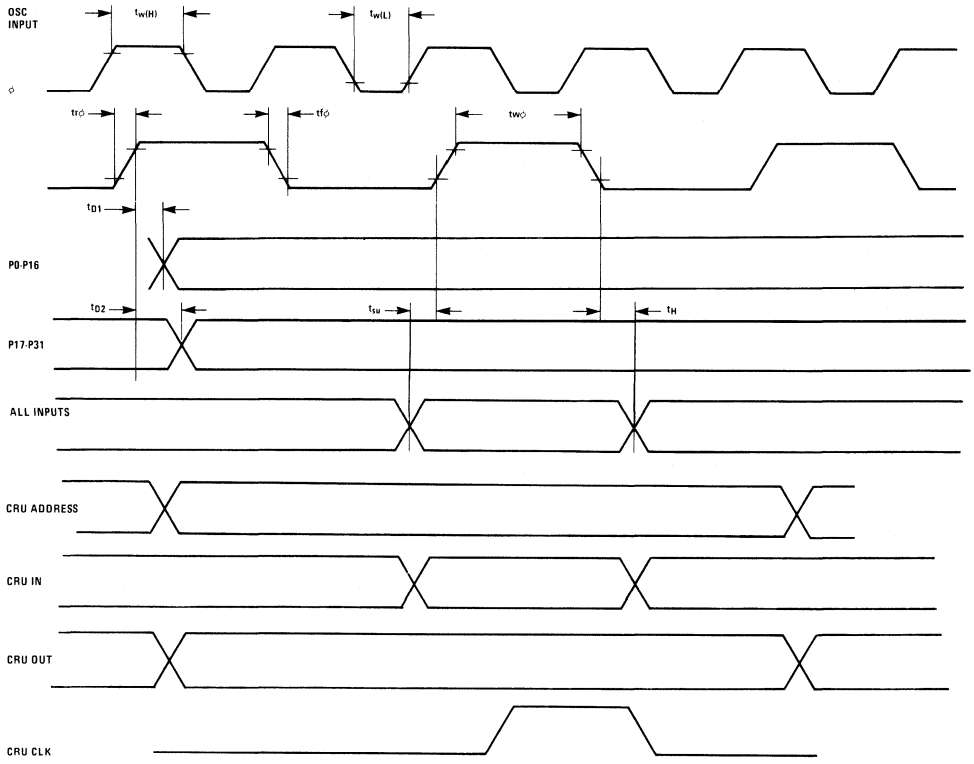
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
f_{ext}	External Source Frequency		4		MHz	
C_{OUT}	Output Capacitance of External Source		15		pF	
V_H	External Source High-Level		4.5		V	
V_L	External Source Low-Level		0.4		V	
$t_{w(H)}$	External Source High-Level Pulse Width		115		ns	
$t_{w(L)}$	External Source Low-Level Pulse Width		115		ns	

Switching Characteristics Over Full Range of Recommended Operating Conditions

All external signal timings are with reference to ϕ (see Figure 1).

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
$t_{R\phi}$	Rise Time of ϕ		30		ns	
$t_{f\phi}$	Fall Time of ϕ		30		ns	
$t_{w\phi}$	Pulse Width of ϕ		350		ns	
t_{D1}	Output Delay Time		100		ns	C_L=100pF
t_{D2}	Output Delay Time		400		ns	
t_{su}	Input Setup Time		10		ns	
t_H	Input Hold Time		0		ns	

Figure 1. External Signal Timing Diagram



System Configuration

The S9940 allows the user to configure part of the I/O pins as special functions for system application. The configurable pins are shown below.

That is, CB0 controls the I/O Expansion Channel, CB1 controls the MPSI, CB2 allows a clock output, and CB3 configures $\overline{\text{HLD}}$, $\overline{\text{HLDA}}$, and $\overline{\text{IDLE}}$ for powerdown. Application of RESET forces the configuration bits to zero, the all I/O line condition. The configuration can then be changed by outputting the desired bit value to the designated CRU address.

Pin Name	Configuration Bit	Configuration	
		0	1
P0/A1	0	P0	A1
P1/A2	0	P1	A2
P2/A3	0	P2	A3
P3/A4	0	P3	A4
P4/A5	0	P4	A5
P5/A6	0	P5	A6
P6/A7	0	P6	A7
P7/A8	0	P7	A8
P8/CRUIN	0	P8	CRUIN
P8/CRUOUT	0	P9	CRUOUT
P10/$\overline{\text{CR}}$UCLK	0	P10	$\overline{\text{CR}}$UCLK
P11/$\overline{\text{TC}}$	1	P11	$\overline{\text{TC}}$
P12/TD	1	P12	TD
P13/ϕ	2	P13	ϕ
P14/HLD	3	P14	HLD
P15/HLDA	3	P15	HLDA
P16/IDLE	3	P16	IDLE

S9940 Pin Description

Table 1 defines the S9940 pin assignments and describes the function of each pin.

Table 1. S9940 Pin Assignments and Functions

SIGNATURE	PIN	I/O	DESCRIPTION
XTAL1	21	IN	Crystal input pin for control of internal oscillator.
XTAL2	22	IN	Crystal input pin for control of internal oscillator. Also input pin for external oscillator.
NC	12		
V_{CC}	13		Supply voltage (+5V).
V_{SS}	40		Ground reference.
$\overline{RST}$	20	IN	$\overline{RESET}$. When active low (Schmitt Trigger input, 0-0.45V) the RESET sequence is initiated. $\overline{RESET}$ must be held active for a minimum of four clock cycles.
INT1	19	IN	Interrupt 1. When active low (0-0.45V) external device interrupt 1 is active.
INT2	37	IN	Interrupt 2. When active low (0-0.45V) and RST/PE is not active high, external device interrupt 2 is active.
P0/A1	23	I/O	General Purpose I/O lines. P0-P7 can also be configured as the address bus (A1 is MSB) of the
P1/A2	24		I/O expansion channel.
P2/A3	25		
P3/A4	26		
P4/A5	27		
P5/A6	28		
P6/A7	29		
P7/A8	30		
P8/CRUIN	18	I/O	General Purpose I/O Line. P8 can also be configured as the CRUIN data input signal for the I/O expansion channel.
P9/CRUOUT	17	I/O	General Purpose I/O Line. P9 can also be configured as the CRUOUT data output signal for the I/O expansion channel.
P10/CRUCLK	16	I/O	General Purpose I/O Line. P10 can also be configured as the CRUCLK data strobe output signal for the I/O expansion channel.
P11/$\overline{TC}$	14	I/O	General Purpose I/O Line. P11 can also be configured as the transfer clock for the Multiprocessor System Interface.
P12/TD	11	I/O	General Purpose I/O Line. P12 can also be configured as the transfer data signal for the Multiprocessor System Interface.
P13/$\overline{\phi}$	15	I/O	General Purpose I/O Line. P13 can also be configured as a clock output signal.
P14/$\overline{HLD}$	10	I/O	General Purpose I/O Line. P14 can also be configured as the $\overline{HOLD}$ (active low) Schmitt Trigger input to force the processor to stop until $\overline{HOLD}$ returns to the inactive state.
P15/$\overline{HLDA}$	9	I/O	General Purpose I/O Line. P15 can also be configured as the Hold Acknowledge output (active low). When the processor enters the HOLD state, $\overline{HOLDA}$ becomes active.
P16/$\overline{IDLE}$	8	I/O	General Purpose I/O Line. P16 can also be configured as the IDLE outputsignal (active low) for power down.
P17/EC	7	I/O	General Purpose I/O Line. P17 can also be programmed as the event counter input. The decrementer will decrement on each positive transition of EC.
P18	6	I/O	General Purpose I/O Line.

Table 1. S9940 Pin Assignments and Functions (Continued)

SIGNATURE	PIN	I/O	DESCRIPTION
P19	5	I/O	General Purpose I/O Line.
P20	4	I/O	General Purpose I/O Line.
P21	3	I/O	General Purpose I/O Line.
P22	2	I/O	General Purpose I/O Line.
P23	1	I/O	General Purpose I/O Line.
P24	31	I/O	General Purpose I/O Line.
P25	32	I/O	General Purpose I/O Line.
P26	33	I/O	General Purpose I/O Line.
P27	34	I/O	General Purpose I/O Line.
P28	35	I/O	General Purpose I/O Line.
P29	36	I/O	General Purpose I/O Line.
P30	38	I/O	General Purpose I/O Line.
P31	39	I/O	General Purpose I/O Line.

S9940 Instruction Set

Definition

Each instruction of the S9940 set performs one of the following operations:

- ☐ Arithmetic, logical, comparison, or manipulation operations on data;
- ☐ Loading or storage of machine registers (program counter, workspace pointer, or status);
- ☐ Data transfer between memory and external devices via the CRU;
- ☐ Control functions.

The instruction set is identical to that of the S9900 with the following exceptions:

- ☐ Instructions deleted

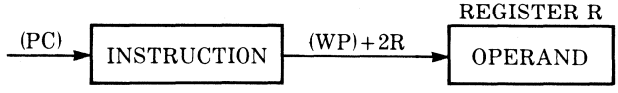
RSET	CKOF
−CKON	−LREX

Addressing Modes

S9940 instructions contain a variety of available modes for addressing random memory data (e.g., program parameters and flags), or formatted memory data (character strings, data lists, etc.). The following figures graphically describe the derivation of the effective address for each addressing mode. The applicability of addressing modes to particular instructions is described later along with the description of the operations performed by the instruction. The symbols following the names of the addressing modes (R, *R, *R+, @LABEL, or @TABLE (R)) are the general forms used by S9940 assemblers to select the addressing mode for register R. Note that the S9940 users use the same assembler and other software support packages as the ones used by the S9900 users.

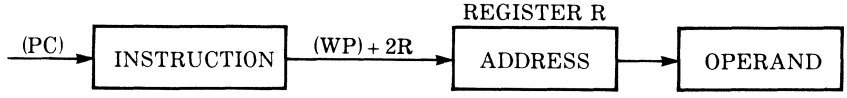
Workspace Register Addressing R

Workspace Register R contains the operand.



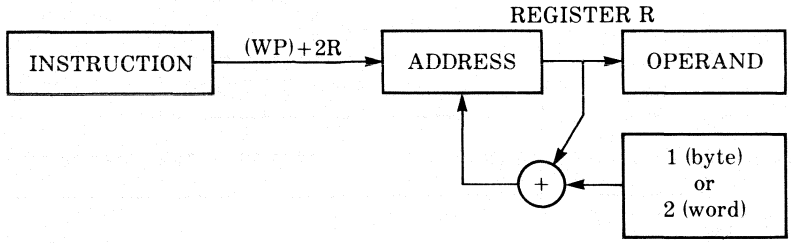
Workspace Register Indirect Addressing *R

Workspace Register R contains the address of the operand.



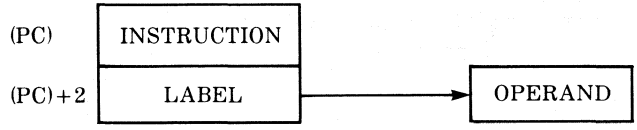
Workspace Register Indirect Auto Increment Addressing ***R+**

Workspace Register R contains the address of the operand. After acquiring the operand, the contents of workspace register R are incremented.



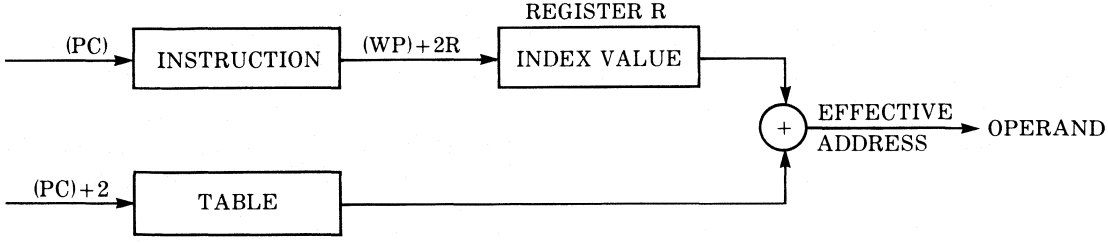
Symbolic (Direct) Addressing **@LABEL**

The word following the instruction contains the address of the operand.



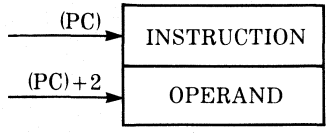
Indexed Addressing **@TABLE (R)**

The word following the instruction contains the base address. Workspace register R contains the index value. The sum of the base address and the index value results in the effective address of the operand.



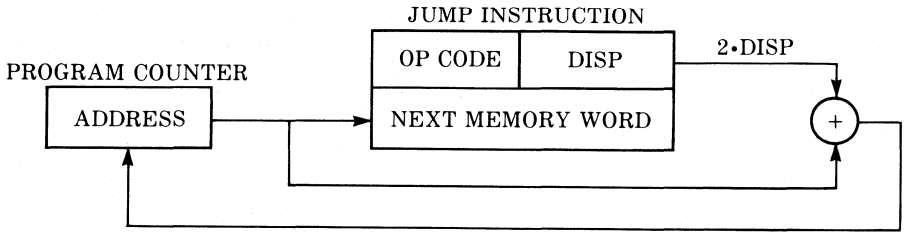
Immediate Addressing

The word following the instruction contains the operand.



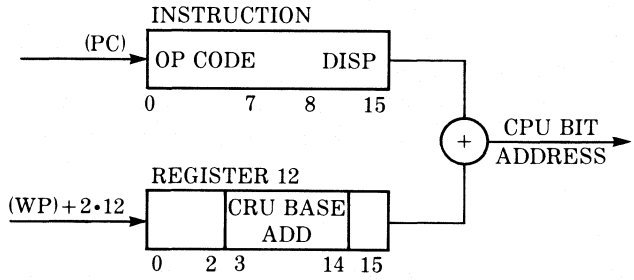
Program Counter Relative Addressing

The 8-bit signed displacement in the right byte (bits 8 through 15) of the instruction is multiplied by 2 and added to the updated contents of the program counter. The result is placed in the PC.



CRU Relative Addressing

The 8-bit signed displacement in the right byte of the instruction is added to the CRU base address (bits 3 through 14 of the workspace register 12). The result is the CRU address of the selection CRU bit.



16-BIT MICROPROCESSOR

Features

- ☐ 16-Bit Instruction Word
- ☐ Full Minicomputer Instruction Set Capability Including Multiply and Divide
- ☐ Up to 16,384 Bytes of Memory
- ☐ 8-Bit Memory Data Bus
- ☐ Advanced Memory-to-Memory Architecture
- ☐ Separate Memory, I/O, and Interrupt-Bus Structures
- ☐ 16 General Registers
- ☐ 4 Prioritized Interrupts
- ☐ Programmed and DMA I/O Capability
- ☐ On-Chip 4-Phase Clock Generator
- ☐ 40-Pin Package
- ☐ N-Channel Silicon-Gate Technology

The S9980A and the S9981 although very similar, have several differences which are:

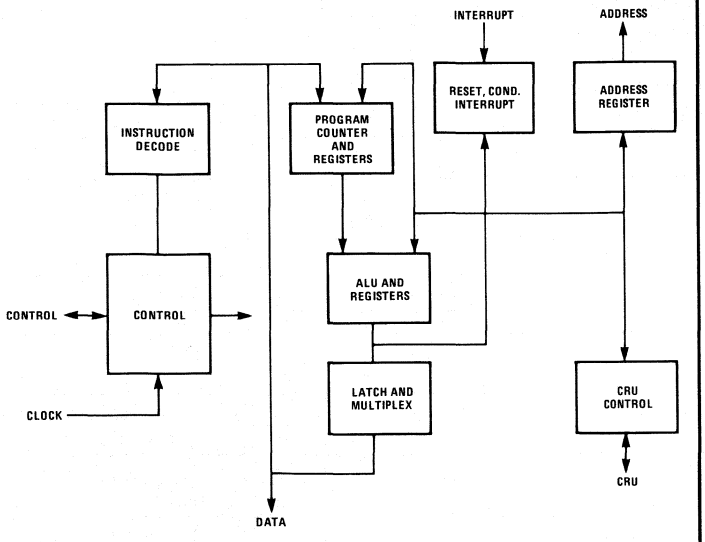
1. The S9980A requires a V_{BB} supply (pin 21) while the S9981 has an internal charge pump to generate V_{BB} from V_{CC} and V_{DD}.
2. The S9981 has an optional on-chip crystal oscillator in addition to the external clock mode of the S9980A.
3. The pin-outs are not compatible for D0-D7, INT0-INT2, and $\overline{\phi 3}$.

Description

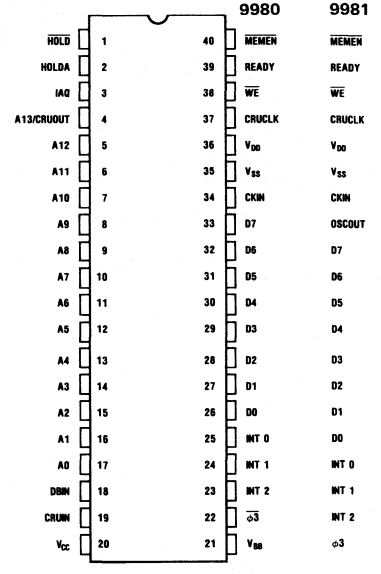
The S9980A/S9981 is a software-compatible member of AMI's 9900 family of microprocessors. Designed to minimize the system cost for smaller systems, the S9980A/S9981 is a single-chip 16-bit central processing unit (CPU) which has an 8-bit data bus, on-chip clock, and is packaged in a 40-pin package (see Figure 1). The instruction set of the S9980A/S9981 includes the capabilities offered by full minicomputers and is exactly the same as the 9900's. The unique memory-to-memory architecture features multiple register files, resident in memory, which allow faster response to interrupts and increased programming flexibility. The separate bus structure simplifies the system design effort.

S9900

Block Diagram



Pin Configuration



S9980A/S9981 Electrical and Mechanical Specifications

Absolute Maximum Ratings Over Operating Free-Air Temperature Range (unless otherwise noted)*

Supply voltage, V_{CC} (see Note 1) ..... – 0.3V to 15V
Supply voltage, V_{DD} (see Note 1) ..... – 0.3V to 15V
Supply voltage, V_{BB} (see Note 1) (9980A only) ..... – 5.25V to 0V
All input voltages (see Note 1) ..... – 0.3V to 15V
Output voltage (see Note 1) ..... – 2V to 7V
Continuous power dissipation 1.4W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 55°C to 150°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Under absolute maximum ratings voltage values are with respect to V_{SS}.

Recommended Operating Conditions

Symbol	Parameter	Min.	Nom.	Max.	Unit	Conditions
V_{BB}	Supply voltage (9980A only)	– 5.25	– 5	– 4.75	V	
V_{CC}	Supply voltage	4.75	5	5.25	V	
V_{DD}	Supply voltage	11.4	12	12.6	V	
V_{SS}	Supply voltage		0		V	
V_{IH}	High-level input voltage	2.2	2.4	$V_{CC}+1$	V	
V_{IL}	Low-level input voltage	– 1	0.4	0.8	V	
T_A	Operating free-air temperature	0	20	70	°C	

Electrical Characteristics Over full Range of Recommended Operating Conditions (unless otherwise noted)

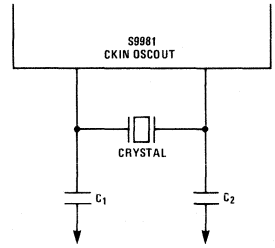
Symbol	Parameter		Min.	Typ.*	Max.	Unit	Conditions
I_I	Input current	Data bus during DBIN			± 75	μA	$V_I = V_{SS}$ to V_{CC}
		$\overline{WE}$, $\overline{MEMEN}$, $\overline{DBIN}$ during HOLDA			± 75	μA	$V_I = V_{SS}$ to V_{CC}
		Any other inputs			± 10	μA	$V_I = V_{SS}$ to V_{CC}
V_{OH}	High-level output voltage		2.4			V	$I_O = -0.4$mA
V_{OL}	Low-level output voltage				0.5 0.65	V	$I_O = 2$mA $I_O = 3.2$mA
I_{BB}	Supply current from V_{BB} (9980A only)				1	mA	
I_{CC}	Supply current from V_{CC}			50 40	60 50	mA	0°C 70°C
I_{DD}	Supply current from V_{DD}			70 65	80 75	mA	0°C 70°C
C_I	Input capacitance (any inputs except data bus)			15		pF	f = 1MHz, unmeasured pins at V_{SS}
C_{DB}	Data bus capacitance			25		pF	f = 1MHz, unmeasured pins at V_{SS}
C_O	Output capacitance (any output except data bus)			15		pF	f = 1MHz, unmeasured pins at V_{SS}

*All typical values are at T_A = 25°C and nominal voltages.

Clock Characteristics

The S9980A and S9981 have an internal 4-phase clock generator/driver. This is driven by an external TTL compatible signal to control the phase generation. In addition, the S9981 provides an output (OSCOUT) that in conjunction with CKIN forms an on-chip crystal oscillator. This oscillator requires an external crystal and two capacitors as shown in Figure 1. The external signal or crystal must be 4 times the desired system frequency.

Figure 1. Crystal Oscillator Circuit



Internal Crystal Oscillator (9981 Only)

The internal crystal oscillator is used as shown in Figure 1. The crystal should be a fundamental series resonant type. C_1 and C_2 represent the total capacitance on these pins including strays and parasitics.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
	Crystal frequency	6		10	MHz	0°C-70°C
	C_1,C_2	10	15	25	pF	0°C-70°C

External Clock

The external clock on the S9980A and optional on the S9981, uses the CKIN pin. In this mode the OSCOUT pin of the S9981 must be left floating. The external clock source must conform to the following specifications.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
f_{ext}	External source frequency*	6		10	MHz	
V_H	External source high level	2.2			V	
V_L	External source low level			0.8	V	
T_r/T_f	External source rise/fall time		10		ns	
T_{WH}	External source high level pulse width	40			ns	
T_{WL}	External source low level pulse width	40			ns	

*This allows a system speed of 1.5MHz to 2.5MHz

Switching Characteristics Over Full Range of Recommended Operating Conditions

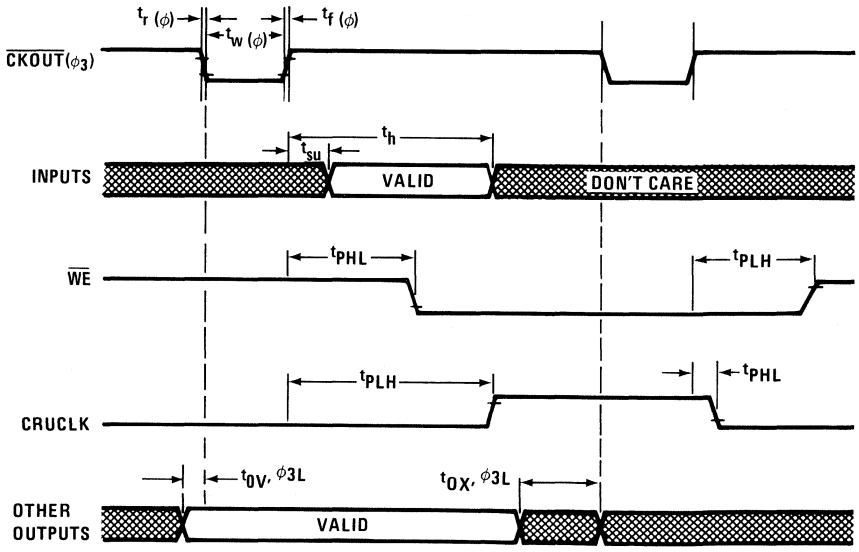
The timing of all the inputs and outputs is controlled by the internal 4 phase clock; thus all timings are based on the width of one phase of the internal clock. This is $1/f_{(CKIN)}$ (whether driven or from a crystal). This is also $\frac{1}{4} f_{system}$. In the following table this phase time is denoted t_w.

All external signals are with reference to $\phi 3$ (see Figure 2).

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
$t_r(\phi 3)$	Rise time of $\phi 3$	3	5	10	ns	
$t_f(\phi 3)$	Fall time of $\phi 3$	5	7.5	15	ns	
$t_w(\phi 3)$	Pulse width of $\phi 3$	$t_w - 15$	$t_w - 10$	$t_w + 10$	ns	
t_{su}	Data or control setup time*	$t_w - 30$			ns	
t_h	Data hold time*	$2t_w + 10$			ns	
t_{PHL} ($\overline{WE}$)	Propagation delay time WE high to low	$t_w - 10$	t_w	$t_w + 20$	ns	tw = 1/f(CKIN) = ¼ f_{system}
t_{PLH} ($\overline{WE}$)	Propagation delay time WE low to high	t_w	$t_w + 10$	$t_w + 30$	ns	
t_{PHL} (CRUCLK)	Propagation delay time, CRUCLK high to low	− 20	− 10	+ 10	ns	C_L = 200pf
t_{PLH} (CRUCLK)	Propagation delay time, CRUCLK low to high	$2t_w - 10$	$2t_w$	$2t_w + 20$	ns	
t_{OV}	Delay time from output valid to $\phi 3$ low	$t_w - 50$	$t_w - 30$		ns	
t_{OX}	Delay time from output invalid to $\phi 3$ low		$t_w - 20$	t_w	ns	

*All inputs except IC0-IC2 must be synchronized to meet these requirements. IC0-IC2 may change asynchronously.

Figure 2. External Signal Timing Diagram



S9980A Pin Description

Table 1 defines the S9980A pin assignments and describes the function of each pin.

Table 1. S9980A Pin Assignments and Functions

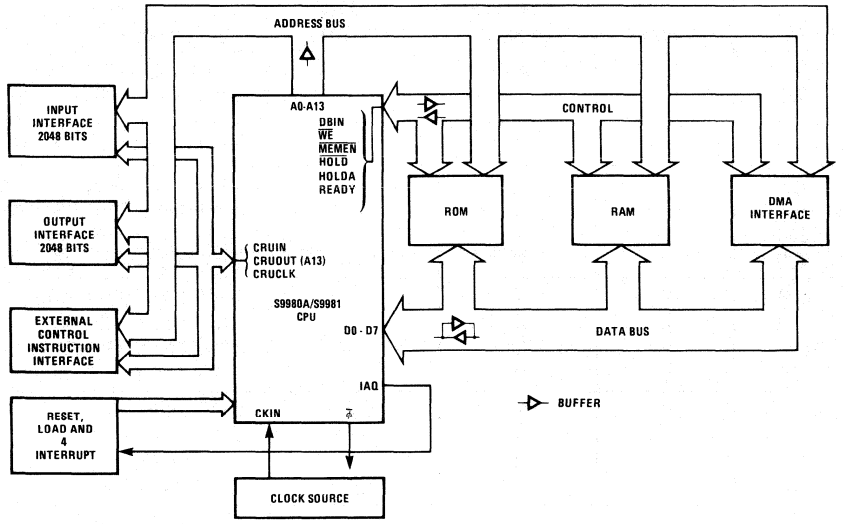
Signature	Pin	I/O	Description
A0 (MSB)	17	OUT	**ADDRESS BUS**
A1	16	OUT	A0 through A13 comprise the address bus. This 3-state bus provides the memory-address vector to the external-memory system when MEMEN is active and I/O-bit addresses and external-instruction addresses to the I/O system when $\overline{\text{MEMEN}}$ is inactive. The address bus assumes the high-impedance state when HOLDA is active.
A2	15	OUT	
A3	14	OUT	
A4	13	OUT	
A5	12	OUT	
A6	11	OUT	
A7	10	OUT	
A8	9	OUT	
A9	8	OUT	
A10	7	OUT	
A11	6	OUT	
A12	5	OUT	
A13/CRUOUT	4	OUT	**CRUOUT**
			Serial I/O data appears on A13 when an LDCR, SBZ and SBO instruction is executed. This data should be sampled by the I/O interface logic when CRUCLK goes active (high). One bit of the external instruction code appears on A13 during external instruction execution.
D0 (MSB)	26	I/O	**DATA BUS**
D1	27	I/O	D0 through D7 comprise the bidirectional 3-state data bus. This bus transfers memory data to (when writing) and from (when reading) the external-memory system when $\overline{\text{MEMEN}}$ is active. The data bus assumes the high-impedance state when HOLDA is active.
D2	28	I/O	
D3	29	I/O	
D4	30	I/O	
D5	31	I/O	
D6	32	I/O	
D7 (LSB)	33	I/O	
			POWER SUPPLIES
V_{BB}	21		Supply voltage (−5V NOM)
V_{CC}	20		Supply voltage (5V NOM)
V_{DD}	36		Supply voltage (12V NOM)
V_{SS}	35		Ground reference
CKIN	34	IN	**CLOCKS**
			Clock In. A TTL compatible input used to generate the internal 4-phase clock. CKIN frequency is 4 times the desired system frequency.
$\overline{\phi 3}$	22	OUT	Clock phase 3 ($\phi 3$) inverted; used as a timing reference.
DBIN	18	OUT	**BUS CONTROL**
			Data bus in. When active (high), DBIN indicates that the S9980A has disabled its output buffers to allow the memory to place memory-read data on the data bus during MEMEN. DBIN remains low in all other cases except when HOLDA is active at which time it is in the high-impedance state.

Table 1. S9980A Pin Assignments and Functions (Continued)

Signature	Pin	I/O	Description
$\overline{\text{MEMEN}}$	40	OUT	Memory enable. When active (low), $\overline{\text{MEMEN}}$ indicates that the address bus contains a memory address. When HOLDA is active, $\overline{\text{MEMEN}}$ is in the high impedance state.
$\overline{\text{WE}}$	38	OUT	Write enable. When active (low), $\overline{\text{WE}}$ indicates that memory-write data is available from the S9980 to be written into memory. When HOLDA is active, $\overline{\text{WE}}$ is in the high-impedance state.
CRUCLK	37	OUT	CRU clock. When active (high), CRUCLK indicates that external interface logic should sample the output data on CRUOUT or should decode external instructions on A0, A1, A13.
CRUIN	19	IN	CRU data in. CRUIN, normally driven by 3-state or open-collector devices, receives input data from external interface logic. When the processor executes a STCR or TB instruction, it samples CRUIN for the level of the CRU input bit specified by the address bus (A2 through A12).
INT2 INT1 INT0	23 24 25	IN IN IN	Interrupt code. Refer to interrupt discussion for detailed description.
			MEMORY CONTROL
$\overline{\text{HOLD}}$	1	IN	Hold. When active (low), $\overline{\text{HOLD}}$ indicates to the processor that an external controller (e.g., DMA device) desires to utilize the address and data buses to transfer data to or from memory. The S9980A enters the hold state following a hold signal when it has completed its present memory cycle.* The processor then places the address and data buses in the high-impedance state (along with $\overline{\text{WE}}$, $\overline{\text{MEMEN}}$, and DBIN) and responds with a hold-acknowledge signal (HOLDA). When $\overline{\text{HOLD}}$ is removed, the processor returns to normal operation.
HOLDA	2	OUT	Hold acknowledge. When active (high), HOLDA indicates that the processor is in the hold state and the address and data buses and memory control outputs ($\overline{\text{WE}}$, $\overline{\text{MEMEN}}$, and DBIN) are in the high-impedance state.
READY	39	IN	Ready. When active (high), READY indicates that memory will be ready to read or write during the next clock cycle. When not-ready is indicated during a memory operation, the S9980A enters a wait state and suspends internal operation until the memory systems indicated ready.
			TIMING AND CONTROL
IAQ	3	OUT	Instruction acquisition. IAQ is active (high) during any memory cycle when the S9980A is acquiring an instruction. IAQ can be used to detect illegal op codes. It may also be used to synchronize LOAD stimulus.

*If the cycle following the present memory cycle is also a memory cycle it, too, is completed before S9980 enters hold state.

Figure 16. Maximum S9980 System



Instructions Summary

MNEMONIC	OP CODE	FORMAT	RESULT COMPARED TO ZERO	STATUS AFFECTED	INSTRUCTIONS
A	A000	1	Y	0-4	ADD(WORD)
AB	B000	1	Y	0-5	ADD(BYTE)
ABS	0740	6	Y	0-4	ABSOLUTE VALUE
AI	0220	8	Y	0-4	ADD IMMEDIATE
ANDI	0240	8	Y	0-2	AND IMMEDIATE
B	0440	6	N	—	BRANCH
BL	0680	6	N	—	BRANCH AND LINK (W11)
BLWP	0400	6	N	—	BRANCH LOAD WORKSPACE POINTER
C	8000	1	N	0-2	COMPARE (WORD)
CB	9000	1	N	0-2,5	COMPARE (BYTE)
CI	0280	8	N	0-2	COMPARE IMMEDIATE
CKOF	03C0	7	N	—	EXTERNAL CONTROL
CKON	03A0	7	N	—	EXTERNAL CONTROL
CLR	04C0	6	N	—	CLEAR OPERAND
COC	2000	3	N	2	COMPARE ONES CORRESPONDING
CZC	2400	3	N	2	COMPARE ZEROES CORRESPONDING
DEC	0600	6	Y	0-4	DECREMENT (BY ONE)
DECT	0640	6	Y	0-4	DECREMENT (BY TWO)
DIV	3C00	9	N	4	DIVIDE
IDLE	0340	7	N	—	COMPUTER IDLE
INC	0580	6	Y	0-4	INCREMENT (BY ONE)
INCT	05C0	6	Y	0-4	INCREMENT (BY TWO)
INV	0540	6	Y	0-2	INVERT (ONES COMPLEMENT)
JEQ	1300	2	N	—	JUMP EQUAL (ST2-1)

Instructions Summary (Continued)

MNEMONIC	OP CODE	FORMAT	RESULT COMPARED TO ZERO	STATUS AFFECTED	INSTRUCTIONS
JGT	1500	2	N	—	JUMP GREATER THAN (ST1 = 1)
JH	1800	2	N	—	JUMP HIGH (ST0 = 1 AND ST2 = 0)
JHE	1400	2	N	—	JUMP HIGH OR EQUAL (ST0 OR ST2 = 1)
JL	1000	2	N	—	JUMP LOW (ST0 AND ST2 = 0)
JLE	1200	2	N	—	JUMP LOW OR EQUAL (ST0 = 0 OR ST2 = 1)
JLT	1100	2	N	—	JUMP LESS THAN (ST1 AND ST2 = 0)
JMP	1000	2	N	—	JUMP UNCONDITIONAL
JNC	1700	2	N	—	JUMP NO CARRY (ST3 = 0)
JNE	1600	2	N	—	JUMP NOT EQUAL (ST2 = 0)
JND	1900	2	N	—	JUMP NO OVERFLOW (ST4 = 0)
JOC	1800	2	N	—	JUMP ON CARRY (ST3 = 1)
JOP	1C00	2	N	—	JUMP ODD PARITY (ST5 = 1)
LDCR	3000	4	Y	0-2,5	LOAD CRU
LI	0200	8	N	0-2	LOAD IMMEDIATE
LIMI	0300	8	N	12-15	LOAD IMMEDIATE TO INTERRUPT MASK
LREX	03E0	7	N	12-15	EXTERNAL CONTROL
LWPI	02E0	8	N	—	LOAD IMMEDIATE TO WORKSPCE POINTER
MOV	C000	1	Y	0-2	MOVE (WORD)
MOVB	D000	1	Y	0-2,5	MOVE (BYTE)
MPY	3800	9	N	—	MULTIPLY
NEG	0500	6	Y	0-4	NEGATE (TWO'S COMPLEMENT)
ORI	0260	8	Y	0-2	OR IMMEDIATE
RSET	0360	7	N	12-15	EXTERNAL CONTROL
RTWP	0380	7	N	0-6, 12-15	RETURN WORKSPACE POINTER
S	6000	1	Y	0-4	SUBTRACT (WORD)
SB	7000	1	Y	0-5	SUBTRACT (BYTE)
SBO	1D00	2	N	—	SET CRU BIT TO ONE
SBZ	1E00	2	N	—	SET CRU BIT TO ZERO
SETO	0700	6	N	—	SET ONES
SLA	0A00	5	Y	0-4	SHIFT LEFT (ZERO FULL)
SOC	E000	1	Y	0-2	SET ONES CORRESPONDING (WORD)
SOCB	F000	1	Y	0-2,5	SET ONES CORRESPONDING (BYTE)
SRA	0800	5	Y	0-3	SHIFT RIGHT (MSB EXTENDED)
SRC	0800	5	Y	0-3	SHIFT RIGHT CIRCULAR
SRL	0900	5	Y	0-3	SHIFT RIGHT (LEADING ZERO FILL)
STCR	3400	4	Y	0-2,5	STORE FROM CRU
STST	02C0	8	N	—	STORE STATUS REGISTER
STWP	02A0	8	N	—	STORE WORKSPACE POINTER
SWPB	06C0	6	N	—	SWAP BYTES
SZC	4000	1	Y	0-2	SET ZEROES CORRESPONDING (WORD)
SZCB	5000	1	Y	0-2,5	SET ZEROES CORRESPONDING (BYTE)
TB	1F00	2	N	2	TEST CRU BIT
X	0480	6	N	—	EXECUTE
XOP	2C00	9	N	6	EXTENDED OPERATION
XOR	2800	3	Y	0-2	EXCLUSIVE OR

ILLEGAL OP CODES 0000-01FF;0320-033F;0780-07FF;0C00-0FFF

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- ☐ **Provides Common Software Base for All Support Packages**
- ☐ **Enhances Software Portability**
- ☐ **Software Warranty Included**
- ☐ **Software Maintenance Available**

ADS Software is part of the Advanced Development Support concept which permits users to learn one common software base for use throughout the various packages. The software system will operate with the AMIX™ disk operating system which is available for use with many popular development systems including the Intel MDS*, Motorola Exorciser*, Tektronix 8002*, TI 990/4* and the Phoenix Family from AMI.

The AMIX Disk Operating System replaces the host operating system with a powerful floppy disk based system, screen oriented editor and utility programs. The AMIX System is optimized for the host machine for maximum programming efficiency and is designed specifically for a single work station environment. The diagram on the back of this data sheet illustrates AMIX's levels of operation and some of the commands that are available.

Cross Assemblers are available for the following microprocessors:

6800, 6801, 6802, 6803, 6805, 6808 and 6809

8080, 8085 and Z80

802X, 803X and 804X

9900, 9940, 9980, 9981 and 9995

S2000, S2150, S22XX and S42XX

6502 and 2650

(Additional assemblers are being added continuously.)

The AMI Cross Support relies on a common software base. This commonality extends to the pseudo-operations of the assemblers. Included in each assembler are:

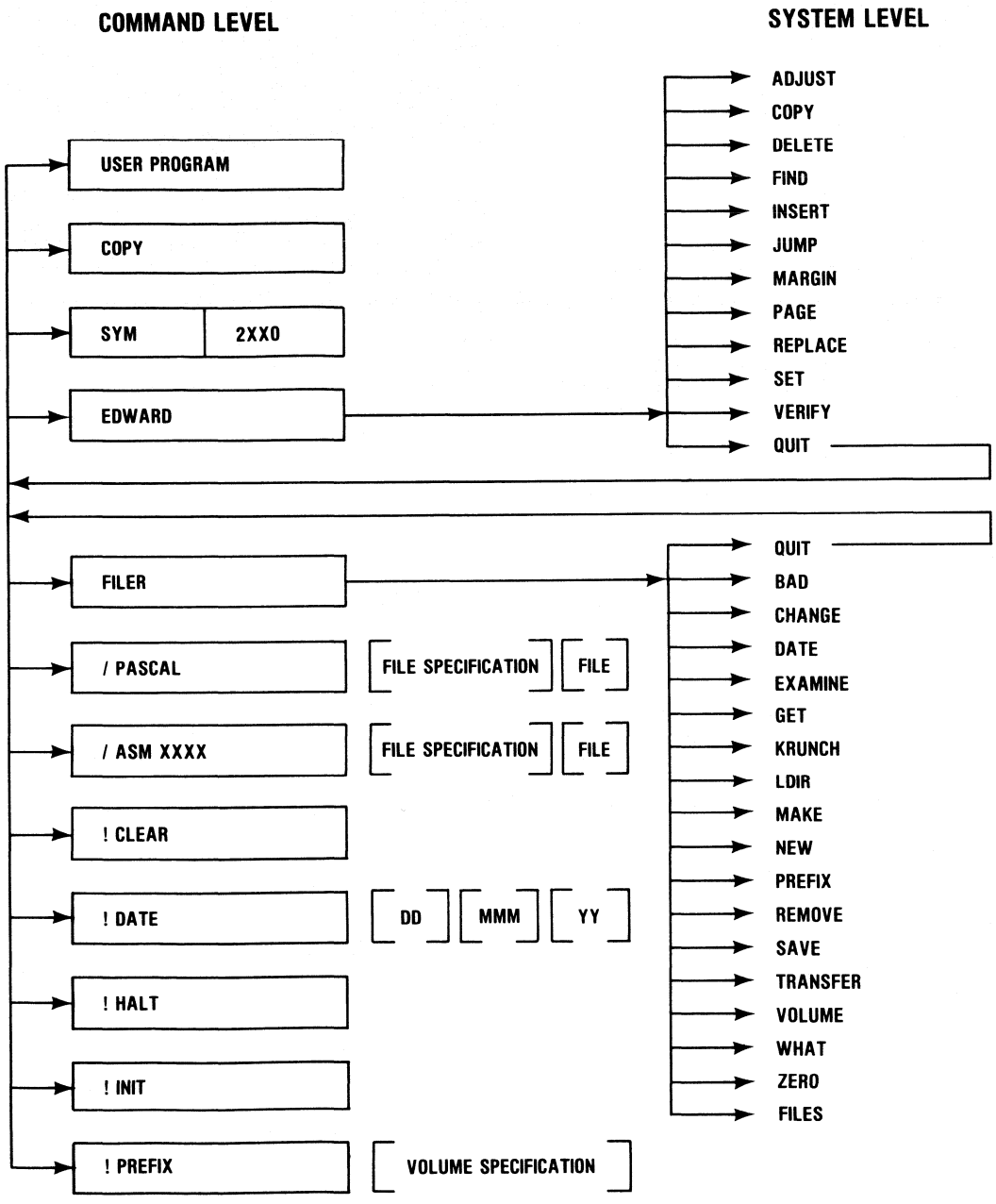
INCLUDE	directs assembler to get source from a file
EQU	allows values to be equated to a symbol
DEF	defines a label for global usage
REF	defines a label to be outside current code or data segment
PAGE	perform page eject
TITLE	print a title heading

The assemblers are each a full macro assembler supporting local and global labels. Arithmetic and logic operations include plus, minus, ones complement, exclusive-OR, multiplication, truncating division, remainder division, or, and, equal, and not equal. Many of the assemblers' features are normally found only in larger systems.

Software simulators are available for all S2000/2200 single chip microcomputers as a development tool. Basic capabilities supported are similar to those available with in circuit emulation but without the hardware interaction. Software facilities include: breakpoint, dump memos, alter memory, single step, set-up I/O and observe I/O. When coupled with the appropriate emulation module a complete hardware-software integration emulation can be performed.

ADS Software is part of our Advanced Development Support package designed to increase your profitability through systems solutions. Other software packages available as part of AMI's Advanced Development Support include AMI Pascal™ and Fortran-77.

**Trademark of Intel, Motorola, Tektronix and Texas Instruments, respectively.*


COMMAND LEVEL
SYSTEM LEVEL
USER PROGRAM
COPY
SYM
2XX0
EDWARD
FILER
/ PASCAL
FILE SPECIFICATION
FILE
/ ASM XXXX
FILE SPECIFICATION
FILE
! CLEAR
! DATE
DD
MMM
YY
! HALT
! INIT
! PREFIX
VOLUME SPECIFICATION
ADJUST
COPY
DELETE
FIND
INSERT
JUMP
MARGIN
PAGE
REPLACE
SET
VERIFY
QUIT
QUIT
BAD
CHANGE
DATE
EXAMINE
GET
KRUNCH
LDIR
MAKE
NEW
PREFIX
REMOVE
SAVE
TRANSFER
VOLUME
WHAT
ZERO
FILES

AMERICAN MICROSYSTEMS, INC.

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CA2000 BOSTON SYSTEMS OFFICE CROSS ASSEMBLER FOR S2000 MICROPROCESSORS BY AMI (and all compatible devices)

This cross assembler, one of a family of cross assemblers produced by The Boston Systems Office, is a powerful programming tool used to develop microprocessor software. It allows the user to take full advantage of a larger computer, whether in a time-sharing or in-house mode, thereby significantly reducing the number of man-hours spent in program development. The advantages of a larger computer include:

-Faster processing speeds
-More powerful editors
-Higher speed peripherals

These cross assemblers are written in the assembly language of the host computer. They require only 8K words of memory to assemble practically any size program. The symbol table can be expanded to fit any program or can be shrunk to fit into a smaller machine if required. The assemblers require much less CPU time to execute, even at this reduced memory requirement, when compared to manufacturer supplied cross assemblers. Benchmarks against competitive products in a time-sharing environment have shown that savings of over 85% are common. Similar efficiencies are realized when using an in-house computer.

The instruction set of each cross assembler is the same as documented in the manuals supplied by the microprocessor manufacturer. Mnemonics exist for data manipulation, binary arithmetic, jumps to subroutines, etc. In addition, all of the BSO cross assemblers have full macro and conditional assembly capabilities. The assembler outputs to disk, which may then be punched on paper tape, loaded into a PROM burner or down line loaded into memory, depending on your facilities.

Cross assemblers are now available for the following microprocessors:

AMD 9080A
AMI S2000, S6800 & S9900
Fairchild 6800 & F8
Hitachi 6800
Intel 8080, 8080A, 8085, 4040, 4004, 8008 8048, 8748, 8035 8049 & 8039
Intersil 8048
MOS Technology 6500 series
Mostek F8 & Z80
Motorola M6800
Nat'l Semiconductor IMP-8, SC/MP, 8080 & PACE
NEC uPD8080AF & uPD8080A
RCA CDP 1800 series (COSMAC)
Rockwell R6500, PPS-8 & PPS-4
Signetics 8048 & 8035
Synertek 6500 series
Thomson-CSF 6800
Texas Instruments TMS1000, 8080, & TMS9900
Zilog Z80

Please feel free to contact The Boston Systems Office for further information on any microprocessor not mentioned above, as we are constantly adding to our product line. BSO will also produce custom assemblers and other application and system software on a contract basis.

400 TOTTEN POND ROAD
WALTHAM, MASSACHUSETTS 02154
(617) 890-0888

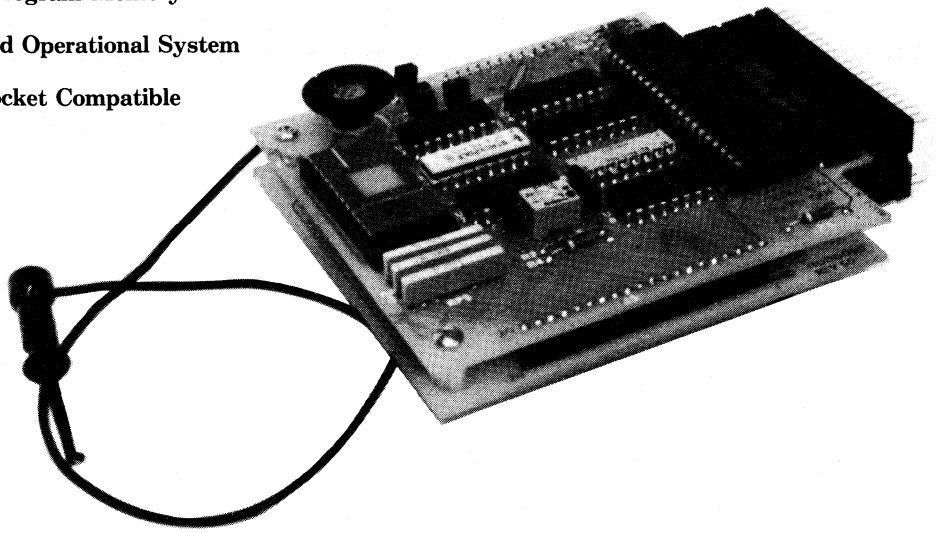
updated 03/23/78

AMERICAN MICROSYSTEMS, INC.

ADS
ADVANCED DEVELOPMENT SUPPORT

SES2000/S2150
S2150 Emulator Module

- ☐ **Full Microcomputer Emulation**
- ☐ **Erasable Program Memory**
- ☐ **Fully-tested Operational System**
- ☐ **System Socket Compatible**



The SES Series of boards provide pin for pin emulation of single-chip microcomputers. The board offers the full operational capabilities of the single-chip microcomputer coupled with the flexibility of board level design. The Series incorporates on-board Erasable PROM to provide ease of program modification in a prototype environment.

SES2000/S2150

The SES2000/S2150 is an emulator board for the popular S2000/S2150 single-chip microcomputer. This board level unit is configured to plug directly into the system socket that would normally hold the mask programmed S2000 /S2150. Through the use of the SES2000/S2150, system hardware and program configurations can be quickly and efficiently accomplished in the prototype stages. The board is also suited for integration into pre-production systems allowing full freedom of modification through memory changes in standard EPROM's.

Incorporated onto the SES2000/S2150 Emulator Module are latches and buffers which allow the S2000/S2150 microcomputer to access user programmed EPROM also located on the module. A separate source of power for the additional circuits eliminates the possibility of altering the users system characteristics. Thus to the system circuitry the SES module appears as a single-chip microcomputer operating from its internally programmed ROM.

General Description:

The S2000/S2150 Static Emulator provides a means of trying a user's program without committing the program to ROM within the S2000/S2150.

This is accomplished by using a S2000/S2150 that is placed into the multiplex mode and providing EPROM as the memory. The EPROM (2716 − 2K×8) can be programmed with a user's program

It is intended that the emulator can be plugged into a socket that would normally be used by the S2000/S2150 in its finished form (the S2000/S2150 ROM would contain a user defined program).

Specifications

Power Requirements		
External Clip (V_{CC})		+9V ± 5% @ 350mA (max)
V_{DD}[1]		+5 or +9V ± 5% @ 75mA (max)
V_{GG} (Max)		(−) 0.3/18V
V_{GG} (NOM)		+9V ± 5% @ 50mA (max)
Interface Signals[2] (V_{SS} = O_V, V_{GG} 9 ± 0.5V, V_{DD} = V_{CC} = 5 ± 5%, T_A = 25°C)		
Inputs		
K_1 — K_8	Low Level High Level	0.0 — (K_{REF} − 0.5V) (K_{REF} + 0.5) — V_{GG}V
K_{REF}		0.28 V_{GG} — 0.32 V_{GG}V
I_1 — I_8, ROMs, Run, POR	Low Level High Level	0.0 — 0.5V[3] 5.3 — V_{GG}V[3]
D_0 — D_7	Low Level High Level	0.0 — 0.8V 4.5 — V_{GG}V
Outputs		
A_0 — A_3	Low Level High Level	0.0 — 0.6V (I = 30mA) 3.5 — V_{DD}V (I = − 3mA)
A_4 — A_{12}, $\overline{EXT}$ SYNC + S	Low Level High Level	0.0 — 0.6V (I = 4.35mA) 3.5 — V_{DD}V (I = − 2mA)
D_0 — D_7	Low Level High Level	0.0 — 1.0V (I = 9mA) 3.5 — V_{DD}V (I = − 4mA)
Operating Temperature		0 — 70°C
Physical Dimensions	WxHxT	3.4 x 4.375 x 1.75 in.
Connector	40 Pin DIP socket	

Notes:

1. V_{DD} may be connected to V_{GG} if single power supply operation is desired.
2. Some minor variations exist in interface levels and currents between the SES 2000/S2150 and the S2000/S2150. Consult the S2000/S2150 data sheet for a full description and values.
3. A 100μA pull up to V_{GG} internal to the S2000/S2150 is connected to these inputs.

AMERICAN MICROSYSTEMS, INC.

ADS™
ADVANCED DEVELOPMENT SUPPORT

DELPHI™
REALTIME INTERACTIVE SYSTEM EMULATOR

- ☐ **Provides Realtime Interactive System Emulation for Many Popular Microprocessors**
- ☐ **Real Time Trace Mode Up to 35 Bits**
- ☐ **Two Programmable Breakpoints**
- ☐ **Simple Interconnect Via RS232 Port to Host Development System**
- ☐ **Easy Personality Module Interchange Provides Universal Support**

The Delphi Realtime Interactive System Emulator is designed to replace the target microprocessor in the system, and therefore gives the designer access to diagnostic and debugging facilities in the environment of the prototype system. Likewise, all of the resources of the target microprocessor are available for examination and modification by the user. The Delphi, via the emulation cable, has full control over the user system and the host development station terminal may be considered a window into your prototype providing the control to diagnose and debug the operation of the microprocessor-based system.

Using the development station terminal, you can read a memory location and can walk up and down memory, location by location. I/O locations can be examined and individual bits can be toggled under your control. This allows quick, simple hardware checks to be performed.

The BREAK command allows you to program breakpoints by address, and additionally use the STEP command for single step analysis. System memory can be replaced by the in-system memory of the Delphi in the event program ROMs or PROMs appear defective. This also allows quick changes to be made when errors are found.

For more complex problems, Delphi features a Realtime Trace Mode. This permits sensing of external events in the system such as interrupts, I/O response, etc. The Trace Mode can be programmed to trigger a set amount of time before or after the event thus allowing you greater flexibility in capturing system bugs. The time interval captured in the trace mode can be up to 128 cycles long.

This is extremely valuable in debugging problem areas. The bus history of address and data information is stored in the memory of the Delphi for your examination. The multiple event triggers can be placed in several locations to aid in catching difficult problems.

The Delphi interconnects to any host development system which uses an AMIX™ operating system. This includes the Intel MDS*, Motorola Exorciser*, Tektronix 8002A* and the TI 990/4* as well as AMI's own low cost, universal microprocessor development station, the Phoenix 1™.

The Delphi Realtime Interactive System Emulator is part of AMI's Advanced Development Support product line which includes the Phoenix 1 microprocessor development station, the Ariel™ Universal PROM Programmer/ROM Simulator and ADS™ software. All of the products in the ADS line are designed to increase your profitability through system solutions.

**Trademark of Intel, Motorola, Tektronix and Texas Instruments, respectively.*

AMERICAN MICROSYSTEMS, INC.

ADS™
ADVANCED DEVELOPMENT SUPPORT

ARIEL™ UNIVERSAL PROM PROGRAMMER AND ROM SIMULATOR

Features

- ☐ **Built in Universality for 256-Bit through 128K-Bit PROMS**
- ☐ **2K×8 RAM Buffer for ROM Simulation**
- ☐ **RS232 and TTY Serial I/O Interface**
- ☐ **Automatic Checksum Verification**
- ☐ **Executes Move and List Commands**
- ☐ **Sockets Fully Buffered**
- ☐ **Hex Keypad and Hex Display**
- ☐ **Eliminates the Need for Personality Modules**

The AMI Ariel Universal PROM Programmer/ROM Simulator provides complete, versatile PROM programming and ROM simulation capability in a small, light and portable product. Design innovations have eliminated the need for costly and cumbersome personality modules.

The Ariel provides an RS232 (and TTY) interface for easy interconnect to a host development system for ROM code down-loading. This direct interface simplifies program development and lowers product development costs.

When used in conjunction with AMI SES modules for the S2000 and S2200 families, the Ariel's ROM simulation capability eliminates the need to continually reprogram EPROMs as program changes are made. This simplifies the software development task.

The AMI Ariel Universal PROM Programmer/Simulator is part of our Advanced Support Tools concept designed to lower your development system costs and increase your efficiency through MOS system solutions.

Operating Modes

The letters in the following section appear in the display as that operation is being executed.

A	Load From Master
B	Blank Check
C	Program Operation
D	Verify
EE	Emulate
AA	Move Operation
BB	Dump/List to Serial Port
CC	Checksum
FF	Receive from Serial Port
—	Read/Alter Location
—	Select Device
—	Select Baud Rate

Device Select

When the unit is first powered on, the display shows a "D" in the window requesting the device type. By depressing a "D" and then a "1" through "A" on the keypad the following devices can be selected:

Device Selection

Triple Supply—D1-2704, D2-2708, D3-2716

Single Supply—D4-2508/2758, D5-2516/2716, D6-2532, D7-2732, D8-2564, D9-2764, DA-TI 128K

Keys

Reset—Initializes programmer to command mode.

Load—Moves data from master to RAM.

Verify—Ram/Master to copy EPROM.

Program—Blank checks/programs/verifies the RAM or Master to the copy EPROM.

Step—Allows manual manipulation of programmer.

Keypad—For data entry and software commands.

Emulate

1. Select device 2704, 2708, 2716 triple power supply. 2758, 2516, 2716 single supply.
2. Depress "E," "Step."
3. Connect master socket on programmer to in-circuit device socket using 24-pin cable.

Timing—Data will be valid within 450ns after all the address and CE are valid.

Inputs—One LS load

Outputs—Standard LS

Serial Interface

25-pin "D" connector set up for:

Serial RS232C—Set up as an EIA DCE using transmit data, receive data, clear to send, carrier detect, and data set ready; 300, 600, 1200 bps.

TTY—20 milliamp current loop signals supplying: send, receive, and reader control, 110 bps.

Mode—Asynchronous full-duplex, half duplex, 1 or 2 stop bits. Parity: none, odd, even.

Remote Control

All features can be controlled from remote terminal of computer.

Sockets

28-pin zero insertion force, mounted on mother sockets. Sockets are fully buffered from microprocessor. No power is applied to the devices in the sockets until an operation is started.

LED Display

8-digit display that shows address, master data and copy data simultaneously. Normally displays the device type in operation or current operation mode.

Checksum

The checksum is calculated and displayed after every verify operation over the memory space selected. This ensures a reliable data transfer. The checksum is an addition of the binary data and is displayed in a 2-byte sum. To calculate the checksum of RAM or copy.

1. Checksum of RAM—Depress "C" then "1".
2. Checksum of Master—Depress "C" then "2".
3. Checksum of Copy—Depress "C" then "3".

Step-by-Step Instructions

Select the device

A device must be selected before any operations can be performed.

Duplicate a master

1. Load master and copy sockets.
2. Depress "Program" key.

The Ariel will automatically blank check the copy PROM, pass a good device and continue into program. Once the manufacturer's programming time is complete, the unit automatically verifies the copy to master.

Verify on part against another

1. Load master and copy sockets.
2. Depress "Verify" key.

The Ariel automatically compares the master PROM to the device to be tested. If the data does not compare the unit will display the address that failed, master data, and copy data. After a fail a simple press of the "Step" key will continue verification.

Alter Data

1. Place master in master socket.
2. Depress "Load." Master data is transferred to internal RAM.
3. Enter "A" and address to be altered on keypad. Unit will display address and RAM data.
4. Enter new data on keypad. As it is entered it will be displayed.
5. Depress "Step." This enters the new data change and steps to next address.
6. Complete as many changes as needed.
7. RAM data can now be programmed into a copy PROM with a Move routine or used in the Emulation mode. (See Emulate.)
8. Depress "Load" to decrement address.

Editing

Move Routine: Block moves of data in RAM to copy device.

1. Depress "A" then depress "Program". This sets the programmer into the editing software.
2. Depress "B" to initiate the software to a block move and then a number "1" through "8." A "1" moves the 2K×8 of RAM into the lower 2K of data in the copy device. A "2" command moves the RAM data into the second 2K section of the copy PROM and "3" into the third section of the copy PROM, etc., until the complete copy device selected is programmed.

1=0000—07FF ...	16K	5=2000—27FF ..	80K
2=0800—0FFF ...	16K	6=2800—2FFF ..	80K

3=1000—17FF ... 48K 7=3000—37FF .. 112K
4=1800—1FFF ... 64K 8=3800—3FFF .. 128K

Generalized Moves:

1. Any number of bytes can be moved from copy, master, or RAM.
2. Depress "A" then "Program". This sets the programmer into the Move routine.
3. Enter beginning address of the block to be moved XXXX.
4. Enter ending address of the block to be moved, YYYY.
5. Enter the beginning address of the destination, ZZZZ.
6. After the last hex key is depressed, the instrument automatically transfers the defined block of data to the address designated.

If the block to be moved is in the master, add 2000 hex to the address and enter that number. If the block is in the copy, add 4000 hex to the address and enter that number.

Example: Move address 0000 through 03FF of master into copy at address 0800.

(a) Depress "A" then "Program".

(b) Enter beginning address 2000 (2000+0000).

(c) Enter ending address 23FF (2000+03FF).

(d) Enter designation 4800 (4000+0800).

(e) After the last hex entry the block of data outlined was programmed into the copy starting at copy address 0800.

AMI
AMERICAN MICROSYSTEMS, INC.

ADS
ADVANCED DEVELOPMENT SUPPORT

PHOENIX — 1™ MICROCOMPUTER DEVELOPMENT STATION

Features

- ☐ **Low-Cost Microprocessor-Based Product Development**
- ☐ **Single High Density Computer with 48K Bytes RAM**
- ☐ **Built-In Interfaces for Line Printer, Universal PROM Programmer, and In-Circuit Emulation**
- ☐ **Software Compatible with AMI Pascal-based Advanced Development Suport Software for 17 Different Microprocessors**
- ☐ **ROM Monitor and Boot**
- ☐ **Extensive Self-test Capability**
- ☐ **Built-in Terminal with 12″ Diagonal Screen**
- ☐ **Three Mini-Floppy Disks**
- ☐ **Easily Upgraded to Include High Level Language and New Microprocessors**

General Description

The Phoenix-1 Microcomputer Development Station is a low-cost, self-contained development system providing Pascal-based software support for products within AMI's S2000 microprocessor families. Modular hardware units are easily configured to allow full in-circuit emulation. Optional software extends the development capability to the 17 products of the S6800, S9900 and many other popular microprocessor families.

A powerful Diskette Operating System, screen oriented editor and file manager increases the ease and efficiency of editing and assembling programs for any of AMI's microprocessors. When used in conjunction with an optional in-circuit emulation module, Phoenix-1 provides all the tools required to develop microcomputer-based products rapidly and cost effectively. To maximize the system's usefulness, hardware and software is included for communications with other computers. Thus you can easily transport programs between different systems.

Phoenix-1 Hardware Description

The Phoenix-1 is a ruggedly packaged computer system complete with a CRT, power supplies, cables, fans, triple 5¼″ single density floppy disks, electronic keyboard, numeric keypad and four printed circuit boards. The master CPU is contained on one board with 48K bytes of dynamic RAM and 2K bytes of ROM. Two interface cards are plugged into the CPU to communicate via the RS232 or floppy disks. The fourth board is a complete terminal controller board with its own CPU. Communication between the two main boards is via high speed serial lines.

All terminal functions can be controlled by the keyboard or software. Eight user-definable keys are provided for special functions. Direct cursor addressing minimizes response time and allows insertion and deletion anywhere on the screen. Upper and lower case letters in 5×7 and 7×9 matrices respectively are included in a 80×24 screen format. A 12″ diagonal CRT makes the 1,920 characters easy to read.

A single built-in 5¼″ floppy disk drive provides 102K bytes of on-line storage for the host operating system. Two additional disk drives brings the total storage up to 306K bytes. The hard sectored diskettes have 40 tracks and will seek to a track in less than 30ms.

Systems are enclosed in structural foam to ensure system reliability and integrity. Power supplies operate from 120/240 VAC 50/60 Hz. Service is provided through 300 U.S. and 100 overseas authorized Zenith service centers.

STATIC MOS RANDOM ACCESS MEMORIES

Part No.	Organization	Process	Max. Access Time(ns)	Max. Active Power(mW)	Max. Standby Power(mW)	Power Supplies	Package
S68B10	128×8	NMOS	250	420	N/A	+5V	24 Pin
S68A10	128×8	NMOS	360	420	N/A	+5V	24 Pin
S6810	128×8	NMOS	450	400	N/A	+5V	24 Pin
S6810-1	128×8	NMOS	575	500	N/A	+5V	24 Pin

STATIC CMOS RANDOM ACCESS MEMORIES

Part No.	Organization	Max. Access Time(ns)	Max. Active Power(mW)	Max. Standby Power(mW)	Power Supplies	Package
S5101L-1	256×4	450	115	.055	+5V	22 Pin
S5101L	256×4	650	115	.055	+5V	22 Pin
S5101L-3	256×4	650	115	.735	+5V	22 Pin
S5101-8	256×4	800	115	2.7	+5V	22 Pin
S6504[2]	4096×1	300	75	0.5	+5V	18 Pin
S6508-1	1024×1	300	13	.055	+5V	16 Pin
S6508	1024×1	460	13	.55	+5V	16 Pin
S6508A-1	1024×1	275/115[2]	12.5/50[2]	1.15	+4V to +11V	16 Pin
S6508A	1024×1	460/185[2]	12.5/50[2]	1.1	+4V to +11V	16 Pin
S6514[2]	1024×4	300	75	0.25	+5V	18 Pin

MOS READ ONLY MEMORIES

Part No.	Description	Organization	Process	Max. Access Time(ns)	Max. Active Power(mW)	Power Supplies	Package
S6831B	16,384 Bit Static ROM	2048×8	NMOS	450	370	+5	24 Pin
S68A316	16,384 Bit Static ROM	2048×8	NMOS	350	370	+5	24 Pin
S68332	32,768 Bit Static ROM	4096×8	NMOS	450	370	+5	24 Pin
S68A332	32,768 Bit Static ROM	4096×8	NMOS	350	370	+5	24 Pin
S2333	32,768 Bit Static ROM	4096×8	NMOS	350	370	+5	24 Pin
S68A364	65,536 Bit Static ROM	8192×8	NMOS	350	370	+5	24 Pin
S2364	65,536 Bit Static ROM	8192×8	NMOS	350	370	+5	28 Pin
S231282	131,072 Bit Static ROM	16,384×8	NMOS	250	—	+5	28 Pin

[1] Not recommended for new designs

[2] To be announced

AMERICAN MICROSYSTEMS, INC.

S5101

1024 BIT (256×4) STATIC CMOS RAM

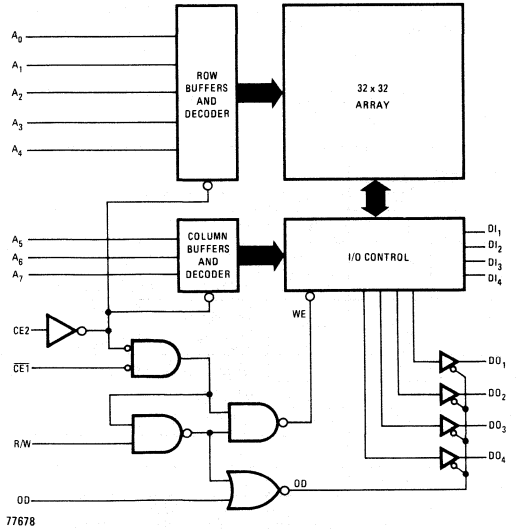
Features

- ☐ **Ultra Low Standby Power**
- ☐ **Data Retention at 2V (L Version)**
- ☐ **Single +5V Power Supply**
- ☐ **Completely Static Operation**
- ☐ **Completely TTL Compatible Inputs**
- ☐ **Three-State TTL Compatible Outputs**
- ☐ **Available in Commercial, Industrial, and Military Temperature Range**

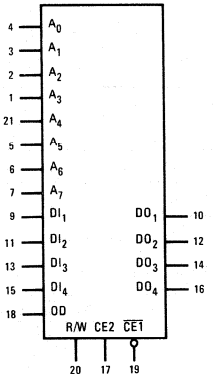
General Description

The AMI S5101 family of 256× 4-bit ultra low power CMOS RAMs offers fully static operation with a single +5 volt power supply. All inputs and outputs are directly TTL compatible. With data inputs and outputs on adjacent pins, either separate or common data I/O operations can easily be implemented for maximum design flexibility. The three-state outputs will drive one full TTL load and are disabled (high impedance state) by output disable (OD), either chip enable ($\overline{CE1}$ or CE2), or in a write cycle (R/W = LOW). This facilitates the control of common data I/O systems.

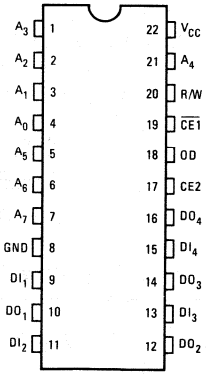
Block Diagram



Logic Symbol



Pin Configuration



Truth Table

$\overline{CE1}$	CE2	OD	R/W	DIN	Output	Mode
H	X	X	X	X	High Z	Not selected
X	L	X	X	X	High Z	Not Selected
X	X	H	H	X	High Z	Output Disabled
L	H	H	L	X	High Z	Write
L	H	L	L	X	*High Z	Write
L	H	L	H	X	Dout	Read

*Also available with D_{IN} on output during Write—consult AMI Sales Office

Pin Names

A_0 - A_7	Address Inputs	$\overline{CE1}$	Chip Enable
DI_1 - DI_4	Data Inputs	CE2	Chip Enable
DO_1 - DO_4	Data Outputs	R/W	Read/Write Input
OD	Output Disable	V_{CC}	+5 Volt Power Supply

RAMs

General Description (Continued)

The stored data is read out nondestructively and is the same polarity as the original input data. The S5101 is totally static, making clocks unnecessary for a new address to be accepted. The device has two chip enable inputs ($\overline{CE1}$ and CE2) allowing easy system expansion. CE2 disables the entire device but $\overline{CE1}$ does not disable the address buffers and decoders. Thus, minimum power dissipation is achieved when CE2 is low.

The L version of the S5101 has the additional feature of guaranteed data retention with the power supply as low as 2 volts. This makes the device an ideal choice when battery augmented non-volatile RAM storage is mandatory.

The S5101 is fabricated using a silicon gate CMOS process suitable for high volume production of ultra low power, high performance memories.

Absolute Maximum Ratings*

Ambient Temperature Under Bias—T_A (Standard Part)	0°C to +70°C
(Industrial temp part)	−40°C to +85°C
(Military temp part)	−55°C to +125°C
Storage Temperature	−65°C to 150°C
Voltage on Any Pin with Respect to Ground	−0.3V to V_{CC} +0.3V
Maximum Power Supply Voltage	8V
Power Dissipation	1W

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics: T_A=0°C to +70°C (Standard part); −40°C to +85°C (Industrial temp part); −55°C to +125°C (Military temp part), V_{CC}=5V±5% (unless otherwise specified)

Symbol	Parameter		Limits Min.	Limits Max.	Units	Conditions
I_{LI}	Input Leakage Current			1	μA	V_{IN} = 0V to V_{CC}
I_{LO}	Output Leakage Current			1	μA	$\overline{CE1}$ = V_{IH} V_{OUT} = 0V to V_{CC}
I_{CC}	Operating Supply Current			22	mA	Outputs = Open, V_{IN} = V_{IL} to V_{CC}
I_{CCL}	Standby Supply Current	S5101L1, S5101L		10	μA	V_{IN} = 0V to V_{CC}
		S5101L3		140	μA	except
		S5101L8, S5101-8		500	μA	CE2 ⩽ 0.2V
V_{IL}	Input Low Voltage		-0.3	0.65	V	
V_{IH}	Input High Voltage		2.2	V_{CC}	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 2 mA
V_{OH}	Output High Voltage		2.4		V	I_{OH} = -1 mA

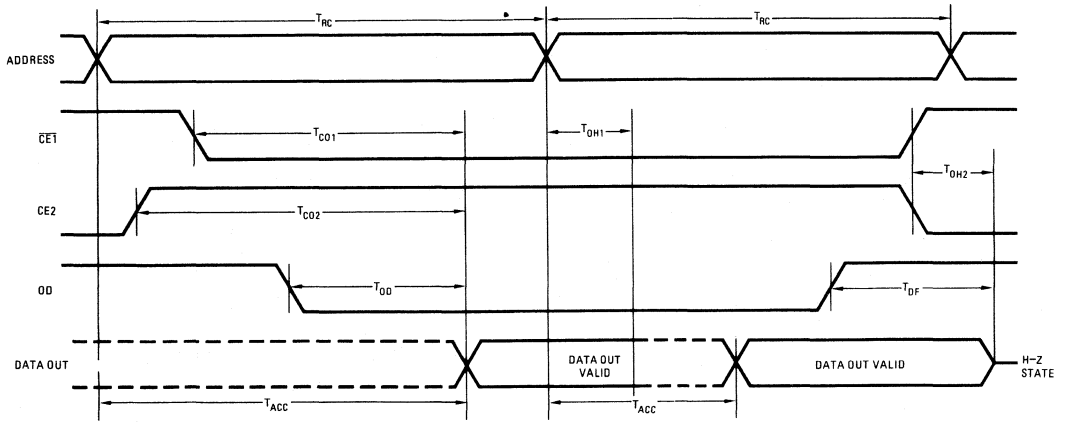
Capacitance

Symbol	Parameter	Limits Min.	Limits Max.	Units	Conditions
C_{IN}	Input Capacitance		8	pF	V_{IN} = 0V, on all Input Pins
C_O	Output Capacitance		12	pF	V_O = 0V

A.C. Characteristics for Read Cycle: $T_A = 0°C$ to $+70°C$ (Standard part); $-40°C$ to $+85°C$ (Industrial temp part); $-55°C$ to $+125°C$ (Military temp part), $V_{CC} = 5V \pm 5\%$ (unless otherwise specified)

Symbol	Parameter	S5101L1 Limits		S5101L S5101L3 Limits		S5101L8 S5101-8 Limits		Units	Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
T_{RC}	Read Cycle Time	450		650		800		ns	See A.C. Conditions of Test and A.C. Test Load
T_{ACC}	Access Time		450		650		800	ns	
T_{CO1}	$\overline{CE1}$ to Output Delay		400		600		800	ns	
T_{CO2}	CE2 to Output Delay		500		700		850	ns	
T_{OD}	Output Disable to Enabled Output Delay		250		350		450	ns	
T_{DF}	Output Disable to Output H-Z State Delay	0	130	0	150	0	200	ns	
T_{OH1}	Output Data Valid Into Next Cycle with respect to Address	0		0		0		ns	
T_{OH2}	Output Data Valid Into Next Cycle with respect to Chip Enable	0		0		0		ns	

Read Cycle



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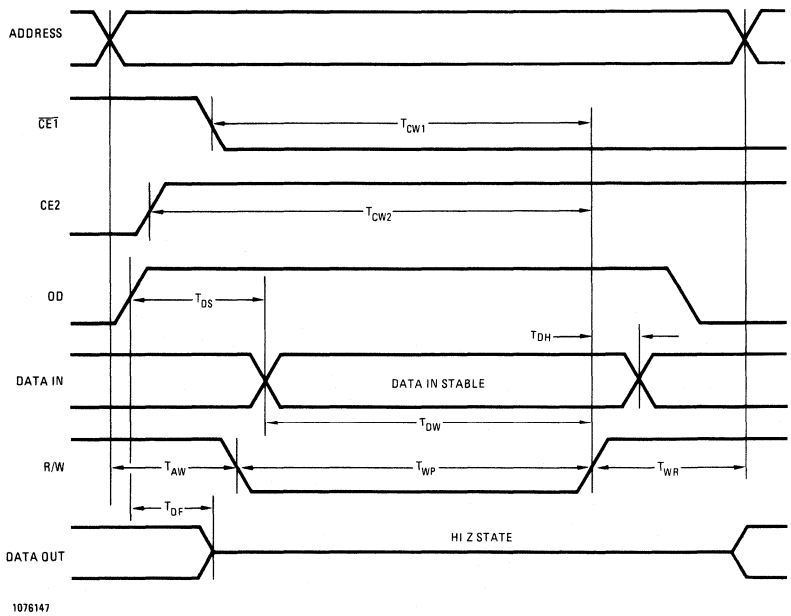
Note:
1. OD may be tied low for seaprate I/O information.
2. The output will go into a high impedance state if either CE1 is high, CE2 is low, OD is high or R/W is low.

RAMs

A.C. Characteristics for Write Cycle—Separate or Common Data I/O Using Output Disable: $T_A = 0°C$ to $+70°C$ (Standard part); $-40°C$ to $+85°C$ (Industrial temp part); $-55°C$ to $+125°C$ (Military temp part), $V_{CC} = 5V \pm 5\%$ (unless otherwise specified)

Symbol	Parameter	S5101L1 Limits		S5101L S5101L3 Limits		S5101L8 S5101-8 Limits		Units	Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
T_{WC}	Write Cycle Time	450		650		800		ns	See A.C. Conditions of Test and A.C. Test Load
T_{AW}	Address To Write Delay	130		150		200		ns	
T_{CW1}	CE1 to Write Delay	350		550		650		ns	
T_{CW2}	CE2 to Write Delay	350		550		650		ns	
T_{DW}	Data Set-Up to End of Write Time	250		400		450		ns	
T_{DH}	Data Hold After End of Write Time	50		100		100		ns	
T_{WP}	Write Pulse Width	250		400		450		ns	
T_{WR}	End of Write to New Address Recovery Time	50		50		100		ns	
T_{DS}	Output Disable to Data-In Set-Up Time	130		150		200		ns	

Write Cycle — For Separate or Common Data I/O

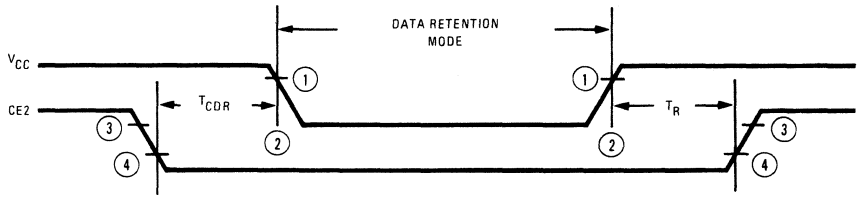


Low V_{CC} Data Retention Characteristics for S5101L, S5101L1, S5101L3 and S5101L8[1]: T_A=0°C to +70°C (Standard part); −40°C to +85°C (Industrial temp part); −55°C to +125°C (Military temp part), V_{CC}=5V±5% (unless otherwise specified)

Symbol	Parameter		Limits Min.	Limits Max.	Units	Conditions
V_{DR}	V_{CC} for Data Retention		2.0		V	CE2≤0.2V
I_{CCDR}	Data Retention Supply Current	S5101L1, S5101L		10	μA	V_{CC} = V_{DR}
		S5101L3		140	μA	T_R = T_F = 20ns
		S5101L8		500	μA	CE2≤0.2V
T_{CRD}	Chip Deselect to Data Retention Time		0		ns	
T_R	Operation Recovery Time		T_{RC}[2]		ns	

Notes:
[1] For guaranteed low V_{CC} Data Retention @ 2.0V, order must specify S5101L, S5101L1, S5101L3 or S5101L8.
[2] T_{RC} = Read Cycle Time.

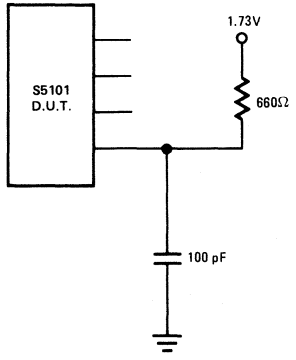
Low V_{CC} Data Retention Wave Form



1. 4.75V
2. V_{DR}
3. V_{IH}
4. 0.2V

477215

A.C. Test Load



1076146

A.C. Conditions of Test

Input Levels	0.65V to 2.2V
Input Rise and Fall Time	20ns
Timing Measurement Reference Level	1.5V

RAMs

S5101 Ordering Information

		0°C to +70°C	−40°C to +85°C	−55°C to −125°C
S5101L1	Plastic	S5101L1P	S5101L1PI	N/A
	Cerdip	S5101L1E	S5101L1EI	N/A
450ns; 10μA Standby	Ceramic	S5101L1C	S5101L1CI	S5101L1CM
S5101L	Plastic	S5101LP	N/A	N/A
	Cerdip	S5101LE	N/A	N/A
650ns; 10μA Standby	Ceramic	S5101LC	N/A	N/A
S5101L3	Plastic	S5101L3P	S5101L3PI	N/A
	Cerdip	S5101L3E	S5101L3EI	N/A
650ns; 140μA Standby	Ceramic	S5101L3C	S5101L3CI	S5101L3CM
S5101L8; S5101-8	Plastic	S5101L8P, S5101-8P	N/A	N/A
	Cerdip	S5101L8E, S5101-8E	N/A	N/A
800ns; 500μA Standby	Ceramic	S5101L8C, S5101-8C	N/A	N/A

N/A = Not Available

NOTE: Also available with MIL STD 883B processing. See Data Sheet for Military 5101L4

AMERICAN MICROSYSTEMS, INC.

S6508/S6508A

1024 BIT (1024×1) STATIC CMOS RAM

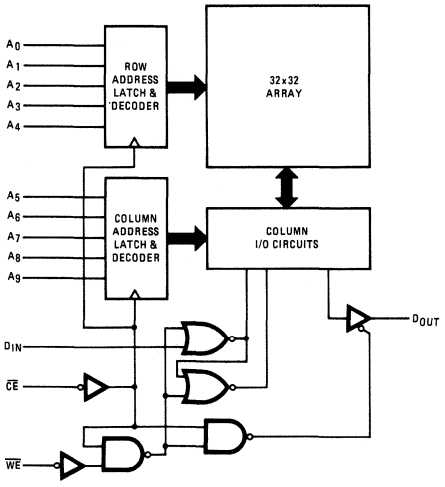
Features

- ☐ **Ultra Low Standby Power**
- ☐ **S6508 Completely TTL Compatible**
- ☐ **S6508A Completely CMOS Compatible**
- ☐ **4V to 11V Operation (S6508)**
- ☐ **Data Retention at 2V**
- ☐ **Three-State Output**
- ☐ **Low Operating Power: 10mW @1MHz (5V)**
- ☐ **Fast Access Time: 185ns @10V**
- ☐ **Available in Commercial, Industrial and Military Temperature Ranges**

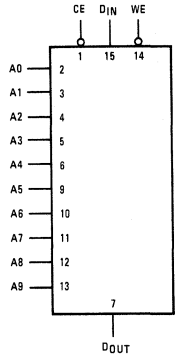
General Description

The AMI S6508 family of 1024×1 bit static CMOS RAMs offers ultra low power dissipation with a single power supply. The device is available in two versions. The basic part (S6508) operates on 5V and is directly TTL compatible on all inputs and the three-state output. The S6508 "A" operates from 4V to 11V and is fully CMOS compatible. The data is stored in ultra low power CMOS static RAM cells (six transistor). The stored data is read out nondestructively and is the same polarity as the original input data. The address is buffered by on-chip address registers. These internal registers are latched by the HIGH to LOW transition of chip enable ($\overline{CE}$). The write enable and chip enable functions are designed such that either separate or common data I/O operations can be easily implemented for maximum design flexibility.

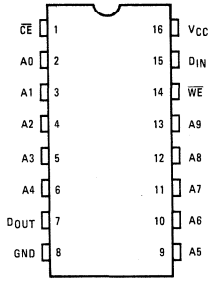
Block Diagram



Logic Symbol



Pin Configuration



Pin Names

A_0—A_9	Address Inputs
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
V_{CC}	Power Supply

RAMs

General Description (Continued)

The S6508 is fabricated using a silicon gate CMOS process suitable for high volume production of high performance, ultra low power memories. When deselected ($\overline{CE}$ = HIGH), the S6508-1 draws less than 10 microamps from the 5V supply. In addition, it offers guaranteed data retention with the power supply as low as 2 volts. This process makes the device an ideal choice where battery augmented nonvolatile RAM storage is mandatory.

CMOS to TTL—S6508/S6508-1
Absolute Maximum Ratings

Supply Voltage	8.0V
Input or Output Voltage Supplied	GND−0.5V to V_{CC}+0.5V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range —T_A (Standard Part)	0°C to +70°C
(Industrial temp part)	−40°C to +85°C
(Military temp part)	−55°C to +125°C

D.C. Characteristics: T_A=0°C to +70°C (Standard part); −40°C to +85°C (Industrial temp part); −55°C to +125°C (Military temp part), V_{CC}=5V±5% (unless otherwise specified)

Symbol	Parameter		Min.	Max.	Units	Conditions
V_{IH}	Logical "1" Input Voltage		V_{CC}−2.0		V	
V_{IL}	Logical "0" Input Voltage			0.8	V	
I_{IL}	Input Leakage		−1.0	1.0	μA	0V V_{IN} V_{CC}
V_{OH2}	Logical "1" Output Voltage		V_{CC}−0.01		V	I_{OUT}=0
V_{OH1}	Logical "1" Output Voltage		2.4		V	I_{OH}=−0.2mA
V_{OL2}	Logical "0" Output Voltage			GND+0.01	V	I_{OUT}=0
V_{OL1}	Logical "0" Output Voltage			0.45	V	I_{OL}=2.0mA
I_O	Output Leakage		−1.0	1.0	μA	0V V_O V_{CC}, $\overline{CE}$=V_{IH}
I_{CCL}	Standby Supply Current	S6508		100	μA	V_{IN}=V_{CC}, $\overline{CE}$=V_{IH}
		S6508-1		10	μA	
I_{CC}	Supply Current S6508/S6508-1			2.0	mA	f=1MHz
C_{IN}	Input Capacitance			7.0	pF	
C_O	Output Capacitance			10.0	pF	

A.C. Characteristics: T_A=0°C to +70°C (Standard part); −40°C to +85°C (Industrial temp part); −55°C to +125°C (Military temp part), V_{CC}=5V±5% (unless otherwise specified)

Symbol	Parameter	S6508-1		S6508		Units	Conditions
		Min.	Max.	Min.	Max.		
t_{ACC}	Access Time from $\overline{CE}$		300		460	ns	See A.C. conditions of test and A.C. test load
t_{EN}	Output Enable Time		180		285	ns	
t_{DIS}	Output Disable Time		180		285	ns	
t_{CEH}	$\overline{CE}$ HIGH	200		300		ns	
t_{CEL}	$\overline{CE}$ LOW	300		460		ns	
t_{WP}	Write Pulse Width (LOW)	200		300		ns	
t_{AS}	Address Setup Time	7		15		ns	
t_{AH}	Address Hold Time	90		130		ns	
t_{DS}	Data Setup Time	200		300		ns	
t_{DH}	Data Hold Time	20		20		ns	
t_{MOD}	Data Modify Time	0		0		ns	

CMOS to CMOS—S6508A
Absolute Maximum Ratings

Supply Voltage	12.0V
Input or Output Voltage Supplied	−0.5V to V_{CC}+0.5V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range —T_A (Standard Part)	0°C to +70°C
(Industrial temp part)	−40°C to +85°C
(Military temp part)	−55°C to +125°C

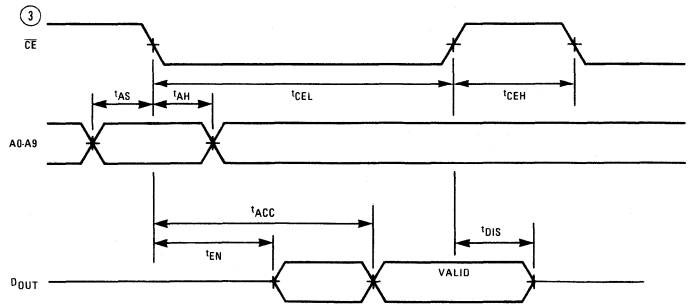
D.C. Characteristics: T_A=0°C to +70°C (Standard part); −40°C to +85°C (Industrial temp part); −55°C to +125°C (Military temp part), V_{CC}=5V±5% (unless otherwise specified)

Symbol	Parameter	Min.	Max.	Units	Conditions
V_{IH}	Logical "1" Input Voltage	70% V_{CC}		V	
V_{IL}	Logical "0" Input Voltage		20% V_{CC}	V	
I_{IL}	Input Leakage	−1.0	1.0	μA	0V V_{IN} V_{CC}
V_{OH}	Logical "1" Output Voltage	V_{CC}−0.01		V	I_{OUT}=0
V_{OL}	Logical "0" Output Voltage		GND+0.01	V	I_{OUT}=0
I_O	Output Leakage	−1.0	1.0	μA	0V V_O V_{CC}, $\overline{CE}$=V_{IH}
I_{CCL}	Standby Supply Current		500	μA	V_{IN}=V_{CC}, $\overline{CE}$=V_{IH}
I_{CC}	Supply Current V_{CC}=5V		2.0	mA	f=1MHz
	Supply Current V_{CC}=10V		4.3	mA	f=1MHz
C_{IN}	Input Capacitance		7.0	pF	
C_O	Output Capacitance		10.0	pF	

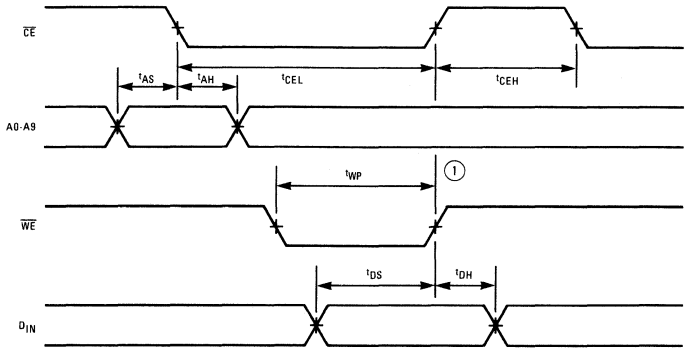
A.C. Characteristics: T_A=0°C to +70°C (Standard part); −40°C to +85°C (Industrial temp part); −55°C to +125°C (Military temp part), V_{CC}=5V±10% (unless otherwise specified)

Symbol	Parameter	V_{CC}	Min.	Max.	Units	Conditions
t_{ACC}	Access Time from $\overline{CE}$	5V		460	ns	See A.C. conditions of test and A.C. test load
		10V		185	ns	
t_{EN}	Output Enable Time	5V		285	ns	
		10V		120	ns	
t_{DIS}	Output Disable Time	5V		285	ns	
		10V		120	ns	
t_{CEH}	$\overline{CE}$ HIGH	5V	300		ns	
		10V	125		ns	
t_{CEL}	$\overline{CE}$ LOW	5V	460		ns	
		10V	185		ns	
t_{WP}	Write Pulse Width (LOW)	5V	300		ns	
		10V	125		ns	
t_{AS}	Address Setup Time	5V	15		ns	
		10V	15		ns	
t_{AH}	Address Hold Time	5V	130		ns	
		10V	60		ns	
t_{DS}	Data Setup Time	5V	300		ns	
		10V	125		ns	
t_{DH}	Data Hold Time	5V	20		ns	
		10V	125		ns	
t_{MOD}	Data Modify Time	5V	0		ns	
		10V	0		ns	

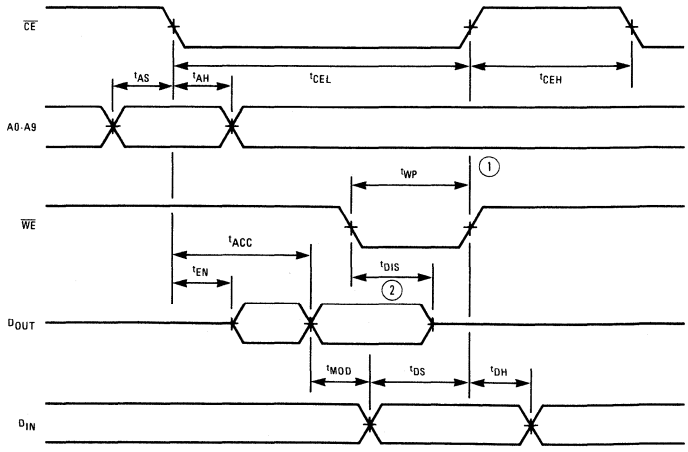
Read Cycle



Write Cycle



Read Modify Write Cycle



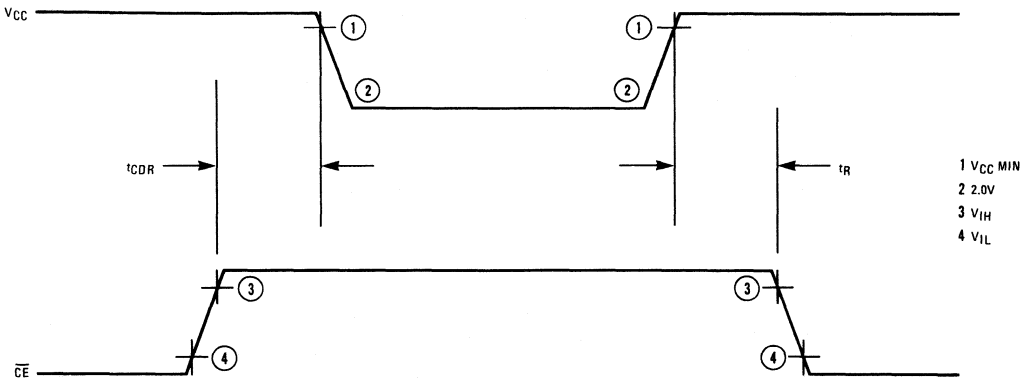
NOTES:

1. The write operation is terminated on any positive edge of Chip Enable ($\overline{CE}$) or Write Enable ($\overline{WE}$).
2. The data output will be in the high impedance state whenever $\overline{WE}$ is LOW.
3. $\overline{WE}$ is HIGH during a read operation.
4. Rise and fall times of V_{CC} equal 20ns.

D.C. Characteristics: T_A=0°C to +70°C (Standard part); −40°C to +85°C (Industrial temp part); −55°C to +125°C (Military temp part), V_{CC}=5V±5% (unless otherwise specified)

Symbol	Parameter		Min.	Max.	Units	Conditions
V_{DR}	V_{CC} for Data Retention		2.0		V	$\overline{CE}$ = 2.0V
I_{CCDR}	Data Retention	S6508,S6508A		10	μA	$V_{CC}=V_{DR}$ Min.
	Supply Current	S6508-1		1.0	μA	$t_r=t_f$=20ns
t_{CDR}	Deselect Setup Time		t_{CEH}		ns	
t_r	Recovery Time		t_{CEH}		ns	

Low V_{CC} Data Retention Waveform



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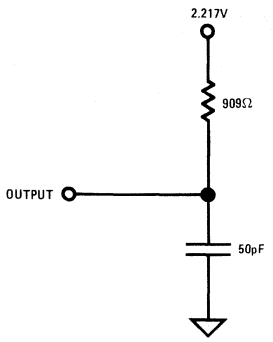
A.C.Test Load



877244

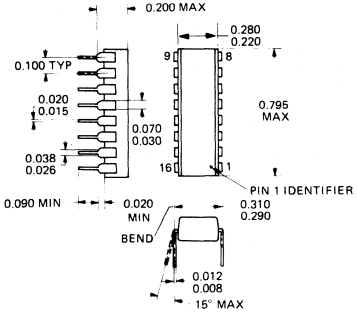
A.C. Test Conditions

Input Levels ..... V_{IL} to V_{IH}
Input Rise & Fall 20ns
Timing Measurement Reference Level
S6508/S6508-1 ..... 1.5V
S6508A ..... 50% V_{CC}

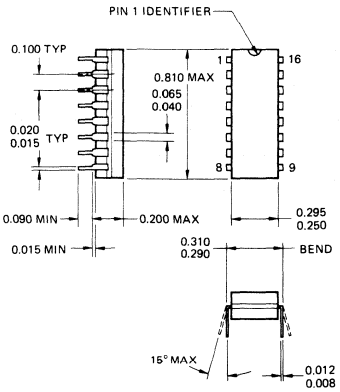
RAMs

Package Outlines

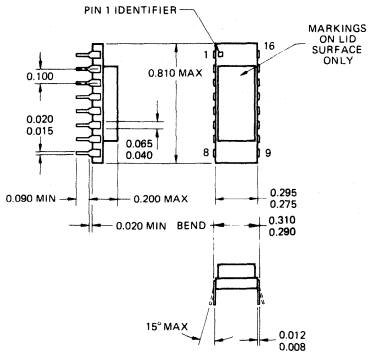
16-Pin Plastic



16-Pin Cer-DIP



16-Pin Ceramic



Ordering Information

Device	Access Time	Low V_{CC} Stby I_{CC}	Package	Order Number		
				0°C to +70°C	−40°C to +85°C	−55°C to +25°C
S6508	460	10μA	Plastic	S6508P	S6508PI	N/A
			Cerdip	S6508E	S6508EI	N/A
			Ceramic	S6508C	S6508CI	S6508CM
S6508-1	300	1μA	Plastic	S65081P	S65081PI	N/A
			Cerdip	S65081E	S65081EI	N/A
			Ceramic	S65081C	S65081CI	S65081CM
S6508A	185 @10V	10μA	Plastic	S6508AP	S6508API	N/A
			Cerdip	S6508AE	S6508AEI	N/A
			Ceramic	S6508AC	S6508ACI	S6508ACM

N/A = Not Available

AMERICAN MICROSYSTEMS, INC.

ADVANCED PRODUCT DESCRIPTION

S6514

4096 BIT (1024 × 4) STATIC CMOS RAM

Features

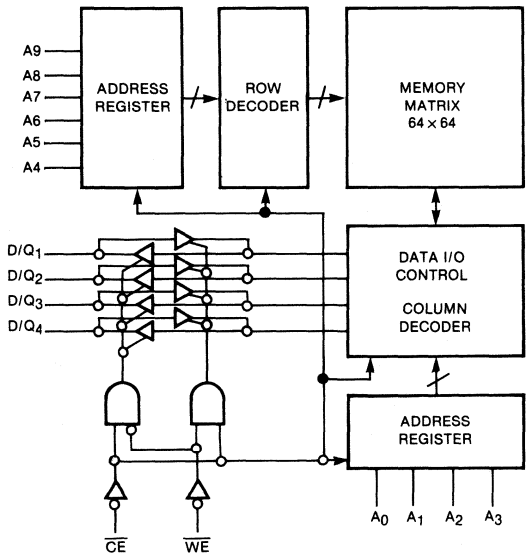
- ☐ **Low Power Standby—1mW MAX**
- ☐ **TTL Compatible Inputs/Outputs**
- ☐ **Three-State Outputs**
- ☐ **On-Chip Address Registers**
- ☐ **Data Retention @ 2V**
- ☐ **Standard 18 pin Package/Pinouts**

General Description

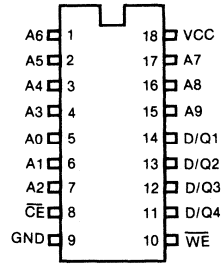
The AMI S6514 is a 1024x4 static CMOS RAM offering low power and static operation with a single +5 volt power supply. All inputs and outputs are TTL compatible. The common Data I/O pins allow direct interface with common bus systems.

Battery-backup design is simplified by use of $\overline{CE}$, which when HIGH, allows the other inputs to float.

Block Diagram



Pin Connections



Pin Names

A0-A9	Address Inputs
D/Q_1-D/Q_4	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable

Truth Table

Mode	$\overline{E}$	$\overline{W}$	Data Out
Read	L	H	Data In
Write	L	L	HI-Z
Disable	H	X	HI-Z

RAMs

Absolute Maximum Ratings

Supply Voltage $-V_{CC}$	$-0.3V$ to $+7.0V$
Input/Output Voltage Applied	$-0.3V$ to $V_{CC}+0.3V$
Storage Temperature $-T_{stg}$	$-65°C$ to $+150°C$

DC Electrical Characteristics: $T_A = 0°C$ to $70°C$, $V_{CC} = +5V \pm 10\%$

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_{LI}	Input Leakage Current	−1		1	μA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current			1	μA	V_{IN} = GND to V_{CC}
I_{SB}	Standby Supply Current			50	μA	V_{IN} = GND or V_{CC}
I_{CC}	Operating Supply Current			7	mA	V_{IN} = GND or V_{CC}, f = MHz
V_{IL}	Input Voltage LOW	−0.3		0.8	V	
V_{IH}	Input Voltage HIGH	2.4		$V_{CC}+0.3$	V	
V_{OL}	Output Voltage LOW			0.4	V	I_{OL} = 1.6mA
V_{OH}	Output Voltage HIGH	2.4			V	I_{OH} = −0.4mA

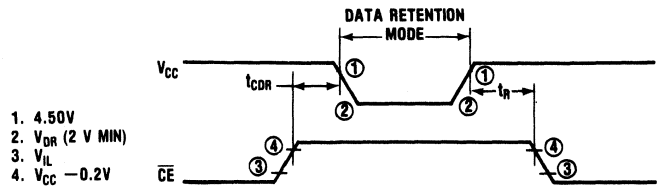
Capacitance: $T_A = 25°C$, t = 1MHz. Capacitance is sampled and guaranteed.

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
C_{IN}	Input Capacitance			8	pF	GND to V_{CC}
C_{OUT}	Output Capacitance			10	pF	GND to V_{CC}

Low V_{CC} Data Retention Characteristics:

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_{CCDR}	I_{CC} for Data Retention			25	μA	V_{IN} = GND to V_{CC}; V_{CC} = 3V
V_{CCDR}	V_{CC} for Data Retention	2.0			V	
t_{CDR}	Chip Deselect to Data Retention Time	0			ns	
t_R	Operation Recovery Time	TELEL				

Low V_{CC} Data Retention Wave Form



AC Test Conditions

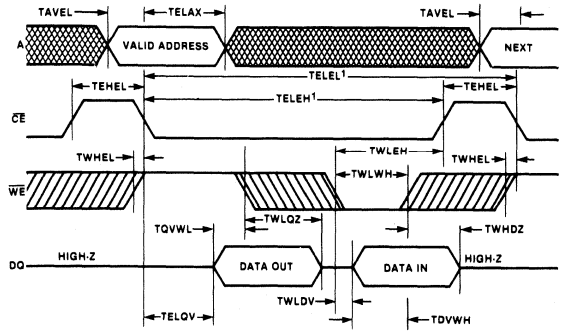
t rise/t fall	20ns
Output Load	1 TTL Load & 50pF
All	Timing 1.5V

AC Electrical Characteristics: $T_A = 0°C$ to $70°C$, $V_{CC} = +5V \pm 10\%$

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
TELQV	Chip Enable Access Time			300	ns	
TAVQV	Address Access Time			320	ns	
TWLQZ	Write Enable Output Disable Time			100	ns	
TEHQZ	Chip Enable Output Disable Time			100	ns	
TELEH	Chip Enable Pulse Negative Width	300			ns	
TEHEL	Chip Enable Pulse Positive Width	120			ns	
TAVEL	Address Setup Time	20			ns	
TELAX	Address Hold Time	50			ns	
TWLWH	Write Enable Pulse Width	300			ns	
TWLEH	Write Enable Pulse Setup Time	300			ns	
TELWH	Write Enable Pulse Hold Time	300			ns	
TDVWH	Data Setup Time	200			ns	
TWHDZ	Data Hold Time	0			ns	
TWHEL	Write Enable Read Setup Time	0			ns	
TQVWL	Output Data Valid to Write Time	0			ns	
TWLDV	Write Data Delay Time	100			ns	
TELWL	Early Output High-Z Time			0	ns	
TWHEH	Late Output High-Z Time			0	ns	
TELEL	Read or Write Cycle Time	420			ns	

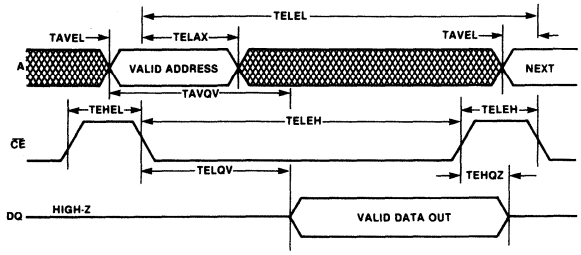
RAMs

Read Modify Write Cycle

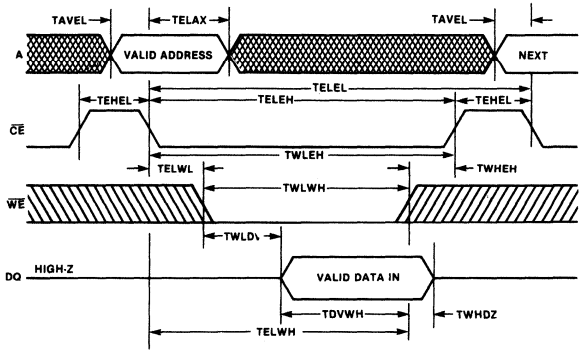


Note 1: TELEL & TELEH are longer than the minimum given for Read or Write cycle.

Read Cycle: $\overline{WE}$ = HIGH

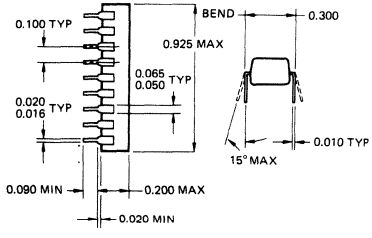


Write Cycle

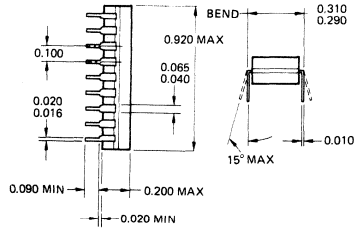


Package Outlines

18-Pin Plastic

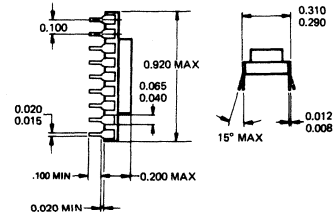


18-Pin Cer-DIP



2P

18-Pin Ceramic



Ordering Information

The following information should be included in the purchase order when ROM devices are being ordered.

- ☐ Part number
- ☐ Number of ROM patterns
- ☐ Quantity of prototypes for each pattern (if none, so state)
- ☐ Total quantity of each pattern
- ☐ Special marking (if required)
- ☐ *Method of ROM code entry (EPROM, punched paper tape, etc.)
- ☐ *Chip select definition —
- ☐ Pricing and delivery (pricing and delivery quotes can be obtained from any AMI Sales Office)

*If ordering a previously supplied pattern, the order should refer to the AMI C number (CXXXXX). This C number can be obtained from previous AMI billing or acknowledgement.

UNIT QUANTITY VARIANCE

AMI manufactures ROMS in a fully proven silicon gate N-channel process. However, as in any semi-conductor production, yield variations do occur. Because of these normal yield variations a policy has been established that requires the customer to accept a small variation from the nominal quantity ordered.

Unit Quantity Variance ±5% or 50 units (whichever is greater)

PART NUMBER

An AMI ROM part number consists of a device number followed by a single letter designating the package type.

P — designates plastic package
C — designates ceramic package (hermetic seal)

Device Numbers

S6831B/S68A316	2K×8	
S68A332/S68332	4K×8	Standard Pinout
S2333	4K×8	(Pin compatible with 2732 EPROM)
S68A364	8K×8	(24 Pin)
S2364	8K×8	(28 Pin-Compatible W/2764 EPROM)
*S23128	16K×8	(28 Pin)

*To Be Announced

ROM Sales Policy

MINIMUM ORDER QUANTITY

Capacity	Part No.	Architecture	Units/Pattern
16K	S6831B, S68A316	2K×8	1,000
32K	S68332, S68A332	4K×8	500
32K	S2333 (Alternate Pinout)	4K×8	500
64K	S68A364 (24-Pin)	8K×8	250
64K	S2364 (28-Pin)	8K×8	250
*128K	S23128 (28-Pin)	16K×8	125

*To Be Announced

Unless otherwise requested by the customer, approximately 5 units will be assembled in a ceramic package for verification of the ROM pattern by the customer. These 5 units will be considered as part of the total quantity ordered.

Mask Charges*

Most ROM suppliers charge a mask charge to cover the expense of generating tooling that is unique to each ROM pattern. Current AMI mask charges are as follows.

		Min. Qty/Mask Charges		
Part No.	Architecture	250 Pcs.	500 Pcs.	1000 Pcs.
S6831B, S68A316	2K×8	N/A	N/A	$ 500
S68332, S68A332, S2333	4K×8	N/A	$1000	$ 750
S68A364, S2364	8K×8	$1500	$1200	$1000

*Subject to Change

Reorder Policy

If a customer wishes to reorder the same ROM pattern, the following policy applies. If finished inventory exists, no minimum quantity limits will be imposed. However, if new wafer starts are required, the same minimum quantity as for a new pattern will apply. The 5 prototypes (supplied with new patterns) will not be supplied. No mask charge is applied to a reorder of a previously supplied ROM pattern.

DELIVERY

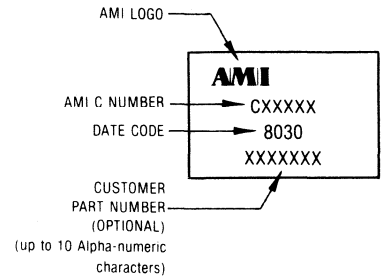
Exact delivery dates must be quoted by AMI Customer Service when the order is placed. The following general guidelines apply.

Prototypes	(5 Units)	5 wks.	(After Pattern Verification)
First Production	(250/500 Units)	7 wks. 7 wks.	(Or 4 wks. after prototype approval)
Quantity Production	(Any Quantity)	9-11 wks.	

ROM PACKAGE MARKING

Unless otherwise specified, AMI ROM's are marked with a C number (the letter C followed by a 5 digit number) and a date code. This C number identifies both the device type and the specific pattern. This C number will be used on all AMI documents concerning the ROM.

A ROM can also be marked with a number supplied by the customer. A single number of up to 10 alpha numeric characters can be marked on the device without extra charge. Other customer markings are possible, but must be approved before the order is entered.



ROM CODE DATA

AMI's preferred method of receiving ROM CODE DATA is in EPROM. Two EPROMs should be submitted. One is programmed to the desired code and the other is blank. AMI will read the programmed EPROM, transfer this data to diskette and then program the blank EPROM from the stored information. This procedure guarantees that the EPROM has been properly entered into the AMI computer system. The AMI programmed EPROM is returned to the customer for verification of the ROM program. Unless otherwise requested, AMI will not proceed until the customer verifies the program in the returned EPROM.

EPROM REQUIREMENTS

The following EPROMs should be used for submitting ROM Code Data:

ROM		EPROM	
		PREFERRED	OPTIONAL
S68A316, S6831B	2K×8	2716/2516	2-2708
S68332/S68A332	4K×8	2532	2-2716/2516
S2333	4K×8	2732	2-2716/2516
S68A364	8K×8	2-2532	4-2716/2516
S2364	8K×8	2764	2-2732

If two EPROM's are used to specify one ROM pattern, (i.e., 2 16K EPROMs for one 32K ROM) two blank EPROMs must be submitted. In this instance, the programmed EPROMs must clearly state which of the two EPROMs is for lower and upper address locations in the ROM. The preferred method is to mark the EPROM with the ROM address (in Hex) where the EPROM data is to be located.

Example: Two 2716 EPROMs for S68332 ROM
Marking: EPROM # 1 000-7FF
EPROM # 2 800-FFF

PATTERN DATA FROM ROMs

If a customer has ROMs produced by another supplier, these ROMs can be submitted for ROM pattern data instead of EPROMs. Obviously, these ROMs must be pin compatible with the AMI device. The programmable chip selects must be defined. (NOTE: In some cases a competitor's ROM may have a chip select or enable that is not customer defined. However, if this pin is customer defined for the AMI ROM, the required active logic level for this input must be specified.).

OPTIONAL METHOD OF SUPPLYING ROM CODE DATA

If an EPROM or ROM cannot be supplied, the following other methods are acceptable.

- ☐ 9 Track NRZ Magnetic Tape (2 each) odd parity, 800 BPI
- ☐ Paper Tape (AMI Hex format)
- ☐ Card Deck (AMI Hex format)

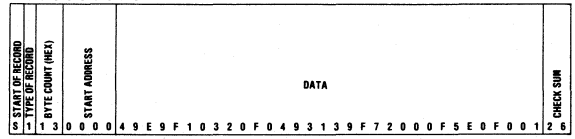
The AMI Hex format is described below. With its built-in address space mapping and error checking, this format is produced by the AMI Assembler.

Position	Description
1	Start of record (Letter S)
2	Type of record 0—Header record (comments) 1—Data record 9—End of file record
3, 4	Byte Count Since each data byte is represented as two hex characters, the byte count must be multiplied by two to get the number of characters to the end of the record. (This includes checksum and address data.) Records may be of any length defined in each record by the byte count.

Position	Description
5, 6, 7, 8	Address Value The memory location where the first data byte of this record is to be stored. Addresses should be in ascending order.
9,..., N	Data Each data byte is represented by two hex characters. Most significant character first.
N+1, N+2	Checksum The one's complement of the additive summation (without carry) of the data bytes, the address, and the byte count.

Example:

```
S1130000 49E9F1032 0F04933 9F72000 F5E0F00 126
S9030000 FC
```



Paper tape format is the same as the card format above except:

a. The record should be a maximum of 80 characters.
b. Carriage return and line feed after each record followed by another record.
c. There should NOT be any extra line feed between records at all.
d. After the last record, four (4) $$$$ (dollar) signs should be punched with carriage return and line feed indicating end of file.

AMERICAN MICROSYSTEMS, INC.

S6831B/S68A316

16,384 BIT (2048x8) STATIC NMOS ROM

Features

- ☐ **Single +5V Power Supply**
- ☐ **Directly TTL Compatible Inputs**
- ☐ **Three-State TTL Compatible Outputs**
- ☐ **Three Programmable Enables**
- ☐ **Access Time: 450ns Maximum—S6831B**
  350ns Maximum—S68A316
- ☐ **2716 EPROM Pin Compatible**
- ☐ **Extended Temperature Range Available**

General Description

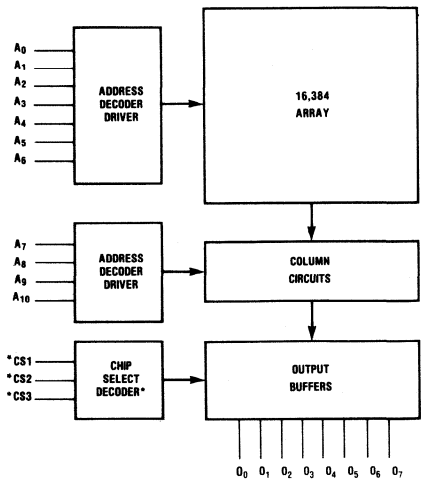
The AMI S6831B is a 16,384 bit mask programmable Read-Only-Memory offering fully static operation with a single +5V power supply. The device is fully TTL compatible on all inputs and three-state outputs. The three enables are mask programmable, the active level is specified by the user.

The S6813B is pin compatible with the 2516 and 2716 EPROMs. Software developed in EPROMs can be put in low cost ROM for high volume production.

The device is organized as 2048 words by 8 bits, a configuration particularly suitable for microprocessors. The S6831B is manufactured with an N-channel silicon gate depletion load technology.

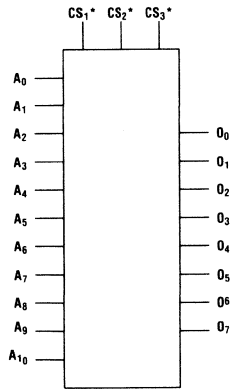
The S68A316 is a high speed version of the S6831B.

Block Diagram



*PROGRAMMABLE CHIP SELECTS

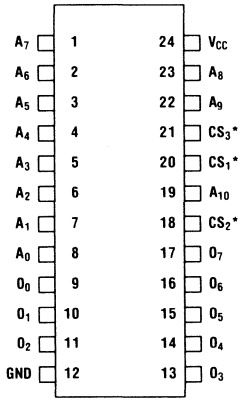
Logic Symbol



Pin Names

A_0-A_{10}	Address Inputs
O_0-O_7	Data Outputs
CS1—CS3	Chip Select Inputs
V_{CC}	+5V Power Supply

Pin Configuration



ROMs

Absolute Maximum Ratings*

Ambient Temperature Under Bias—T_A (Standard Part)	0°C to +70°C
(Industrial temp part)	−40°C to +85°C
Storage Temperature	−65°C to 150°C
Output or Supply Voltages	−0.5V to 7V
Input Voltages	−0.5V to 7V
Power Dissipation	1W

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

D.C. Characteristics: V_{CC} = +5V ± 5%, T_A=0°C to 70°C (Standard part); −40°C to +85°C (Industrial temp part)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{OL}	Output LOW Voltage			0.4	V	I_{OL}=3.2mA
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH}=−220μA
V_{IL}	Input LOW Voltage	−0.5		0.8	V	
V_{IH}	Input HIGH Voltage	2.0		V_{CC}	V	
I_{LI}	Input Leakage Current			10	μA	V_{IN}=0V to 5.25V
I_{LO}	Output Leakage Current			10	μA	V_O=0.4V to 5.25V Chip Deselected
I_{CC}	Power Supply Current			70	mA	

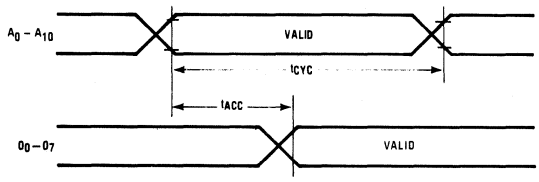
Capacitance: T_A=25°C, f=1.0MHz

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
C_{IN}	Input Capacitance			7	pF	V_{IN}=0V
C_{OUT}	Output Capacitance			10	pF	V_{OUT}=0V

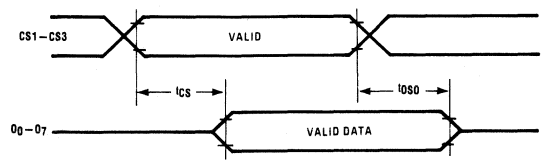
A.C. Characteristics: V_{CC} = +5V ± 5%, T_A=0°C to +70°C (Standard part); −40°C to +85°C (Industrial temp part)

Symbol	Parameter		Min.	Max.	Units	Conditions
t_{ACC}	Address Access Time	S6831B		450	ns	See Test Circuits And Waveforms
		S68A316		350	ns	
t_{CS}	Chip Select Access Time	S6831B		150	ns	
		S68A316		120	ns	
t_{OSO}	Chip Deselect Time	S6831B	0	150	ns	
		S68A316	0	120	ns	

Propagation Delay from Address Inputs



Propagation Delay From Chip Enable



A.C. Test Conditions

Input Pulse Levels	0.4V to 2.4V
Input Rise and Fall Times	≤20ns
Input Timing Level	1.5V
Output Timing Levels	0.8V and 2.0V
Output Load	1 TTL Gate and $C_L = 100pF$

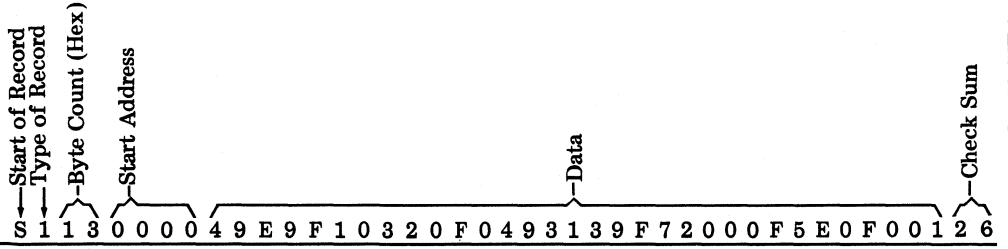
Custom Programming

The preferred method of pattern submission is the AMI Hex format as described below, with its built-in address space mapping and error checking. This is the format produced by the AMI Assembler. The format is as follows and may be on paper tape, punched cards or other media readable by AMI.

Position	Description
1	**Start of record (Letter S)**
2	**Type of record** 0 — Header record (comments) 1 — Data record 9 — End of file record
3, 4	**Byte Count** Since each data byte is represented as two hex characters, the byte count must be multiplied by two to get the number of characters to the end of the record. (This includes checksum and address data.) Records may be of any length defined in each record by the byte count.
5, 6, 7, 8	**Address Value** The memory location where the first data byte of this record is to be stored. Addresses should be in ascending order.
9, . . ., N	**Data** Each data byte is represented by two hex characters. Most significant character first.
N+1, N+2	**Checksum** The one's complement of the additive summation (without carry) of the data bytes, the address, and the byte count.

Example:

```
S 1 1 3 0 0 0 0 4 9 E 9 F 1 0 3 2 0 F 0 4 9 3 1 3 9 F 7 2 0 0 0 F 5 E 0 F 0 0 1 2 6
S 9 0 3 0 0 0 0 F C
```



NOTES:
1. Only positive logic formats for E_0, E_1, E_2 are accepted. 1 = V_{HIGH}; 0 = V_{LOW}
2. A "0" indicates the chip is enabled by a logic 0.
   A "1" indicates the chip is enabled by a logic 1.
3. Paper tape format is the same as the card format above except:
   a. The record should be a maximum of 80 characters.
   b. Carriage return and line feed after each record followed by another record.
   c. There should NOT be any extra line feed between records at all.
   d. After the last record, four (4) $$$$ (dollar) signs should be punched with carriage return and line feed indicating end of file.

AMERICAN MICROSYSTEMS, INC.

S68332/S68A332

32,768 BIT (4096x8) STATIC NMOS ROM

Features

- ☐ **Fast Access Time:**
  S68332: 450ns Maximum
  S68A332: 350ns Maximum
- ☐ **Fully Static Operation**
- ☐ **Single +5V ±5% Power Supply**
- ☐ **Directly TTL Compatible Inputs**
- ☐ **Three-State TTL Compatible Outputs**
- ☐ **Two Programmable Chip Selects**
- ☐ **EPROM Pin Compatible—2532**
- ☐ **Extended Temperature Range Available**

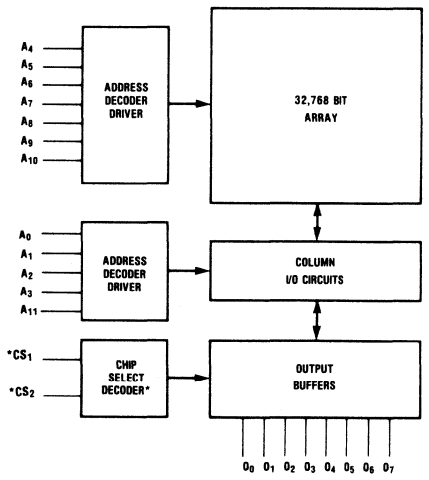
General Description

The AMI S68332 is a 32,768 bit static mask programmable NMOS ROM organized as 4096 words by 8 bits. The device is fully TTL compatible on all inputs and outputs and has a single +5V power supply. The three state outputs facilitate memory expansion by allowing the outputs to be OR-tied to other devices.

The S68332 is pin compatible with UV EPROMs making system development much easier and more cost effective. It is fully static, requiring no clocks for operation. The two chip selects are mask programmable, the active level for each being specified by the user.

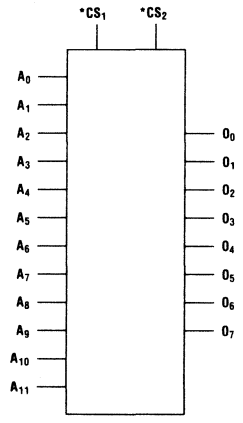
The S68332 is fabricated using AMI's N-Channel MOS technology. This permits the manufacture of very high density, high performance mask programmable ROMs.

Block Diagram

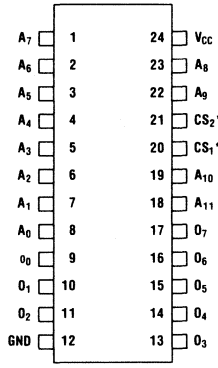


*PROGRAMMABLE CHIP SELECTS

Logic Symbol



Pin Configuration



Pin Names

$A_0 - A_{11}$	Address Inputs
$O_0 - O_7$	Data Outputs
$CS_1 - CS_2$	Chip Select Inputs
V_{CC}	+5V Power Supply

Absolute Maximum Ratings*

Ambient Temperature Under Bias—T_A (Standard Part)	0°C to +70°C
(Industrial temp part)	−40°C to +85°C
Storage Temperature	−65°C to 150°C
Output or Supply Voltages	−0.5V to 7V
Input Voltages	−0.5V to 7V
Power Dissipation	1W

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

D.C. Characteristics: V_{CC} = +5V ± 5%, T_A=0°C to 70°C (Standard part); −40°C to +85°C (Industrial temp part)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{OL}	Output LOW Voltage			0.4	V	I_{OL}=3.2mA
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH}=−220μA
V_{IL}	Input LOW Voltage	−0.5		0.8	V	
V_{IH}	Input HIGH Voltage	2.0		V_{CC}	V	
I_{LI}	Input Leakage Current			10	μA	V_{IN}=0V to 5.25V
I_{LO}	Output Leakage Current			10	μA	V_O=0.4V to 5.25V Chip Deselected
I_{CC}	Power Supply Current			70	mA	

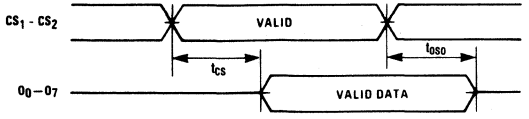
Capacitance: T_A=25°C, f=1.0MHz

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
C_{IN}	Input Capacitance			7	pF	V_{IN}=0V
C_{OUT}	Output Capacitance			10	pF	V_{OUT}=0V

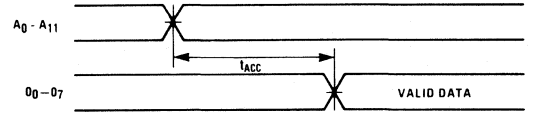
A.C. Characteristics: V_{CC} = +5V ± 5%, T_A=0°C to +70°C (Standard part); −40°C to +85°C (Industrial temp part)

Symbol	Parameter		Min.	Typ.	Max.	Units	Conditions
t_{ACC}	Address Access Time	S68332			450	ns	See A.C. Test Conditions and Waveforms
		S68A332			350	ns	
t_{CS}	Chip Select Access Time	S68332			150	ns	
		S68A332			150	ns	
t_{OSO}	Chip Deselect Time	S68332	0		150	ns	
		S68A332	0		150	ns	

Waveforms



Propagation From Chip Select



Propagation From Address

A.C. Test Conditions

Input Pulse Levels	0.4V to 2.4V
Input Rise and Fall Times	≤20ns
Input Timing Level	1.5V
Output Timing Levels	0.8V and 2.0V
Output Load	1 TTL Load and 100pF

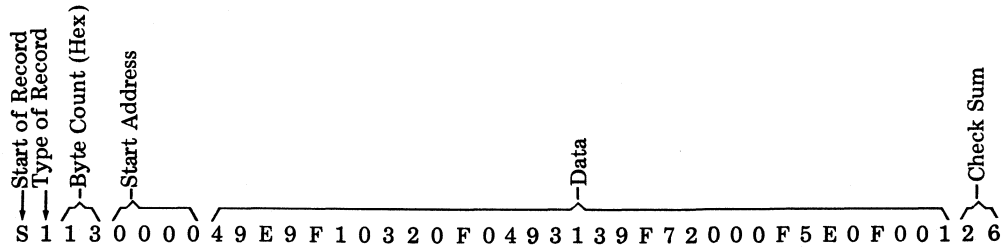
Custom Programming

The preferred method of pattern submission is the AMI Hex format as described below, with its built-in address space mapping and error checking. This is the format produced by the AMI Assembler. The format is as follows and may be on paper tape, punched cards or other media readable by AMI.

Position	Description
1	**Start of record (Letter S)**
2	**Type of record** 0 — Header record (comments) 1 — Data record 9 — End of file record
3, 4	**Byte Count** Since each data byte is represented as two hex characters, the byte count must be multiplied by two to get the number of characters to the end of the record. (This includes checksum and address data.) Records may be of any length defined in each record by the byte count.
5, 6, 7, 8	**Address Value** The memory location where the first data byte of this record is to be stored. Addresses should be in ascending order.
9, . . ., N	**Data** Each data byte is represented by two hex characters. Most significant character first.
N+1, N+2	**Checksum** The one's complement of the additive summation (without carry) of the data bytes, the address, and the byte count.

Example:

```
S 1 1 3 0 0 0 0 4 9 E 9 F 1 0 3 2 0 F 0 4 9 3 1 3 9 F 7 2 0 0 0 F 5 E 0 F 0 0 1 2 6
S 9 0 3 0 0 0 0 F C
```

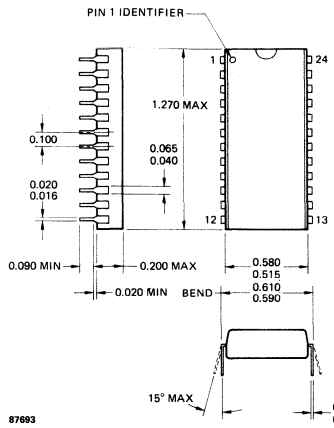


NOTES:

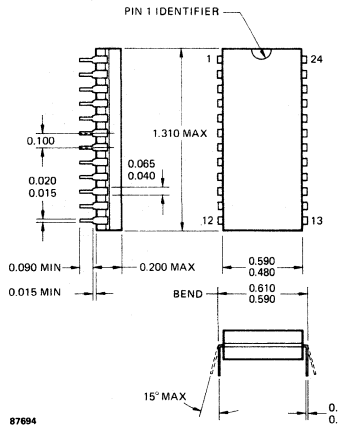
1. Only positive logic formats for CS_1 and CS_2 are accepted. 1 = V_{HIGH}; 0 = V_{LOW}
2. A "0" indicates the chip is enabled by a logic 0.
   A "1" indicates the chip is enabled by a logic 1.
3. Paper tape format is the same as the card format above except:
   a. The record should be a maximum of 80 characters.
   b. Carriage return and line feed after each record followed by another record.
   c. There should NOT be any extra line feed between records at all.
   d. After the last record, four (4) $$$$ (dollar) signs should be punched with carriage return and line feed indicating end of file.

Package Outlines

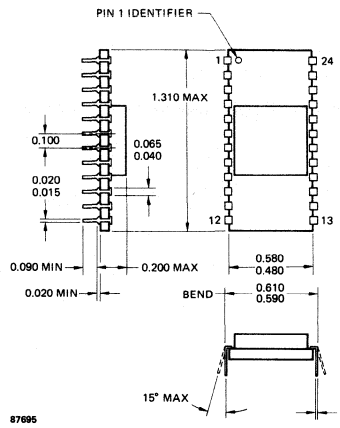
24-Pin Plastic



24-Pin Cer-DIP



24-Pin Ceramic



ROMs

AMERICAN MICROSYSTEMS, INC.

PRELIMINARY

S2333

32,768 BIT (4096x8) STATIC NMOS ROM

Features

- ☐ Fast Access Time: 350ns Maximum
- ☐ Fully Static Operation
- ☐ Single +5V ±5% Power Supply
- ☐ Directly TTL Compatible Inputs
- ☐ Three-State TTL Compatible Outputs
- ☐ Two Programmable Chip Selects
- ☐ EPROM Pin Compatible (2732)
- ☐ Extended Temperature Range Available

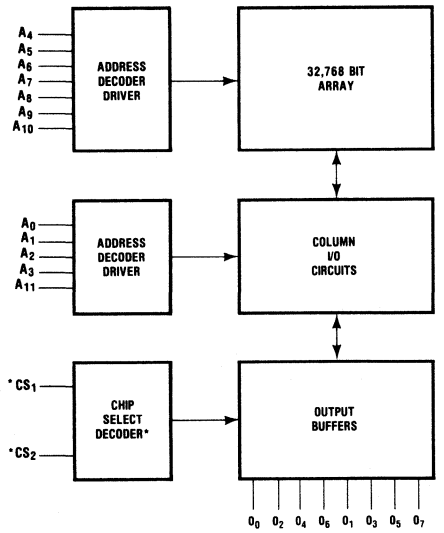
General Description

The AMI S2333 is a 32,768 bit static mask programmable NMOS ROM organized as 4096 words by 8 bits. The device is fully TTL compatible on all inputs and outputs and has a single +5V power supply. The three state outputs facilitate memory expansion by allowing the outputs to be OR-tied to other devices.

The S2333 is pin compatible with UV EPROMs making system development much easier and more cost effective. The fully static S2333 requires no clocks for operation. The two chip selects are mask programmable with the active level for each being specified by the user.

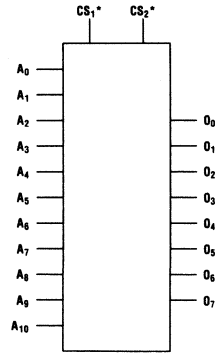
The S2333 is fabricated using AMI's N-Channel MOS technology. This permits the manufacture of very high density, high performance mask programmable ROMs.

Block Diagram

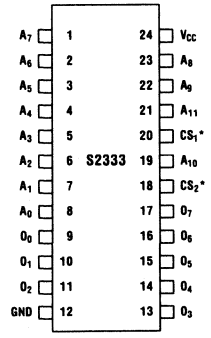


*User Defined As Active High (CS), Active Low ($\overline{CS}$) or NC (No Connection)

Logic Symbol



Pin Configuration



Pin Names

$A_0 - A_{11}$	Address Inputs
$O_0 - O_7$	Data Outputs
$CS_1 - CS_2$	Chip Select Inputs
V_{CC}	+5V Power Supply

Absolute Maximum Ratings*

Ambient Temperature Under Bias—T_A (Standard Part)	0°C to +70°C
(Industrial temp part)	−40°C to +85°C
Storage Temperature	−65°C to 150°C
Output or Supply Voltages	−0.5V to 7V
Input Voltages	−0.5V to 7V
Power Dissipation	1W

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

D.C. Characteristics: V_{CC} = +5V ± 5%, T_A=0°C to 70°C (Standard part); −40°C to +85°C (Industrial temp part)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{OL}	Output LOW Voltage			0.4	V	I_{OL}=3.2mA
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH}=−220μA
V_{IL}	Input LOW Voltage	−0.5		0.8	V	
V_{IH}	Input HIGH Voltage	2.0		V_{CC}	V	
I_{LI}	Input Leakage Current			10	μA	V_{IN}=0V to 5.25V
I_{LO}	Output Leakage Current			10	μA	V_O=0.4V to 5.25V Chip Deselected
I_{CC}	Power Supply Current			70	mA	V_{CC}=5.25V, T_A=0°C

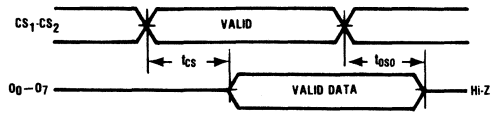
Capacitance: T_A=25°C, f=1.0MHz

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
C_{IN}	Input Capacitance			7	pF	V_{IN}=0V
C_{OUT}	Output Capacitance			10	pF	V_{OUT}=0V

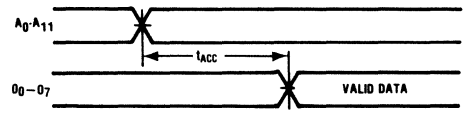
A.C. Characteristics: V_{CC} = +5V ± 5%, T_A=0°C to 70°C (Standard part); −40°C to +85°C (Industrial temp part)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
t_{ACC}	Address Access Time			350	ns	See A.C. Test
t_{CS}	Chip Select Access Time			120	ns	Conditions and
t_{OSO}	Chip Deselect Time	0		120	ns	Waveform

Waveforms



Propagation From Chip Select



Propagation From Address

ROMs

A.C. Test Conditions

Input Pulse Levels	0.4V to 2.4V
Input Rise and Fall Times	≤20ns
Input Timing Level	1.5V
Output Timing Levels	0.8V and 2.0V
Output Load	1 TTL Load and 100pF

ROM Code Data

AMI's preferred method of receiving ROM CODE DATA is in EPROM. Two EPROMs should be submitted. One is programmed to the desired code and the other is blank. AMI will read the programmed EPROM, transfer this data to disk and then program the blank EPROM from the stored information. This procedure guarantees that the EPROM has been properly entered into the AMI computer system. The AMI programmed EPROM is returned to the customer for verification of the ROM program. Unless otherwise requested AMI will not proceed until the customer verifies the program in the returned EPROM.

EPROM Requirements

The following EPROMs should be used for submitted ROM Code Data:

PREFERRED 1-2732; Optional 2-2716

If two EPROMs are used to specify one ROM pattern, two blank EPROMs must be submitted. In this instance, the programmed EPROMs must clearly state which of the two EPROMs is for lower and upper address locations in the ROW. The preferred method is to mark the EPROM with the ROM address (in Hex) where the EPROM data is to be located.

Pattern Data from ROMS

If a customer has ROMs produced by another supplier, these ROMs can be submitted for ROM pattern data instead of EPROMs. Obviously, these ROMs must be pin compatible with the AMI device. The programmable chip selects must be defined. (NOTE: In some cases a competitors ROM may have a chip select or enable that is not customer defined. However, if this pin is customer defined for the AMI ROM, the required active logic level for this input must be specified.)

Optional Method of Supply ROM Data*

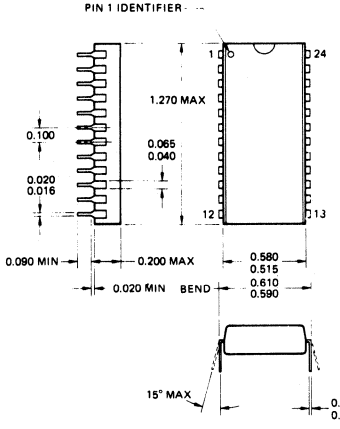
If an EPROM or ROM cannot be supplied the following, other methods are acceptable.

- ☐ 9 Track NRZ Magnetic Tape
- ☐ Paper Tape
- ☐ Card Deck

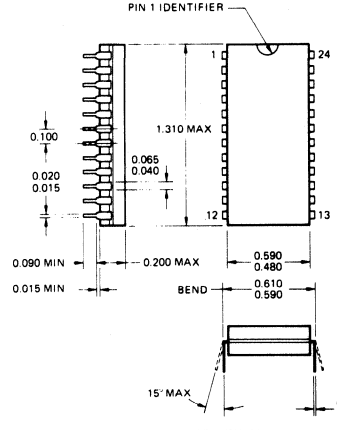
* *Consult AMI sales office for format.*

Package Outlines

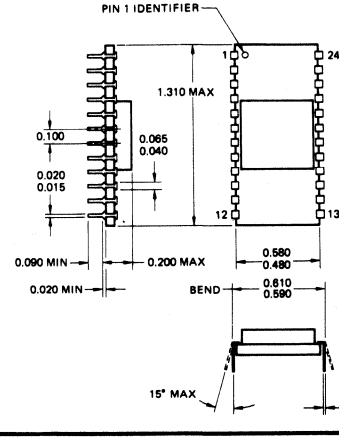
24-Pin Plastic



24-Pin Cer-DIP



24-Pin Ceramic



AMERICAN MICROSYSTEMS, INC.

PRELIMINARY

S68A364

65,536 BIT (8192x8) STATIC NMOS ROM

Features

- ☐ **Fast Access Time: 350ns Maximum**
- ☐ **Low Standby Power 55mW Maximum**
- ☐ **Fully Static Operation**
- ☐ **Single +5V ±10% Power Supply**
- ☐ **Directly TTL Compatible Inputs**
- ☐ **Three-State TTL Compatible Outputs**
- ☐ **Programmable Chip Enable**
- ☐ **Extended Temperature Range Available**

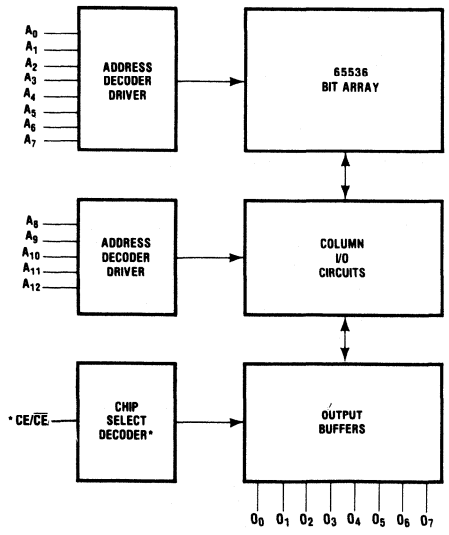
General Description

The AMI S68A364 is a 65,536 bit static mask programmable NMOS ROM organized as 8192 words by 8 bits. The device is fully TTL compatible on all inputs and outputs and has a single +5V power supply. The three state outputs facilitate memory expansion by allowing the outputs to be OR-tied to other devices.

The fully static S68A364 requires no clocks for operation. The chip enable is mask programmable with the active level being specified by the user. When not enabled, power supply current is reduced to a maximum of 10mA.

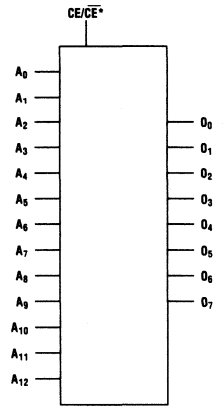
The S68A364 is fabricated using AMI's N-Channel MOS technology. This permits the manufacture of very high density, high performance mask programmable ROMs.

Block Diagram

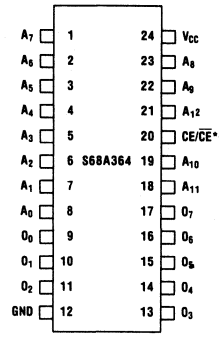


* USER DEFINED AS ACTIVE HIGH (CE); ACTIVE LOW ($\overline{CE}$).

Logic Symbol



Pin Configuration



Pin Names

$A_0 - A_{11}$	Address Inputs
$O_0 - O_7$	Data Outputs
$CE/\overline{CE}$	Programmable Chip Enable
V_{CC}	+5V Power Supply

ROMs

Absolute Maximum Ratings*

Ambient Temperature Under Bias—T_A (Standard Part)	0°C to +70°C
(Industrial temp part)	−40°C to +85°C
Storage Temperature	−65°C to 150°C
Output or Supply Voltages	−0.5V to 7V
Input Voltages	−0.5V to 7V
Power Dissipation	1W

**COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.*

D.C. Characteristics:

$V_{CC} = +5V \pm 10\%$, $T_A = 0°C$ to 70°C (Standard part); −40°C to +85°C (Industrial temp part)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{OL}	Output LOW Voltage			0.4	V	$I_{OL} = 3.2mA$
V_{OH}	Output HIGH Voltage	2.4			V	$I_{OH} = -220\mu A$
V_{IL}	Input LOW Voltage	−0.5		0.8	V	
V_{IH}	Input HIGH Voltage	2.0		$V_{CC}+0.5$	V	
I_{LI}	Input Leakage Current			10	μA	$V_{IN} = 0V$ to V_{CC}
I_{LO}	Output Leakage Current			10	μA	$V_O = 0.4V$ to V_{CC} Chip Deselected
I_{CC}	Power Supply Current—Active			70	mA	$V_{CC} = 5.50V$, $T_A = 0°C$
I_{SB}	Power Supply Current Active —Standby			10	mA	Chip Deselected (Note 1)

Capacitance: $T_A = 25°C$, f = 1.0MHz

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
C_{IN}	Input Capacitance			7	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance			10	pF	$V_{OUT} = 0V$

A.C. Characteristics:

$V_{CC} = +5V \pm 10\%$, $T_A = 0°C$ to +70°C (Standard part); −40°C to +85°C (Industrial temp part)

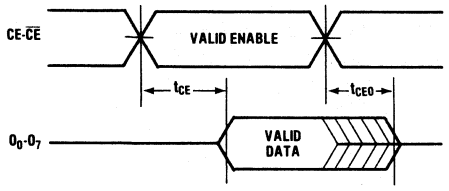
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
t_{ACC}	Address Access Time			350	ns	See A.C. Test
t_{CE}	Chip Enable Access Time (Note 1)			350	ns	Conditions and
t_{CEO}	Disable Time From Chip Enable (Note 1)			200	ns	Waveforms

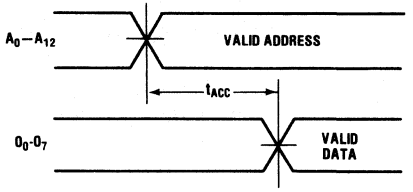
Note 1—Pin 20 must be defined by the user as CE, $\overline{CE}$. Defining pin 20 as CE(1) or $\overline{CE}$(0) provides a low power standby mode.

A.C. Test Conditions

Input Pulse Levels	0.8V to 2.0V
Input Rise and Fall Times	⩽20ns
Input Timing Level	1.5V
Output Timing Levels	0.4V and 2.4V
Output Load	1 TTL Load and 100pF

Waveforms





AMERICAN MICROSYSTEMS, INC.

PRELIMINARY

S2364

65,536 BIT (8192x8) STATIC NMOS ROM

Features

- ☐ Fast Access Time: 350ns Maximum
- ☐ Low Standby Power 55mW Maximum
- ☐ Fully Static Operation
- ☐ Single +5V ±10% Power Supply
- ☐ Directly TTL Compatible Inputs
- ☐ Three-State TTL Compatible Outputs
- ☐ Three Programmable Chip Enables
- ☐ EPROM Pin Compatible (2764)
- ☐ Extended Temperature Range Available

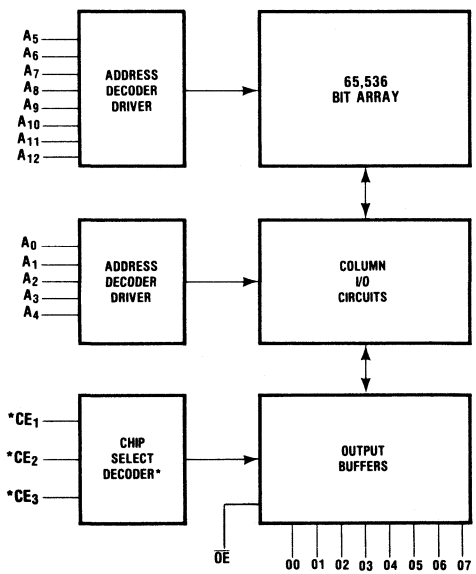
General Description

The AMI S2364 is a 65,536 bit static mask programmable NMOS ROM organized as 8192 words by 8 bits. The device is fully TTL compatible on all inputs and outputs and has a single +5V power supply. The three state outputs facilitate memory expansion by allowing the outputs to be OR-tied to other devices.

The S2364 is pin compatible with the 2764 UV EPROM making system development much easier and more cost effective. The fully static S2364 requires no clocks for operation. The three chip enables are mask programmable, with the active level for each being specified by the user. When not enabled, power supply current is reduced to a 10mA maximum.

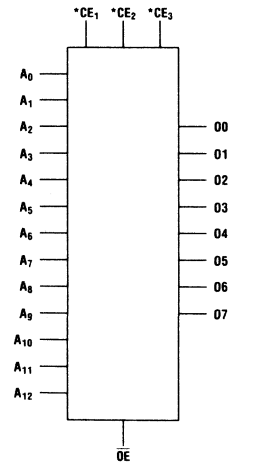
The S2364 is fabricated using AMI's N-Channel MOS technology. This permits the manufacture of very high density, high performance mask programmable ROMs.

Block Diagram

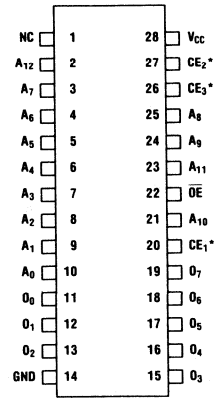


*USER DEFINED MASK PROGRAMMABLE CHIP ENABLE – MAY BE DEFINED AS ACTIVE HIGH, ACTIVE LOW, OR NO CONNECT.

Logic Symbol



Pin Configuration



Pin Names

$A_0 - A_{12}$	Address Inputs
$O_1 - O_7$	Data Outputs
$\overline{CE}_2, \overline{CE}_1, CE_2$	Chip Enables (User Defined)
$\overline{OE}$	Output Enable
V_{CC};GND;NC	5V;Ground;No Connect

Absolute Maximum Ratings*

Ambient Temperature Under Bias—T_A (Standard Part)	0°C to +70°C
(Industrial temp part)	−40°C to +85°C
Storage Temperature	−65°C to 150°C
Output or Supply Voltages	−0.5V to 7V
Input Voltages	−0.5V to 7V
Power Dissipation	1W

COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

D.C. Characteristics: $V_{CC} = +5V \pm 10\%$, $T_A = 0°C$ to 70°C (Standard part); −40°C to +85°C (Industrial temp part)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{OL}	Output LOW Voltage			0.4	V	$I_{OL} = 3.2mA$
V_{OH}	Output HIGH Voltage	2.4			V	$I_{OH} = -220\mu A$
V_{IL}	Input LOW Voltage	−0.5		0.8	V	
V_{IH}	Input HIGH Voltage	2.0		V_{CC}	V	
I_{LI}	Input Leakage Current			10	μA	$V_{IN} = 0V$ to 5.50V
I_{LO}	Output Leakage Current			10	μA	$V_O = 0.4V$ to 5.50V Chip Deselected
I_{CC}	Power Supply Current—Active			70	mA	Chip Enabled
I_{SB}	Power Supply Current—Standby			10	mA	Chip Disabled

Capacitance: $T_A = 25°C$, $f = 1.0MHz$

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
C_{IN}	Input Capacitance			7	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance			10	pF	$V_{OUT} = 0V$

A.C. Characteristics: $V_{CC} = +5V \pm 10\%$, $T_A = 0°C$ to +70°C (Standard part); −40°C to +85°C (Industrial temp part)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
t_{ACC}	Address Access Time			350	ns	See A.C.
t_{CE}	Chip Enable Access Time			350	ns	Test Conditions
t_{OE}	Output Enable Access Time			100	ns	and
t_{CEO}	Disable Time From Chip Enable			200	ns	Waveforms
t_{OEO}	Disable Time From $\overline{OE}$			100	ns	

ROMs

Truth Table: CE_2, CE_1, CE_0 Are User Defined; Chip Is Enabled When CE_2, CE_1 & CE_0 Inputs Match The User Defined Logic States.

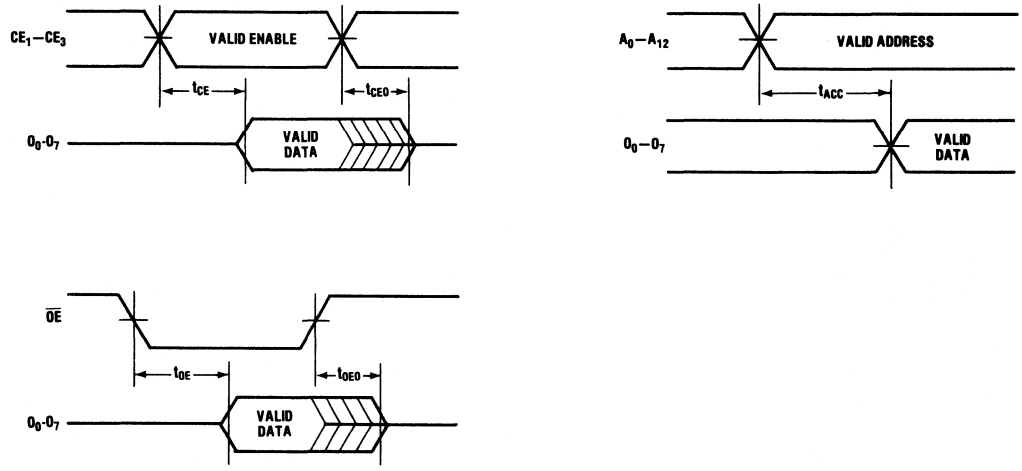
CE_3	CE_2	CE_1	$\overline{OE}$	Outputs	Power
$\overline{CE_3}$	X	X	X	Hi-Z	Stby
X	$\overline{CE_2}$	X	X	Hi-Z	Stby
X	X	$\overline{CE_1}$	X	Hi-Z	Stby
CE_3	CE_2	CE_1	H	Hi-Z	Active
CE_3	CE_2	CE_1	L	Data Out	Active

X=Don't Care Condition

A.C. Test Conditions

Input Pulse Levels	0.8V to 2.0V
Input Rise and Fall Times	⩽20ns
Input Timing Level	1.5V
Output Timing Levels	0.4V and 2.4V
Output Load	1 TTL Load and 100pF

Waveforms



AMERICAN MICROSYSTEMS, INC.

ADVANCED PRODUCT DESCRIPTION
S23128

131,072 BIT (16384x8) STATIC NMOS ROM

Features

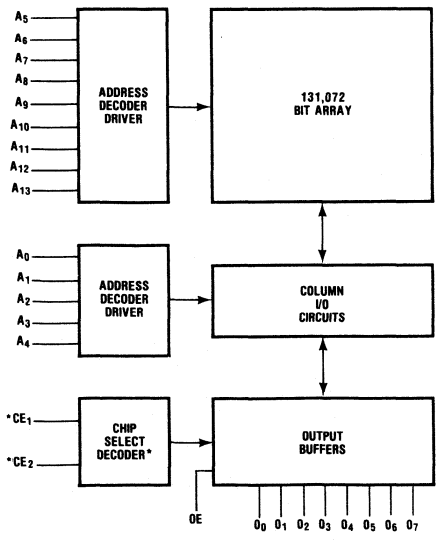
- ☐ Fast Access Time: 250ns max.
- ☐ Low Standby Power: 55mW max.
- ☐ Fully Static Operation
- ☐ Single +5V ± 10% Power Supply
- ☐ Directly TTL Compatible Outputs
- ☐ 2 Programmable Chip Enables
- ☐ EPROM Pin Compatible (2764)

General Description

The AMI S23128 is a 131,072 bit static mask programmable NMOS RAM organized as 16,384 words by 8 bits. The device is fully TTL compatible on all inputs and outputs and has a single +5V power supply. The three state outputs facilitate memory expansion by allowing the outputs to be OR-tied to other devices.

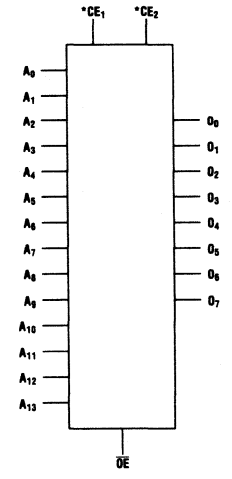
The S23128 is pin compatible with the 2764 EPROM making system development easier and more cost effective. The fully static S23128 requires no clocks for operation. The two chip enables are mask programmable with the active level for each being specified by the user. When not enabled, power supply current is reduced to 10mA max. The S23128 is fabricated using AMI's N-Channel MOS technology. This permits the manufacture of very high density, high performance mask programmable ROMs.

Block Diagram

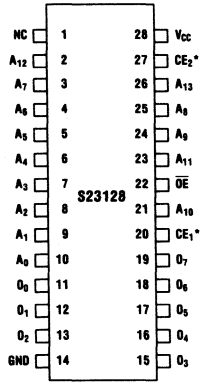


*USER DEFINED MASK PROGRAMMABLE CHIP ENABLE - MAY BE DEFINED AS 1, 0, OR NO CONNECT

Logic Symbol



Pin Configuration



Pin Names

A_0-A_{13}	Address Inputs
O_0-O_7	Data Outputs
$\overline{CE_1}$, CE_2	Chip Enables (User Defined)
$\overline{OE}$	Output Enable
V_{CC};GND;NC	5V;Ground; No Connect

ROMs

AMERICAN MICROSYSTEMS, INC.

ADVANCED PRODUCT DESCRIPTION

UNCOMMITTED LOGIC ARRAYS

Features

- ☐ **Arrays of Uncommitted CMOS Transistors Programmed by Metal Layer Interconnect to Implement Arbitrary Digital Logic Functions**
- ☐ **Multiple Developmental Interfaces: AMI or Customer Designed**
- ☐ **Six Array Configurations—From 300 to 1260 Gates**
- ☐ **Quick Turn Prototypes and Short Production Turn-On Time**
- ☐ **Economical Semi-Custom Approach for Low-to-Medium Production Volume Requirements**
- ☐ **Advanced Oxide-Isolated Silicon Gate CMOS Technology**
- ☐ **High Performance—5 to 10 ns Typical Gate Delay**
- ☐ **Broad Power Supply Range—3V to 10V (±10%)**
- ☐ **TTL or CMOS Compatible I/O**
- ☐ **Up to 76 I/O Connections**
- ☐ **Numerous Package Options**
- ☐ **Full Military Temperature Range (−55°C to 125°C) and MIL-STD-883 Class B Screening Available**

General Description

AMI's Uncommitted Logic Array (ULA) products consist of arrays of CMOS devices whose interconnections are initially unspecified. By "programming" interconnect at the metal layer mask level, virtually arbitrary configurations of digital logic can be realized in an LSI implementation.

AMI ULA designs are based on topological cells—i.e., groups of uncommitted silicon-gate N-channel and P-channel transistors—that are placed at regular intervals along the X and Y axes of the chip with intervening polysilicon underpasses. Pads, input protection circuitry, and uncommitted output drivers are placed around the periphery.

A family of CMOS ULA products is offered in six configurations, summarized in Table 1, with circuit complexities equivalent to 300, 400, 540, 770, 1000, and 1260 two-input gates, respectively. All pads (except the two preassigned power supply connections) can be individually configured as inputs, outputs, or I/O's. Input switching characteristics can be programmed for either CMOS or TTL compatibility. LS buffer output drivers will support CMOS levels or two low power schottky TTL loads. TTL buffer outputs will also provide CMOS levels and are capable of driving up to six LS TTL loads. All output drivers can be programmed for tri-state or open drain (open collector) operation as required. One input-only pad is also provided.

Table 1

Circuit	Equivalent Two-Input Gates	Pads	LS Output Drivers	TTL Output Drivers	Input Only
UA-1	300	40	17	20	1
UA-2	400	46	23	20	1
UA-3	540	52	25	24	1
UA-4	770	62	31	28	1
UA-5	1000	70	35	32	1
UA-6	1260	78	39	36	1

Pinout or lead count varies with die size and array complexity as shown in Table 1. The arrays are offered in standard plastic and ceramic dual-in-line packages with pin counts ranging from 16 to 64, and in JEDEC-Standard leadless chip carriers. AMI ULA products are also available in wafer or unpackaged die form.

The CMOS technology used for these products is AMI's state-of-the-art 5-micron, oxide-isolated, silicon gate CMOS process. This process offers all the conventional advantages of CMOS—i.e., very low power consumption, broad power supply voltage range (3V to 10V ±10%), and high noise immunity—as well as dense circuits with high performance. Gate propagation delays are in the five to ten ns range for 5 volt operation at room temperature. AMI ULA products can be supplied in versions intended for operation over the standard commercial temperature range (0°C to +70°C), the industrial range (−40°C to +85°C), or the full military range (−55°C to +125°C). MIL-STD-883 Class B screening, including internal visual inspection and high temperature burn-in, is offered. Similarly, customer-specified high reliability screening is available for commercial and industrial applications.

Compared to SSI/MSI logic implementations, AMI's ULA approach offers lower system cost and, in addition, all the benefits of CMOS LSI. The lower system cost is due to significant reductions in component count, board area and power consumption. Product reliability, a strong function of component count, is thereby greatly enhanced. And compared to fully custom LSI circuits, the ULA offers several advantages: low development cost; shorter development time; shorter production turn-on time; and low unit costs for small to moderate production volumes.

In conjunction with these arrays, AMI has developed a set of "functional overlays." These are basic logic element building blocks—e.g. two input and larger gates of various types, flip-flops, and so forth—from which complete logic designs can be developed. Each functional overlay corresponds to a metal interconnect pattern that is superimposed on a set of uncommitted transistors (and polysilicon underpasses) in the array to implement the logic element. Typical functional overlay logic elements and the number of two-input gate equivalents they utilize are shown in Table 2.

AMI will convert customer designed logic to metal interconnect patterns using functional overlays and its proprietary Symbolic Interactive Design System (SIDS). SIDS is a computer aided design tool for layout using on-line color graphics terminals. Interested customers should submit logic diagrams for evaluation and a quotation.

For programs involving multiple ULA patterns from customers with suitable MOS design and layout experience, AMI will also support arrangements in which the customer designs the ULA metal interconnect patterns and furnishes AMI with corresponding metal mask PG tapes to AMI specification.

Table 2

Logic Element	2-Input Gate Equivalent
2-Input NOR	1
2-Input NAND	1
3-Input NOR	1.5
3-Input NAND	1.5
INVERTER	.5
D FLIP-FLOP W/RESET	5
D FLIP-FLOP W/SET-RESET	6
J-K FLIP-FLOP	8
CLOCKED LATCH	2.5
EXCLUSIVE OR	2.5
SCHMITT TRIGGER	2
4-BIT BCD CNTR W/RESET	27
TRANSMISSION GATE	.5

DC Characteristics—TTL Interface

Specified @ $V_{DD}=+5V \pm 10\%$; $V_{SS}=0$; Temperature $=-55°C$ to $+125°C$

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage	2.0		V_{DD}	V
V_{IL}	Input Low Voltage	0.0		0.8	V
V_{OH}	Output High Voltage (LS Buffer $I_{OH}=-700\mu A$) (T Buffer $I_{OH}=-1.5mA$)	2.7 2.4			V V
V_{OL}	Output Low Voltage (T Buffer $V_{OL}=2.4mA$) (LS Buffer $I_{OL}=0.8mA$)			0.4 0.4	V V
I_{OZ}	3-State Output Leakage $V_O=0$ or V_{DD}	−10	0.001	10	μA

DC Characteristics—CMOS Interface

Sym.	Parameter	V_{DD}	Limits *T Low Min	*T Low Max	25°C Min	25°C Typ	25°C Max	*T High Min	*T High Max	Units	Condition
I_{DD}	Quiescent Device Current	5V 10V		0.1 0.2		.001 .002	0.1 0.2		1 2	μA/gate μA/gate	$V_{IN}=0$ or V_{DD}
V_{OL}	Low Level Output Voltage			0.05			0.05		0.05	V	$I_O=1\mu A$
V_{OH}	High Level Output Voltage	5V 10V	4.95 9.95		4.95 9.95			4.95 9.95		V V	$I_O=-1\mu A$
V_{IL}	Input Low Voltage	5V 10V	0.0 0.0	1.5 3.0	0.0 0.0		1.5 3.0	0.0 0.0	1.5 3.0	V V	
V_{IH}	Input High Voltage	5V 10V	3.5 7.0	5.0 10.0	3.5 7.0		5.0 10.0	3.5 7.0	5.0 10.0	V V	
I_{OL}	Output Low (Sink) Current T Buffer LS Buffer	5V 10V 5V 10V	3.2 6.0 1.0 1.8		3.2 6.0 1.0 1.8	4.8 9.0 1.6 3.1		2.4 4.0 0.8 1.0		mA mA mA mA	$V_O=0.4V$ $V_O=0.5V$ $V_O=0.4V$ $V_O=0.5V$
I_{OH}	Output High (Source) Current T Buffer LS Buffer	5V 10V 5V 10V		−600 −1120 −300 −560			−600 −1120 −300 −560		−500 −940 −250 −470	μA μA μA μA	$V_O=4.6V$ $V_O=9.5V$ $V_O=4.6V$ $V_O=9.5V$
I_{IN}	Input Leakage Current			1			1		1	μA	$V_{IN}=0$ or V_{DD}
I_{OZ}	3 State Output Leakage Current			±1			±1		±10	μA	$V_O=0$ or V_{DD}
C_I	Input Capacitance					5				pF	Any Input

*Military temperature range is −55°C to +125°C
Industrial temperature range is −40°C to +85°C
Commercial temperature range is 0°C to +70°C

AMERICAN MICROSYSTEMS, INC.

Application Note Summary

Communications Products

S2559 Digital Tone Generator **70T01**

Describes design considerations, test methods, and results obtained using the S2559 Tone Generator family in DTMF pushbutton telephones. Interface with type 500 and 2500 networks are discussed. Use in ancillary equipment is also covered.

Using the S3525 DTMF Bandsplit Filter **80T04**

Describes interfacing with three different decoder chips to build compact 2-chip DTMF receivers. Also covers various applications in remote control, radio, etc.

Consumer Products

Useful Noise **79C01**

The S2688 Noise Generator is useful in many applications where digital noise is required for audio effects.

Programming the S8890 Rhythm Generator **79C02**

Explains the program format and how to submit data for ROM programming.

MOS Music **79C05**

MOS Music is a primer on the application of standard MOS/LSI circuits in creating electronic music. This note discusses the key elements of music production in an electronic organ.

Real Remote Control **79C06**

A remote control system using the S2742 and S2743 with infrared transmission is shown. A simple but effective alignment technique is demonstrated which will ensure successful operation.

S2000 Family

Extended Memory **792K01**

This note describes the necessary circuitry needed to extend the program memory (ROM) beyond an S2000/S2150's normal amount.

Musical Application for an S2000 Microcomputer **792K02**

This note describes some theory and the application of a microcomputer to generate musical notes. Applications might include electronic games, alarm clock, door bells and telephones.

Repertory Dialers/Feature Phones Using S2000/S2150 ..... **792K05**

This note describes how an S2000/S2150 can be used in a repertory dialer circuit and how to communicate with external RAM.

S2000 Software TouchControl Keyboard Scan and Display Output **792K06**

This note describes programs for typical display output with delay and a keyboard scan and debounce. This program will handle eight digits and up to 32 keys.

S2000 Software Seconds Timing and Display **792K07**

This note describes several useful software timing/display routines and the associated hardware.

Analog-to-Digital Conversion Using the S2000 Family **792K10**

This note describes several A/D schemes using the S2000 family, e.g., from a simple single slope integration method with an S2000 to a complex scheme using the S2200's on-chip A/D converter.

S2000 Family Technical Articles **792K11**

This brochure contains several reprints of articles on S2000 family members.

Programmable Appliance/Outlet Controller Using the S2000/S2150 ..... **792K14**

This note describes an intelligent programmable appliance/outlet controller.

S2000 Software Routines-Keyboard Entry, LED Display, Software Timing and Sound Generation **802K16**

This note describes several general purpose programs listed in title.

S2000/S2150 Single-Chip Microcomputer Positive BCD Integer Arithmetic Routines **802K17**

This note describes additon, subtraction, multiplication and division routines for the S2000 Family Microcomputer.

S6800 Family

S68047 Video Display Generator **796801**

Describes a low cost link between an MPU and a standard black and white or color television set

A Minimal S6802/S6846 System Design **796802**

Details how to make an S6802/S6846 version of the EVK in a minimal systems application.

Microprocessor Crystal Specification **796803**

Aids the MPU system designer in specifying and ordering the crystal required for the S6802 microprocessor.

S68488 General Purpose Interface Adapter **806805**

Describes basic design information needed in using the S68488 GPIA.

S68045 Compared with Motorola MC 6845 ..... **806806**

Describes the fundamental differences between the two devices.

S9900 Family

S9900 Simplifies Design of Bi-Directional I/O Module **799901**

Illustrates use of the CPU. The design can be used for simple TTL logic tester. (Reprint from *Electronics)*

Minimum Systems Design with the S9900 16-Bit Microprocessor **799902**

This design uses just the CPU, a 1K ROM, a 2K RAM, a clock and six smaller IC's.

Controlled Dot Matrix Printer—S9900

Shows how to control a 7040 series dot matrix printer.

S9900 Technical Article Reprints **799904**

A compilation of 6 technical articles covering: a comparison of the 9900, Z8000 and 8086; an 8-page description of the 9900; a real-time control software design using the 9900; a multiprocessor system design using the 9900; the bi-directional I/O module identical to the above application note; using the 9940 to implement the NBS data encryption standard.

At AMI we are continually searching for more effective methods of providing protection for MOS devices. Present configurations of protective devices are the result of years of research and review of field problems.

In the normal course of producing integrated circuits however, there occasionally occur variations in oxide thickness which may allow a condition where gate oxide breakdown voltage is less than the protective device breakdown. Although the oxide breakdown voltage may still be far beyond normal voltage levels encountered in operation, excessive voltages may cause permanent damage. Even though AMI has evolved the best designed protective device possible, we recognize that it is not 100% effective.

A large number of failed returns have been due to misapplication of biases. In particular, forward bias conditions cause excessive current through the protective devices, which in turn will vaporize metal lines to the inputs. *Careful inspection of the device data sheets and proper pin designation should help reduce this failure mode.*

Gate ruptures caused by static discharge also account for a large percentage of device failures in customers' manufacturing areas. *Precautions should be taken to minimize the possibility of static charges occurring during handling and assembly of MOS circuits.*

To assist our customers in reducing the hazards which may be detrimental to MOS circuits, the following guidelines for handling MOS are offered. *The precautions listed here are used at AMI.*

1. All benches used for assembly or test of MOS circuits are covered with conductive sheets. *WARNING*: Never expose an operator directly to a hard electrical ground. For safety reasons, the operator must have a resistance of at least 100K Ohms between himself and hard electrical ground.
2. All entrances to work areas have grounding plates on door and/or floor, which must be contacted by people entering the area.
3. Conductive straps are worn inside and outside of employees' shoes so that body charges are grounded when entering work area.
4. Anti-static neutralized smocks are worn to eliminate the possibility of static charges being generated by friction of normal wear. Two types are available; Dupont anti-static nylon and Dupont neutralized 65% polyester/35% cotton.
5. Cotton gloves are worn while handling parts. Nylon gloves and rubber finger cots are not allowed.
6. Humidity is controlled at a minimum of 35% to help reduce generation of static voltages.
7. All parts are transported in conductive trays. Use of plastic containers is forbidden. Axial leaded parts are stored in conductive foam, such as Velofoam#7611.
8. All equipment used in the assembly area must be thoroughly grounded. Attention should be given to equipment that may be inductively coupled and generate stray voltages. Soldering irons must have grounded tips. Grounding must also be provided for solder posts, reflow soldering equipment, etc.
9. During assembly of I.C.'s to printed circuit boards, it is advisable to place a grounding clip across the fingers of the board to ground all leads and lines on the board.
10. Use of carpets should be discouraged in work areas, but in other areas may be treated with anit-static solution to reduce static generation.
11. MOS parts should be handled on conductive surfaces and the handler must touch the conductive surface *before* touching the parts.
12. In addition, no power should be applied to the socket or board while the MOS device is being inserted. This permits any static charge accumulated on the MOS device to be safely removed before power is applied.
13. MOS devices should not be handled by their leads unless absolutely necessary. If possible, MOS devices should be handled by their packages as opposed to their leads.
14. In general, materials prone to static charge accumulation should not come in contact with MOS devices.

These precautions should be observed even when an MOS device is suspected of being defective. The true cause of failure cannot be accurately determined if the device is damaged due to static charge build-up.

It should be remembered that even the most elaborate physical prevention techniques will not eliminate device failure if personnel are not fully trained in the proper handling of MOS.

This is a most important point and should not be overlooked.

More information can be obtained by contacting the Product Assurance Department.

American Microsystems, Inc.
3800 Homestead Road
Santa Clara, California 95051
Telephone (408) 246-0330
TWX 910-338-0024 or 910-338-0018

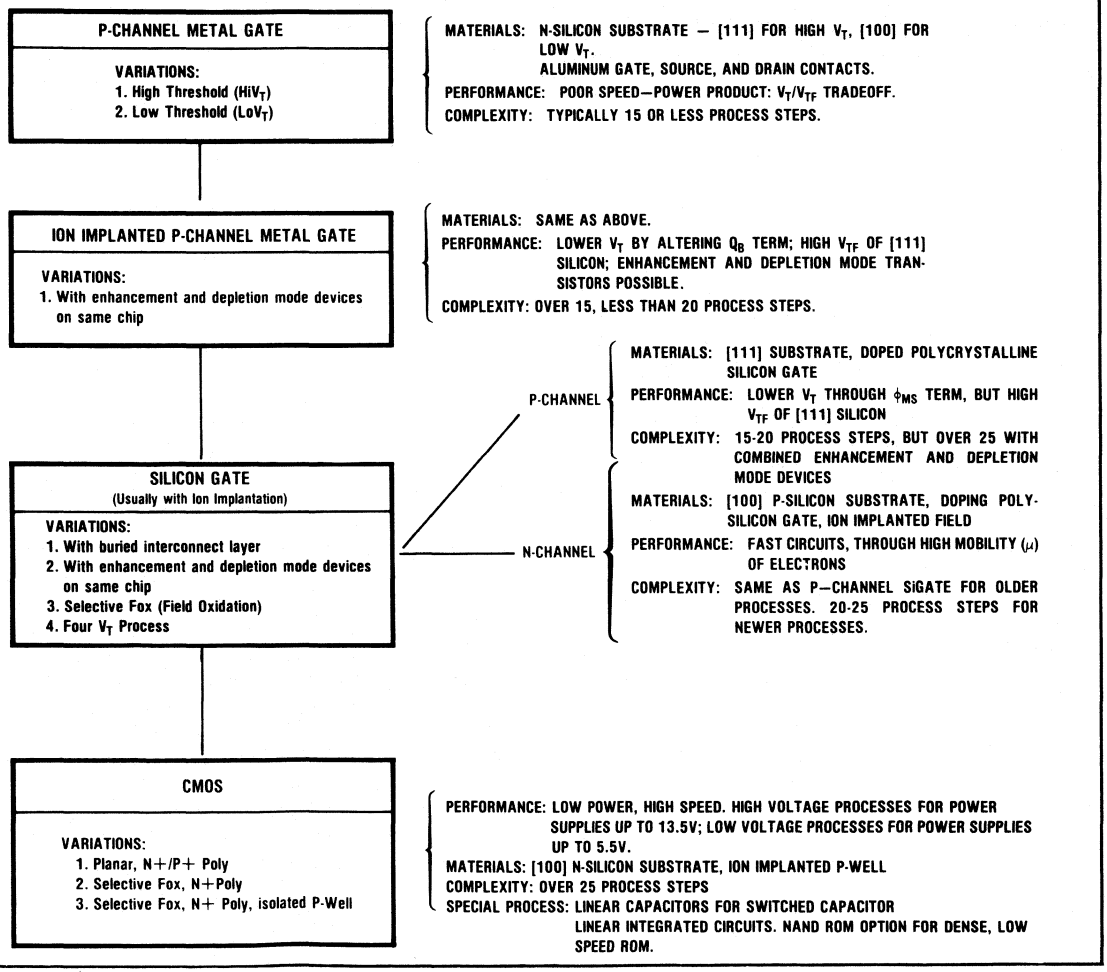
PROCESS DESCRIPTIONS

Each of the major MOS processes is described on the following pages. First, the established production proven processes are described, followed by those advanced processes, which are starting to go into volume production now. In each case, the basic processes is described first, followed by an explanation of its advantages, applications, etc.

P-CHANNEL METAL GATE PROCESS

Of all the basic MOS processes, P-Channel Metal Gate is the oldest and the most completely developed. It has served as the foundation for the MOS/LSI industry and still finds use today in some devices. Several versions of this process have evolved since its earliest days. A thin slice (8 to 10 mils) of lightly doped N-type silicon wafer serves as the substrate or body of the MOS transistor. Two closely spaced, heavily doped P-type regions, the source and drain, are formed within the substrate by selective diffusion of an impurity that provides holes as majority electrical carriers. A thin deposited layer of aluminum metal, the gate, covers the area between the source and drain regions, but is electrically insulated from the substrate by a thin layer (1000-15000Å) of silicon dioxide. The P-Channel transistor is turned on by a negative gate voltage and conducts current between

Figure B.1. Summary of MOS Process Characteristics



the source and the drain by means of holes as the majority carriers.

The basic P-Channel metal gate process can be subdivided into two general categories: *High-threshold and low-threshold.* Various manufacturers use different techniques (particularly so with the low threshold process) to achieve similar results, but the difference between them always rests in the threshold voltage V_T required to turn a transistor on. The high threshold V_T is typically -3 to -5 volts and the low threshold V_T is typically -1.5 to -2.5 volts.

The original technique used to achieve the difference in threshold voltages was by the use of substrates with different crystalline structures. The high V_T process used [111] silicon whereas, the low V_T process used [100] silicon. The difference in the silicon structure causes the surface charge between the substrate and the silicon dioxide to change in such a manner that it lowers the threshold voltages.

One of the main advantages of lowering V_T is the ability to interface the device with TTL circuitry. However, the use of [100] silicon carries with it a distinct disadvantage also. Just as the surface layer of the [100] silicon can be inverted by a lower V_T, so it also can be inverted at other random locations—through the thick oxide layers—by large voltages that may appear in the metal interconnections between circuit components. This is undesirable because it creates parasitic transistors, which interfere with circuit operation. The maximum voltage that can be carried in the interconnections is called the parasitic field oxide threshold voltage V_{TF}, and generally limits the overall voltage at which a circuit can operate. This, then, is the main factor that limits the use of the [100] low V_T process. A drop in V_{TF} between a high V_T and low V_T process may, for example, be from -28V to -17V.

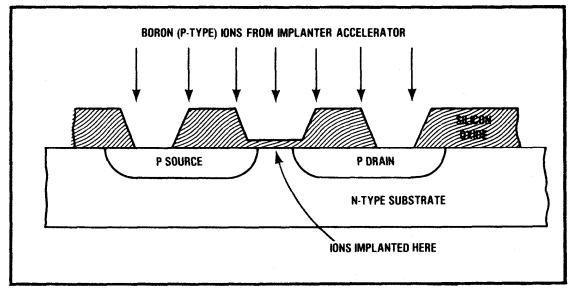
The low V_T process, because of its lower operating voltages, usually produces circuits with a lower operating speed than the high V_T process, but is easier to interface with other circuits, consumes less power, and therefore is more suitable for clocked circuits. Both P-Channel metal gate processes yield devices slower in speed than those made by other MOS processes, and have a relatively poor speed/power product. Both processes require two power supplies in most circuit designs, but the high V_T process, because it operates at a high threshold voltage, has excellent noise immunity.

Ion Implanted P-Channel Metal Gate Process

The P-Channel Ion Implanted process uses essentially the same geometrical structure and the same materials as the high V_T P-Channel process, but includes the ion implantation step. The purpose of ion implantation is to introduce P-type impurity ions into the substrate in the limited area under the gate electrode. By changing the characteristics of the substrate in the gate area, it is possible to lower the threshold voltage V_T of the transistor, without influencing any other of its properties.

Figure B.2. shows the ion implantation step in a diagrammatic manner. It is performed after the gate oxide is grown, but before the source, gate, and drain metallization deposition. The wafer is exposed to an ion beam which penetrates through the thin gate oxide layer and implants ions into the silicon substrate. Other areas of the substrate are protected both by the thicker oxide layer and sometimes also by other masking means. Ion implantation can be used with any process and, therefore could, except for the custom of the industry, be considered a special technique, rather than a process in itself.

Figure B.2. Diagram of Ion Implantation Step



The implantation of P-type ions into the substrate, in effect, reduces the effective concentration of N-type ions in the channel area and thus lowers the V_T required to turn the transistor on. At the same time, it does not alter the N-type ion concentration elsewhere in the substrate and therefore, does not reduce the parasitic field oxide threshold voltage V_{TF} (a problem with the low V_T P-Channel Metal Gate process, described above). The [111] silicon usually is used in ion-implanted transistors.

In fact, if the channel area is exposed to the ion beam long enough, the substrate in the area can be turned into P-type silicon (while the body of the substrate still re-

mains N-type) and the transistor becomes a depletion mode device. In any circuit some transistors can be made enhancement type, while others are depletion type, and the combination is a very useful circuit design tool.

The Ion-implanted P-Channel Metal Gate process is very much in use toady. Among all the processes, it represents a good optimization between cost and performance and thus is the logical choice for many common circuits, such as memory devices, data handling (communication) circuits, and others.

Because of its low V_T, it offers the designer a choice of using low power supply voltages to conserve power or increase supply voltages to get more driving power and thus increase speed. At low power levels it is more feasible to implement clock generating and gating circuits on the chip. In most circuit designs only a single power supply voltage is required.

N-CHANNEL PROCESS

Historically, N-Channel process and its advantages were known well at the time when the first P-Channel devices were successfully manufactured; however, it was much more difficult to produce N-Channel. One of the main reasons was that the polarity of intrinsic charges in the materials combined in such a way that a transistor was on at 0V and had a V_T of only a few tenths of a volt (*positive*). Thus, the transistor operated as a marginal depletion mode device without a well-defined *on/off* biasing range. Attempts to raise V_T by varying gate oxide thickness, increasing the substrate doping, and back biasing the substrate, created other objectionable results and it was not until research into materials, along with ion implantation, silicon gates, and other improvements came about that N-Channel became practical for high density circuits.

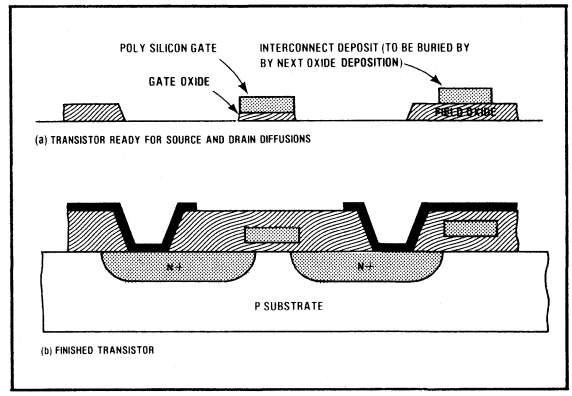
The N-Channel process gained its strength only after the P-Channel process, ion implantation, and silicon gate all were already well developed. N-Channel went into volume productions with advent of the 4K dynamic RAM and the microprocessor, both of which required speed and high density. Because P-Channel processes were nearing their limits in both of these respects, N-Channel became the logical answer.

The N-Channel process is structurally different from any of the processes described so far, in that the source, drain, and channel all are N-type silicon, whereas the body of the substrate is P-type. Conduction in the N-Channel is by means of electrons, rather than holes.

The main advantage of the N-Channel process is that the mobility of electrons is about three times greater than that of holes and, therefore, N-Channel transistors are faster than P-Channel . In addition, the increased mobility allows more current flow in a channel of any given size, and therefore N-Channel transistors can be made smaller. The positive gate voltage allows an N-Channel transistor to be completely compatible with TTL.

Although metal gate N-Channel processes have been used, the predominant N-Channel process is a silicon gate process. Among the advantages of silicon gate is the possibility of a buried layer of interconnect lines, in addition to the normal aluminum interconnections deposited on the surface of the chip. This gives the circuit designer more latitude in layout and often allows the reduction of the total chip size. Because the polysilicon gate electrode is deposited in a separate step, after the thick oxide layer is in place, the simultaneous deposition of additional polysilicon interconnect lines is only a matter of masking. These interconnect lines are buried by later steps, as shown in Figure B.3.

Figure B.3. Crosssection of an N-Channel Silicon Gate MOS Transistor



One minor limitation associated with the buried interconnect lines is their location. Because the source and drain diffusions are done after the polysilicon is deposited [see (a) of Figure B.3] the interconnect lines cannot be located over these diffusion regions.

A second advantage of a silicon gate is associated with the reduction of overlap between the gate and both the source and drain. This reduces the parasitic capacitance at each location and improves speed, as well as power consumption characteristics. Whereas in the metal gate process, the P region source and drain diffusion must be done prior to deposition of the gate electrode, in silicon gate process, the electrode is in place during diffusion, see (a) of Figure B.3. Therefore, no planned overlap for manufacturing tolerance purposes need exist and the gate is said to be *self-aligned.* The only overlap that occurs is due to the normal lateral extension of the source and drain regions during the diffusion process.

The silicon-gate process produces devices that are more compact than metal gate, and are slightly faster because of the reduced gate overlap capacitance. Because the basic silicon gate process is relatively simple, it is also economical. It is a versatile process that is used in memory devices and most any other circuit.

N-Channel development continues at a vigorous pace, resulting in all kinds of process variations, production techniques and applications. The combination of high speed, TTL compatibility, low power requirements, and compactness have already made N-Channel the most widely used process. The cost of N-Channel has been coming down also.

In addition to its use in large memory chips and microprocessors, N-Channel has become a good general purpose process for circuits in which compactness and high speed are important.

CMOS

The basic CMOS circuit is an inverter, which consists of two adjacent transistors—one an N-Channel, the other a P-Channel, as shown in Figure B.4. The two are fabricated on the same substrate, which can be either N or P type.

The CMOS inverter in Figure B.4 is fabricated on an N-type silicon substrate in which a P "tub" is diffused to form the body for the N-Channel transistor. All other steps, including the use of silicon gates and ion implantation, are much the same as for other processes.

The main advantage of CMOS is extremely low power consumption. When the common input to both gate electrodes is at a logic 1 (a positive voltage) the N-Channel transistor is biased on, the P-Channel is off, and the output is near ground potential. Conversely, when the input is at a logic 0 level, its negative voltage biases only the P-Channel transistor on and the output is near the drain voltage $+V_{DD}$. In either case, only one of the two transistors is on at a time and thus, there is virtually no current flow and no power consumption. Only during the transition from one logic level to the other are both transistors on and current flow increases momentarily.

Silicon Gate CMOS is also fast, approaching speeds of bipolar TTL circuits. On the other hand, the use of two transistors in every gate makes CMOS slightly more complex and costly, and requires more chip size. For these reasons, the original popularity of CMOS was in SSI logic elements and MSI circuits—logic gates, inverters, small shift registers, counters, etc. These CMOS devices consititute a logic family in the same way as TTL, ECL, and other bipolar circuits do; and in the areas of very low power consumption, high noise immunity, and simplicity of operation, are still widely accepted by discrete logic circuit designers.

Low power CMOS circuits made the watch circuit possible and also have been used in space exploration, battery operated consumer products, and automotive control devices. As experience was gained with CMOS, tighter design rules and reduced device sizes have been implemented and now LSI circuits, such as 1K RAM memories and microprocessors, are being manufactured in volume.

CMOS circuits can be operated on a single power supply voltage, which can be varied from +2.5 to about +13.5 volts with the high voltage processes, with a higher voltage giving more speed and higher noise immunity. Low voltage processes allow single power supply voltages from +1.5 to +5.5 volts.

The first implementation of an inverting gate is a process that uses both n+ to p+ polysilicon. The basic structure is a first-generation approach to which a selective field-oxidation process has been added. (At American Microsystems, Inc., the selective field-oxidation process is used only to shrink existing designs down to 5-micrometer rules; it is not applied to new designs.)

Figure B.5 shows the plan and section views of the three-device gate portion. Because the P-Well in the top view spans both N-Channel devices, it is referred to as ubiquitous, and the process is called Ubiquitous P-Well.

In this planar process, p+ guard rings are used to reduce

surface leakage. Polysilicon cannot cross the rings, however, so that bridges must be built. Note the use of p+ polysilicon in the P-Channel areas. The plan view shows the construction of the bridges linking p+ to metal to n+. (Were the process to be used for a low-voltage, first-generation application like a watch circuit, the guard rings would not be necessary and polysilicon could directly connect N-Channel and P-Channel devices; however, to ensure good ohmic contact from one type of polysilicon to another, polysilicon-diode contacts must be capped with metal.)

This process provides a buried contact (n+ polysilicon to n+ diffusion) that can yield a circuit-density advantage. However, neither of the other two second-generation approaches provides buried contacts. Therefore, if a layout in this process is to be compatible with the others, the buried contact must be eliminated. Though there will be a penalty in real estate, the gain for custom applications is a great increase in the number of available CMOS vendors.

The n+-Only Polysilicon Aproach

Both of the second-generation CMOS processes that follow are variants of the n+-only, selective-field-oxide approach. One closely resembles the p+ n+ Ubiquitous-P-Well process, since it, too, has a Ubiquitous P-Well that is implanted before the field oxidation and thus runs under the field oxide. The other, called isolated P-Well, has separate wells for each N-Channel device that are implanted after field oxidation.

Figure B.6 shows the section and plan views of the n+-only Ubiquitous-P-Well approach used to build the gate of Figure B.4. This is the 5μm process recommended by AMI and others for new, high-performance CMOS designs. The layout is simpler than with the n+/p+ polysilicon Ubiquitous-Well approach (there are no buried contacts and no polysilicon-diode contacts), and it occupies less area for the same line widths. Also, since the process permits implanting in the field region, no guard rings are required. Polysilicon can thus cross directly from P- to N-Channel device areas without the need for bridges or polysilicon-dioxide contacts.

Figure B.4. Crossection and Schematic Diagram of a CMOS Inverter

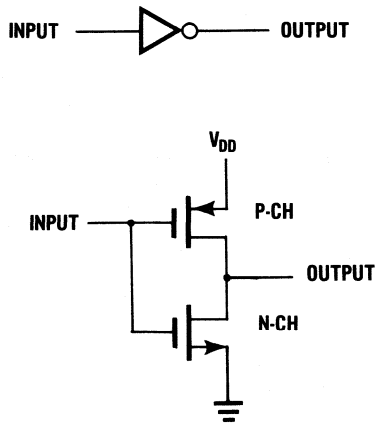
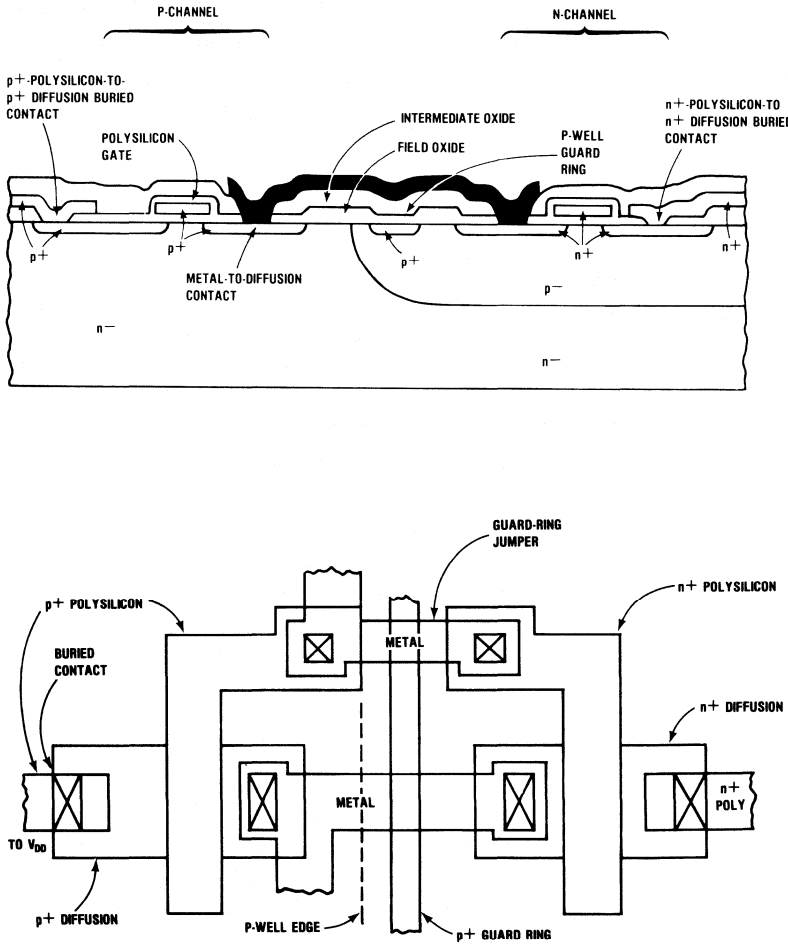
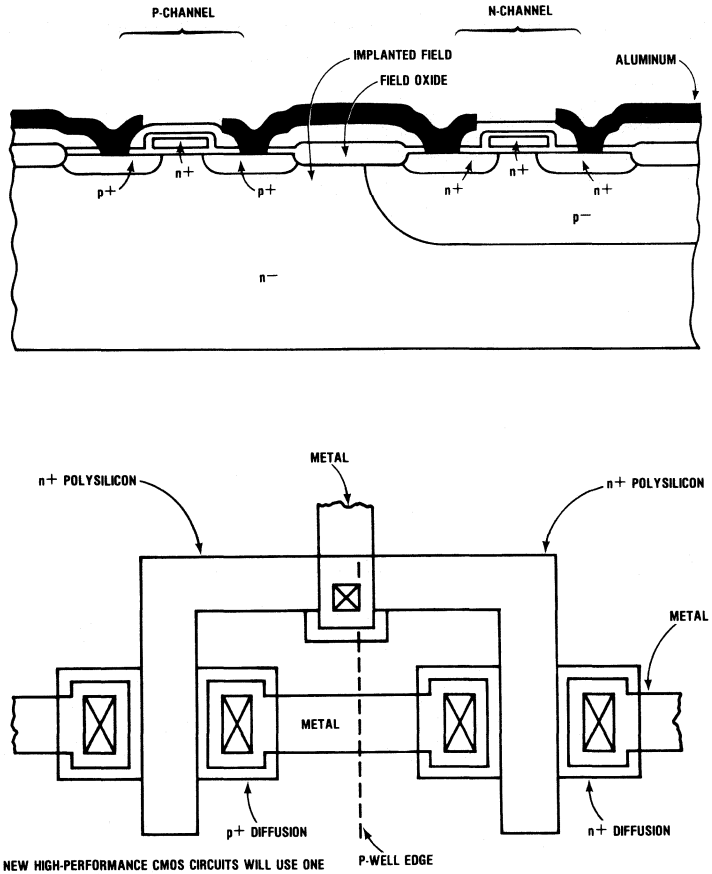


Figure B.5. n+/p+ Polysilicon Approach



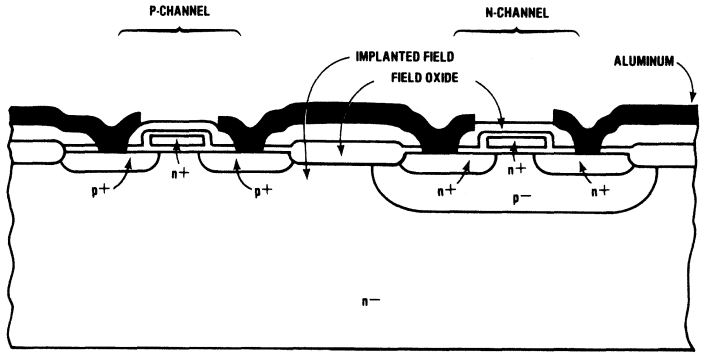
THE FIRST HIGH-PERFORMANCE COMPLEMENTARY-MOS PLANAR PROCESS. ITS DRAWBACKS: TWO TYPES OF POLYSILICON ARE USED, AND THE UNAVAILABILITY OF FIELD IMPLANT DOPING TIES FIELD THRESHOLD TO DEVICE THRESHOLDS.

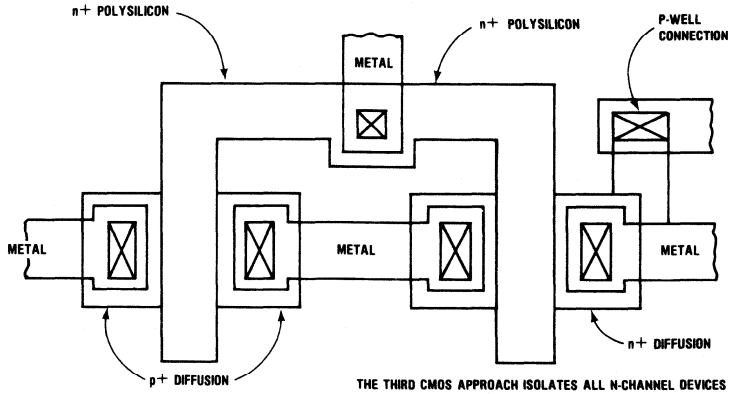
Figure B.6. n+-Only Polysilicon Approach



ALL NEW HIGH-PERFORMANCE CMOS CIRCUITS WILL USE ONE TYPE OF POLYSILICON. THIS VERSION HAS A UBIQUITOUS P-WELL: THAT IS, SERIES N-CHANNEL DEVICES SIT IN A COMMON P-WELL, WHICH, IMPLANTED BEFORE FIELD OXIDATION, RUNS UNDER THE FIELD OXIDE. THIS IS AMI'S PREFERRED CMOS PROCESS FORMAT FOR ALL NEW DESIGNS.

Figure B.7. Isolated Wells.





THE THIRD CMOS APPROACH ISOLATES ALL N-CHANNEL DEVICES IN SEPARATE P-WELLS. SINCE THE ISOLATED WELLS MUST BE DOPED MUCH MORE HEAVILY THAN THOSE OF THE UBIQUITOUS-WELL APPROACH, n+-TO P-WELL CAPACITANCE IS GREATER AND SWITCHING SPEEDS LOWER. THIS IS AN n+-ONLY POLYSILICON PROCESS.

A variant of the all n+ (See Figure B.7) polysilicon process just discussed uses basically the selective field-oxide approach except that the P-Wells are not continuous under the field-oxide areas; they are instead bounded by field-oxide edges. Since the P-Wells are naturally isolated from one another, the process is called n+ poly-isolated P-Well. The isolated wells must all be connected to ground; if they are left floating, circuit malfunctions are bound to occur. The grounding is done either with p+ diffusions or with top-side metalization that covers a p+-to-P-Well contact diffusion.

In the Isolated-Well process, the P-Wells must be doped much more heavily than in the Ubiquitous-Well process. One result is a higher junction capacitance between the n+ areas and the wells that both slows switching speeds and raises the power dissipation of a device. Even though the speed loss could be compensated for by slightly shorter channel lengths, the operating power still remains high.

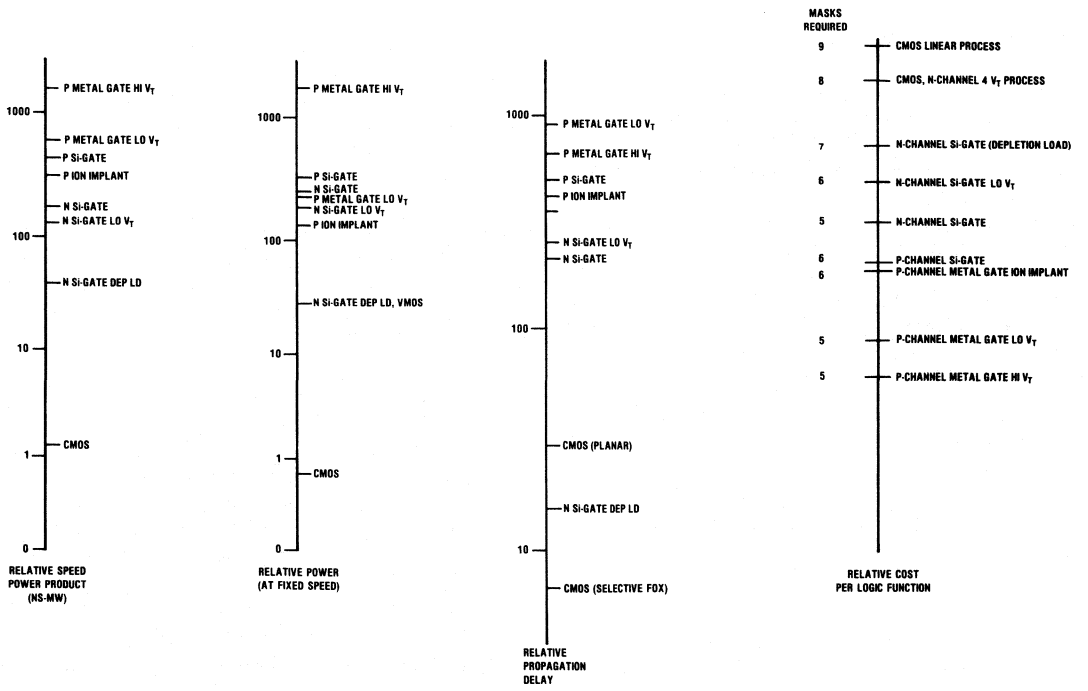
Although currently available from AMI and other manufacturers, the Isolated-Well process is in fact not recommended for new designs by AMI. Its layout takes up more area than does one using the Ubiquitous-Well approach, even though its P-Well to p+-area spacing is slightly less.

Table 1. Layout Compatibility Concerns for CMOS Processes

LAYOUT FEATURE	n+/p+ POLY-SILICON UBIQUITOUS P-WELL	n+-ONLY POLYSILICON UBIQUITOUS P-WELL	n+-ONLY POLY SILICON ISOLATED P-WELL
BURIED CONTACT	X	NO	NO
POLYSILICON DIODE CONTACT	YES	X	X
P-WELL ISOLATION WITH DIFFUSION MASK	NO	NO	YES
TIGHT P-WELL-TO-p+ SPACING	NO	NO	YES
LAYOUT CARE REQUIRED FOR P-WELL ELECTRICAL CONTACTS	NO	NO	YES

X = DOES NOT MATTER

Figure B.8. Comparative Data on Major MOS Processes



INTRODUCTION

Quality is one of the most used, least understood, and variously defined assets of the semiconductor industry. At AMI we have always known just how important effective quality assurance, quality control, and reliability monitoring are in the ability to deliver a repeatably reliable product. Particularly, through the manufacture of custom MOS/LSI, experience has proved that one of the most important tasks of quality assurance is the effective control and monitoring of manufacturing processes. Such control and monitoring has a twofold purpose: to assure a consistently good product, and to assure that the product can be manufactured at a later date with the same degree of reliability.

To effectively achieve these objectives, AMI has developed a Product Assurance Program consisting of three major functions:

- ☐ Quality Control
- ☐ Quality Assurance
- ☐ Reliability

Each function has a different area of concern, but all share the responsibility for a reliable product.

The AMI Product Assurance Program

The program is based on MIL-STD-883, MIL-M-38510, and MIL-Q-9858A methods. Under this program, AMI manufactures highest quality MOS devices for all segments of the commercial and industrial market and, under special adaptations of the basic program, also manufactures high reliability devices to full military specifications for specific customers.

The three aspects of the AMI Product Assurance Program—Quality Control, Quality Assurance, and Reliability— have been developed as a result of many years of experience in MOS device design and manufacture.

Quality Control establishes that every method meets or fails to meet, processing or production standards—*QC checks methods.*

Quality Assurance establishes that every method meets, or fails to meet, product parameters—*QA checks results.*

Reliability establishes that QA and QC are effective—*Reliability checks device performance.*

One indication that the AMI Product Assurance Program has been effective is that NASA has endorsed AMI products for flight quality hardware since 1967. The Lunar Landers and Mars Landers all have incorporated AMI circuits, and AMI circuits have also been utilized in the Viking and Vinson programs, as well as many other military airborne and reconnaissance hardware programs.

QUALITY CONTROL

The Quality Control function in AMI's Product Assurance Program involves constant monitoring of all aspects of materials and production, starting with the raw materials purchased, through all processing steps, to device shipment. There are three major areas of Quality Control:

- ☐ Incoming Materials Control
- ☐ Microlithography Control
- ☐ Process/Assembly Control

Incoming Materials Control

All purchased materials, including raw silicon, are checked carefully to various test and sampling plans. The purpose of incoming materials inspection is to ensure that all items required for the production of AMI MOS circuits meet such standards as are required for the production of high quality, high reliability devices.

Incoming inspection is performed to specifications agreed to by suppliers of all materials. The Quality Control group continuously analyzes supplier performance, performs comparative analysis of different suppliers, and qualifies the suppliers.

Tests are performed on all direct material, including packages, wire, lids, eutectics, and lead frames. These tests are performed using a basic sampling plan in accordance with MIL-S-19500, generally to a Lot Tolerance Percent Defective (LTPD) level of 10%. The AQL must be below 1% overall.

Two incoming material inspection sequences illustrate the thoroughness of AMI Quality Control:

- ☐ Purchased packages are first inspected visually. Then, dimensional inspections are performed, followed by a full functional inspection, which subjects the packages to an entire production run simulation. Finally, a full electrical evaluation is made, including checks of the insulation, resistance, and lead-to-lead isolation. A package lot which passes these tests to an acceptable LTPD level is accepted.
- ☐ Raw silicon must also pass visual and dimensional checks. In addition, a preferential etch quality inspection is performed. For this inspection, the underlayers

of bulk silicon are examined for potential anomalies such as dislocation, slippage or etch pits. Resistivity of the silicon is also tested.

Microlithography Control

Microlithography involves the processes which result in finished working plates, used for the fabrication of wafers. These processes are pattern or artwork generation, photo-reduction, and the actual printing of the working plates.

Pattern generation now is the most common practice at AMI. The circuit layout is digitized and stored on a tape, which then is read into an automated pattern generator which prints a highly accurate 10x reticle directly.

In cases where the more traditional method of artwork generation is used whether Rubylith, Gerber Plots, AMI generated or customer generated—the artwork is throughly inspected. It is checked for level-to-level registration and dimensional tolerances. Also, a close visual inspection of the workmanship is made. AMI artwork is usually produced at 200x magnification and must conform to stringent design rules, which have been developed over a period of years as part of the process control requirements.

Acceptable artwork is photographically reduced to a 20x magnification, and then further to a 10x magnification. The resulting 10x reticles are then used for producing 1x masters. The masters undergo severe registration comparisons to a registration master and all dimensions are checked to insure that reductions have been precise. During this step, image and geometry are scrutinized for missing or faded portions and other possible photographic omissions.

For a typical N-Channel silicon gate device, master sets are checked at all six geometry levels in various combinations against each other and against a proven master set. Allowable deviations within the die are limited to 0.5 micron, deviations within a plate are limited to 1 micron, and all plate deviations are considered cumulatively.

Upon successful completion of a device master set, it is released to manufacturing where the 1x plates are printed. A sample inspection is performed by manufacturing on each 30-plate lot and the entire lot is returned to Quality Control for final acceptance. Quality Control performs audits on each manufacturing inspector daily, by sample inspection techniques.

The plates can be rejected first by manufacturing, when the 30-plate lots are inspected, or by Quality Control when the lots are submitted for final acceptance. If either group rejects the plates, they are rescreened and then undergo the same inspection sequence. In the rescreening process, the plates undergo registration checks; visual checks for pin holes, protrusions, and faded or missing images, as well as all critical dimension checks.

Process Control

Once device production has started in manufacturing, AMI Quality Control becomes involved in one of the most important aspects of the Product Assurance Program—the analysis and monitoring of virtually all production processes, equipment, and devices.

Process controls are performed in the fabrication area, by the Quality Control Fabrication Group, to assure adherence to specifications. This involves checks on operators, equipment and environment. Operators are tested for familiarity with equipment and adherence to procedure. Equipment is closely checked both through calibration and maintenance audits. Environmental control involves close monitoring of temperature, relative humidity, water resistivity and bacteria content, as well as particle content in ambient air. All parameters are accurately controlled to minimize the possiblity of contamination or adverse effects due to temperature or humidity excesses.

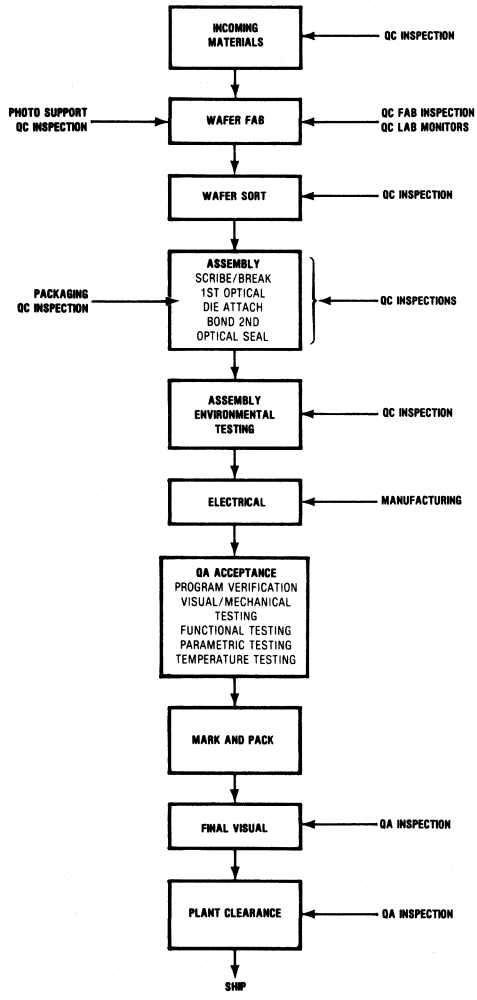
Experience has proven that such close control of the operators, equipment, and environment is highly effective towards improved quality and increased yields.

In addition to the specification adherence activities of the QC Fabrication Group, a QC Laboratory performs constant process monitoring of virtually every step of all processes. Specimens are taken from all production steps and critically evaluated. Sampling frequency varies, depending on the process, but generally, oxidation, diffusion, masking, and evaporization are the most closely monitored steps.

Results are supplied both to manufacturing and engineering. When evidence of a problem occurs, QC provides recommendations for corrections and follows up the corrective action taken.

Optical Inspections are performed at several steps; quality control limits are based on a 10% LTPD. The chart in Figure 1 shows process steps and process control points.

Figure 1. Flowchart of Product Assurance Program Implementation



QUALITY ASSURANCE

The Quality Assurance function in the Product Assurance Program involves checking the ability of manufactured parts to meet specifications. In addition, the QA group also is responsible for calibration of all equipment, and for the maintenance of AMI internal product specifications, to assure that they are always in conformance with customer specifications or other AMI specifications.

After devices undergo 100% testing in manufacturing, they are sent to Quality Assurance for acceptance. Lots are defined, and using the product specifications, sample sizes are determined, along with the types of tests to be performed and the test equipment to be used. Lots must pass QA testing either with an LTPD of 10%, or less, if the specification requires tighter limits. Lots with quantities greater than 2000 are checked to a 1% AQL or less.

Three types of tests are performed on the samples: visual/mechanical, parametric, and functional. All tests are performed both at room temperature and at elevated temperature. In addition, a number of other special temperature tests may be performed if required by the specification.

To perform the tests, QA uses AMI PAFT test systems, ROM test systems, Macrodata testers, Fairchild *Sentry*, LTX *Sentinel*, *XINCOM* systems, Teradyne test systems, and various bench test units. In special instances a part may also be tested in a real life environment in the equipment which is to finally utilize it.

If a lot is rejected during QA testing, it is returned to the production source for an electrical rescreening. It is then returned to QA for acceptance but is identified as a resubmitted lot. If it fails again, corrective action in engineering is initiated. As evidence of the problem is detected, the parts may also be traced all the way back to the wafer run to analyze the cause.

When a lot is acceptable, it is sent to packaging and then to finished goods. When parts leave finished goods, they are again checked by the QA group to a 10% LTPD with visual/mechanical tests. Also, all supporting documentation for the parts is verified, including QA acceptance, special customer specifications, certificates of compliance, etc. Only after this last check are devices considered ready for plant clearance.

If there are customer returns, they are first sample tested by QA to determine the cause of the return. (Many times an invalid customer test will incorrectly cause returns.) Selected return samples are sent to Reliability for failure analysis.

RELIABILITY

The Reliability function in the Product Assurance Program involves process qualification, device qualification,

package qualification, reliability program qualification and failure analysis. To perform these functions AMI Reliability group is organized into two major areas:

- ☐ Reliability Laboratory
- ☐ Failure Analysis

Reliability Laboratory

AMI Reliability Laboratory is responsible for the following functions.

- ☐ New Process Qualification
- ☐ Process Change Qualification
- ☐ Process Monitoring
- ☐ New Device Qualification
- ☐ Device Change Qualification
- ☐ New Package Qualification
- ☐ Device Monitoring
- ☐ Package Change Qualification
- ☐ Package Monitoring
- ☐ High Reliability Programs

There are various closely interrelated and interactive phases involved in the development of a new process, device, package or reliability program. A process change may affect device performance, a device change may affect process repeatability, and a package change may affect both device performance and process repeatability. To be effective. the Reliability Laboratory must monitor and analyze all aspects of new or changed processes, devices, and packages. It must be determined what the final effect is on product reliability, and then evaluate the merits of the innovation or change.

Process Qualification

For example, AMI Research and Development group recommends a new process or process alteration when it feels that the change can result in product improvement. The Reliability Laboratory then performs appropriate environmental and electrical evaluations of a new process. Typically, a special test vehicle, or "rel chip", generated by R&D during process development, is used to qualify the recommended new process or process change.

The rel chip is composed of circuit elements similar to those that may be required under worst-case circuit design conditions. The rel chip elements are standard for any given process, and thus allow precise comparisons between diffusion runs. The following is an example of what is included on a typical rel chip:

- ☐ A discrete inverter and an MOS capacitor
- ☐ A large P-N junction covered by an MOS capacitor.
- ☐ A large P-N junction area (identical to the junction area above, but without the MOS capacitor)
- ☐ A large area MOS capacitor over substrate
- ☐ Several long contact strings with different contact geometries
- ☐ Several long conductor geometries, which cross a series of eight deeply etched areas

Each circuit element of a rel chip allows a specific test to be performed. As an example, the discrete inverter and MOS load device accommodate power life tests. As a consequence, any type of parameter drift can be observed. The MOS capacitor, covering the large P-N junction, can serve to indicate the presence of contamination in the oxide, under the oxide, or in the bulk silicon. If unusual drift is evidenced, the location of contamination can be determined through analysis of the additional MOS capacitor and the large P-N junction area. The metal conductor interconnecting contacts is useful for life testing under relatively high current conditions. It facilitates the detection of metal separation when moisture or other contaminants are present.

The conductors crossing deeply etched areas allow the checking of process control. Rather than depending upon optical inspection of metal quality, burned out areas caused by high currents are readily identified and provide a quantitative measure of metal quality.

If the Reliability Laboratory determines that a recommended new process or process change is viable for manufacturing purposes, further analysis is necessary to determine that production devices can be manufactured in high volume, in a repeatable and reliable manner.

Process Monitoring

In addition to process qualification, the Reliability group also conducts ongoing process monitoring programs. Once every 90 days each major production process is evaluated using rel chips as test vehicles. The resulting test data is analyzed for parameter limits and process stability. In this manner AMI can help assure repeatability and high product quality.

Package Qualification

New packages are also qualified before they are adopted. To analyze packages, a qualification matrix is designed, according to which the new package and an established package (used for control) are tested concurrently. The test matrix consists of a full spectrum of electrical and environmental stress tests, in accordance with MIL-STD-883.

Failure Analysis

Another important function of the Reliability group is failure analysis. Scanning electron microscopes, high power optical microscopes, diagnostic probe stations, and other equipment is used in failure analysis of devices submitted from various sources. It is the function of the Reliability group to determine the cause of failure and recommend corrective action.

The Reliability group provides a failure analysis service for the previously mentioned in-house programs and for the evaluation of customer returns. All AMI customers are provided a failure analysis service for any part that fails within one year from date of purchase and the results of the analysis are returned in the form of a written report.

SUMMARY

The Product Assurance Program at AMI is oriented towards process control and monitoring, and the evaluation of devices. The Program consists of three major functions: Quality Control, Quality Assurance, and Reliability. Constant monitoring of all phases of production, with information feedback at all levels, allows fast and efficient detection of problems, evaluation and analysis, correction, and verification of the correction. The overall result is a line of products which are highly repeatable and reliabile, with a very low reject level.

Aerospace and defense equipments generally require LSI microcircuits capable of superior product reliability and performance. To meet these needs, AMI offers two standard screening options patterned after MIL-STD-883, Method 5004.

Operation/MIL-STD-883 Test Method	Class B Method 5004.5 MIL-STD-883	Class C Method 5004.5 MIL-STD-883
Internal Visual/2010	Condition B	Condition B
Final Seal	100%	100%
Stabilization Bake/1008	Condition C, 24 Hours	Condition C, 24 Hours
Temperature Cycle/1010, 10 Cycles	Condition C	Condition C
Constant Acceleration/2001(1)	Y_1 Axis	Y_1 Axis
Seal Test/1014		
—Fine Leak	Condition A or B	Condition A or B
—Gross Leak	Condition C	Condition C
Pre-burn-in Electrical Test	@AMI Option(2)	—
Burn-in/1015(3)	125°C Min, 160 Hours	—
Final Electrical Test/5004(4)		
—Static Tests, 25°C	100%	100%
—Static Tests, Maximum Rated Operating Temperature	100%	—
—Static Tests, Minimum Rated Operating Temperature	100%	—
—Switching Tests, 25°C	100%	—
—Functional Tests, 25°C	100%	100%
Group A Electricals/5005	Sample(5)	Sample(5)
−55°C, 25°C, 125°C	Table I	Table I

Notes:

(1) Stress level (g) applied is dependent on package size/lead count.

(2) Per paragraph 3.5.1 of MIL-STD-883, Method 5004.

(3) Per MIL-STD-883, Method 1015 and Method 5004, paragraph 3.4.2, accelerated testing (Test Condition F of Method 1015) may be used at AMI's option.

(4) Final test electrical measurements per the applicable AMI data sheet.

(5) Group A is performed on each lot.

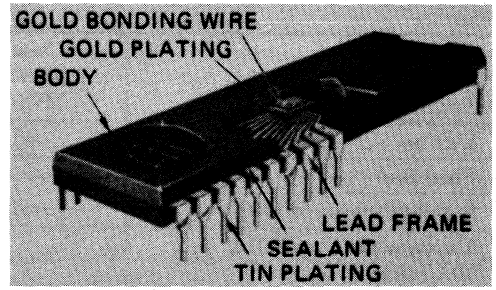
PART NUMBER	DESCRIPTION
MBC 6800 MCC 6800	8-Bit Microprocessor 8-Bit Microprocessor
MBC 6802 MCC 6802	8-Bit Microprocessor with Clock and 128×8 Bit On-Chip RAM 8-Bit Microprocessor with Clock and 128×8 Bit On-Chip RAM
MBC 6808 MCC 6808	8-Bit Microprocessor with Clock 8-Bit Microprocessor with Clock
MBC 6810 MCC 6810	1024-Bit (128×8) Static Read/Write Memory 1024-Bit (128×8) Static Read/Write Memory
MBC 6821 MCC 6821	Peripheral Interface Adapter (PIA) Peripheral Interface Adapter (PIA)
MBC 6840 MCC 6840	Programmable Timer Programmable Timer
MBC 6852 MCC 6852	Synchronous Serial Data Adapter Synchronous Serial Data Adapter
MBC 6831B MCC 6831B	16,384-Bit (2048×8) Static NMOS ROM 16,384-Bit (2048×8) Static NMOS ROM
MBC 5101L-4 MCC 5101L-4	1024-Bit (256×4) Static CMOS RAM 1024-Bit (256×4) Static RAM
MBC 6508 MCC 6508	1024-Bit (1024×1) Static CMOS RAM 1024-Bit (1024×1) Static CMOS RAM

PLASTIC PACKAGE

The AMI plastic dual-in-line package is the equivalent of the widely accepted industry standard, refined by AMI for MOS/LSI applications. The package consists of a plastic body, transfer-molded directly onto the assembled lead frame and die. The lead frame is Kovar or Alloy 42, with external pins tin plated. Internally, there is a 50μin. gold spot on the die attach pad and on each bonding fingertip. Gold bonding wire is attached with the thermo-compression gold ball bonding technique.

Materials of the lead frame, the package body, and the die attach are all closely matched in thermal expansion coefficients, to provide optimum response to various thermal conditions. During manufacture every step of the process is rigorously monitored to assure maximum quality of the AMI plastic package.

Available in: 8, 14, 16, 18, 22, 24, 28, 40 and 64 pin configurations.

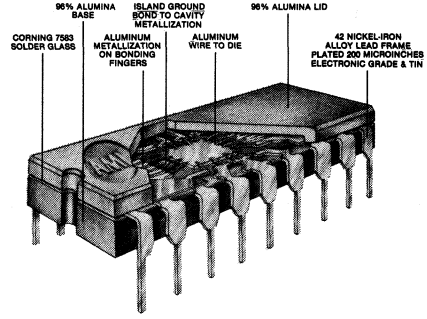


Cerdip PACKAGE

The Cerdip dual-in-line package has the same high performance characteristics as the standard three-layer ceramic package yet is a cost-effective alternative. It is a military approved type package with excellent reliability characteristics.

The package consists of an Alumina (Al_2O_3) base and the same material lid, hermetically fused onto the base with low temperature solder glass. Inert gasses are sealed inside the die cavity.

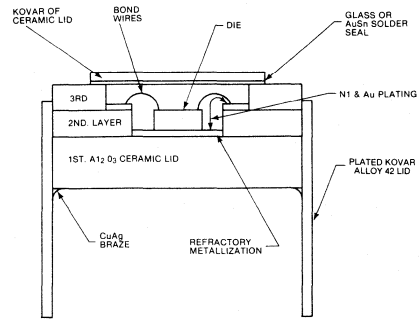
Available in 14,16,18,22,24,28 and 40 pin configurations.



CERAMIC PACKAGE

Industry standard high performance, high reliability package, made of three layers of AL_2O_3 ceramic and nickel-plated refractory metal. Either a low temperature glass sealed ceramic lid or a gold tin *eutectic* sealer Kovar lid is used to form the hermetic cavity of this package. Package leads are available with gold over nickel or tin plating for socket insertion or soldering.

Available in 14, 16, 18, 22, 24, 28, 40 and 64 pin configurations.

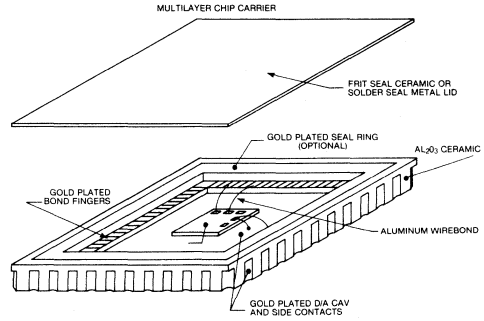


CHIP CARRIER PACKAGE

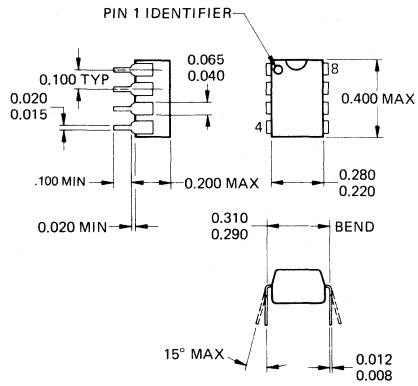
Chip carriers are the new industry standard in reducing package size. Built on the same concept as the highly reliable side-braze ceramic package, it is made of three layers of AL_2O_3 ceramic, refactory metallization, and gold plating. The chip carrier also offers contact pads equally spaced on all four sides of the carrier resulting in increased package density, better electrical characteristics, and a more cost effective way of packaging IC devices.

The package comes with a gold tin *eutectic* sealed metal lid or the low cost glass sealed ceramic lid creating a standard hermetic cavity.

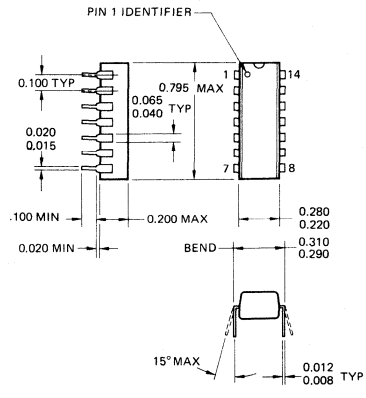
Available in 24, 28, 40 LD pin configurations to the JEDEC and Mantec standards.



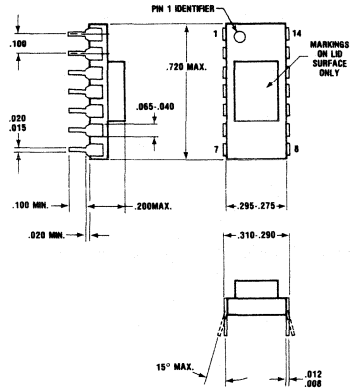
8-Pin Plastic



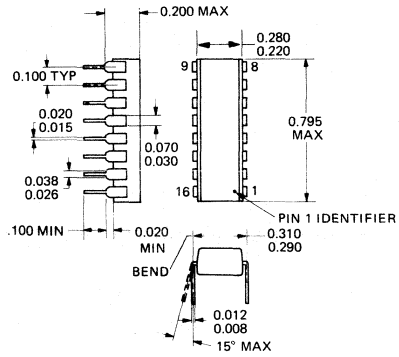
14-Pin Plastic



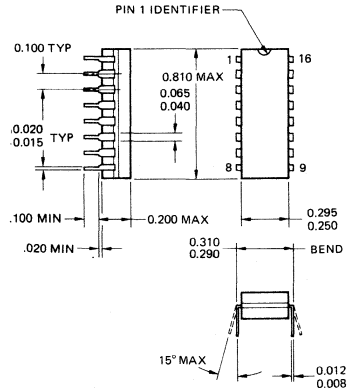
14-Pin Ceramic



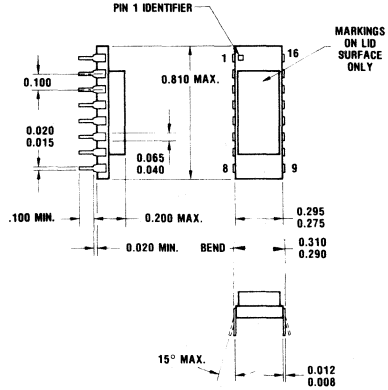
16-Pin Plastic



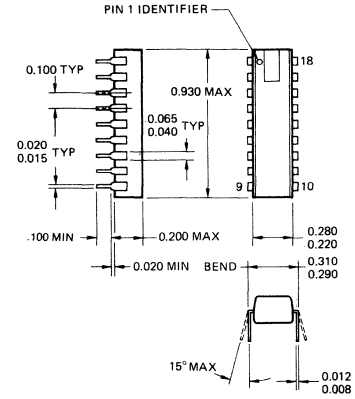
16-Pin Cerdip



16-Pin Ceramic



18-Pin Plastic



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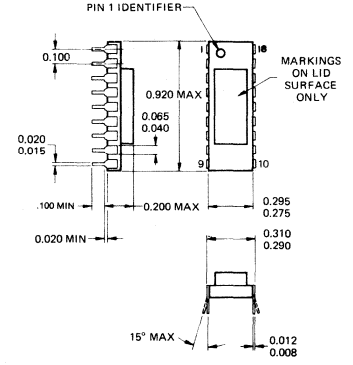
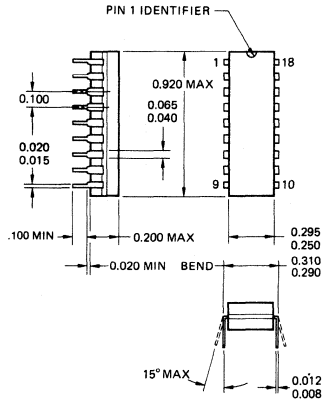
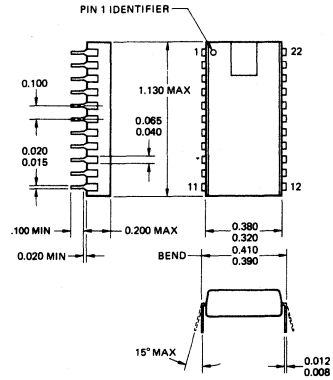


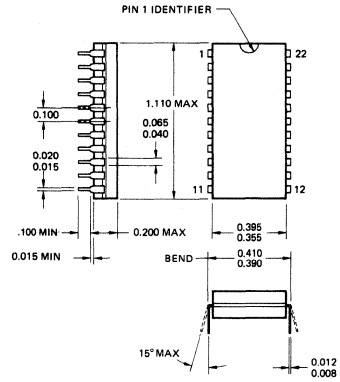
18-Pin Cerdip



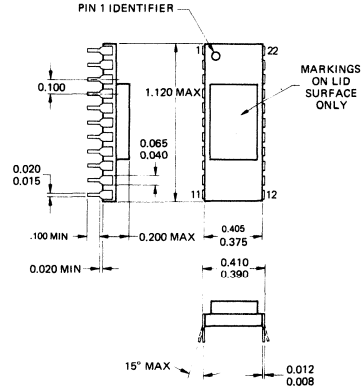
22-Pin Plastic



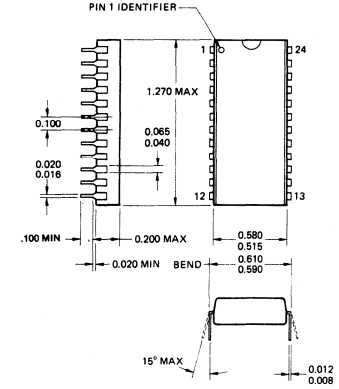
22-Pin Cerdip



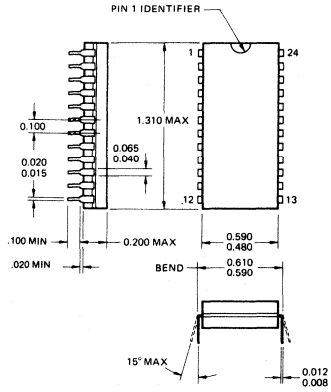
22-Pin Ceramic



24-Pin Plastic



24-Pin Cerdip



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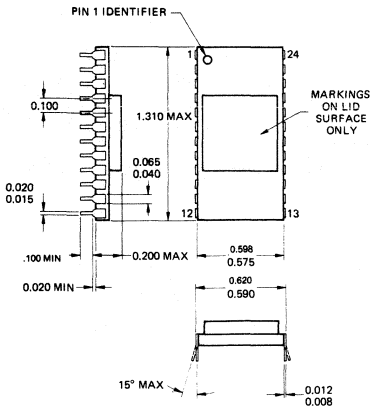
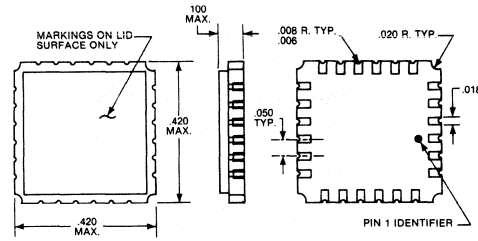
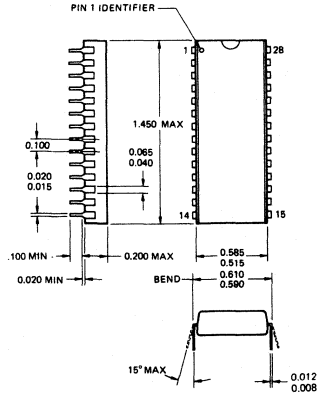


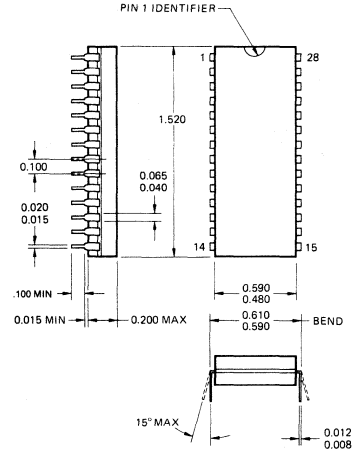
24-Lead Chip Carrier



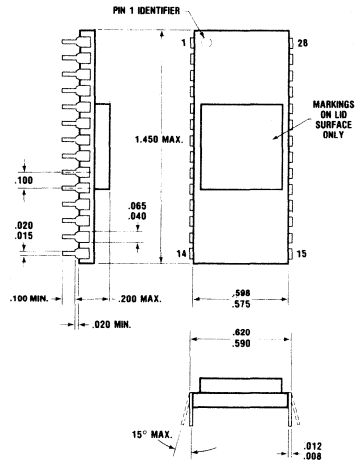
28-Pin Plastic



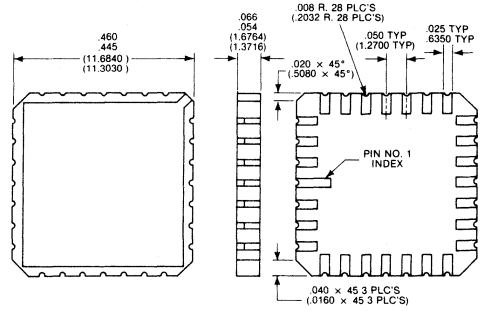
28-Pin Cerdip



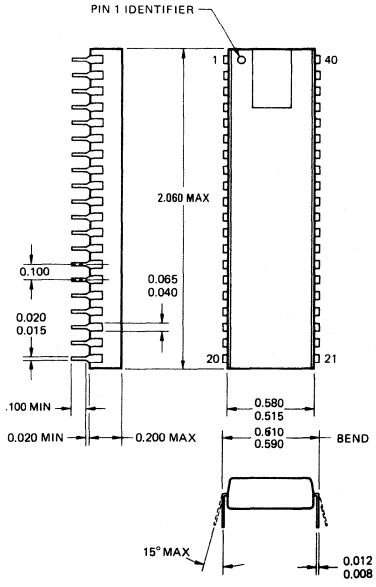
28-Pin Ceramic



28-Lead Chip Carrier



40-Pin Plastic



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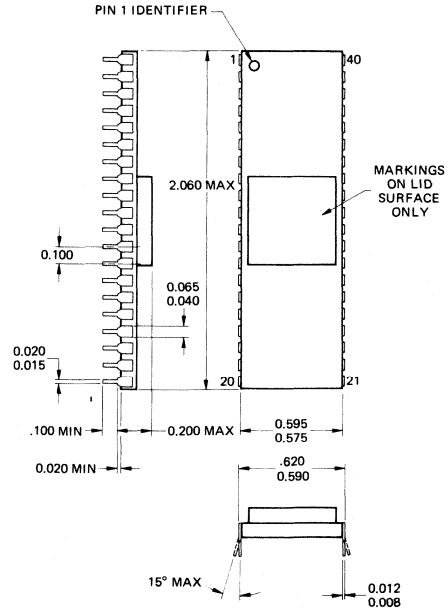
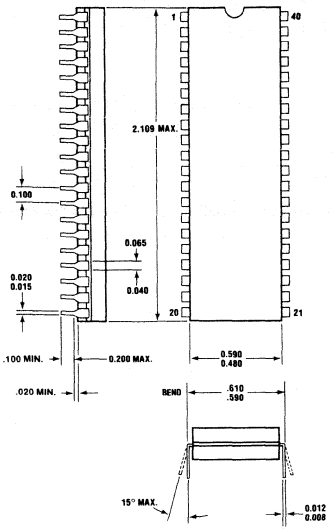
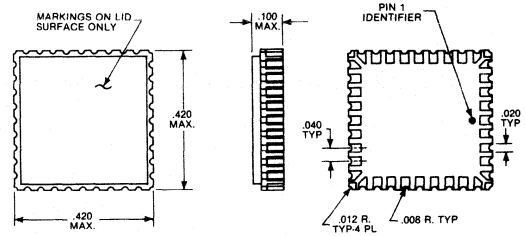


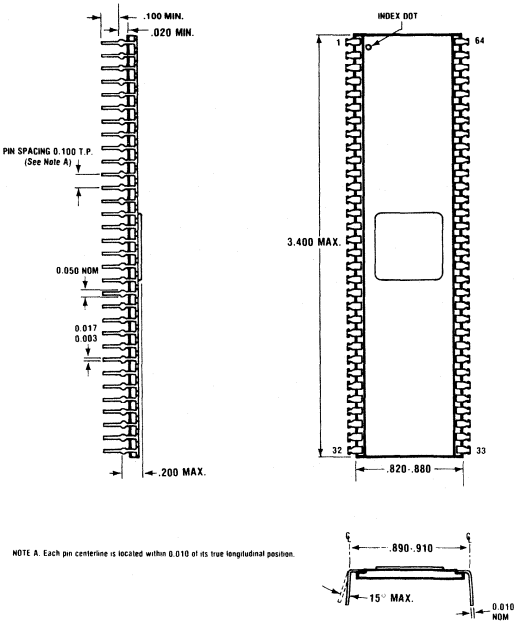
40-Pin Cerdip



40-Lead Chip Carrier

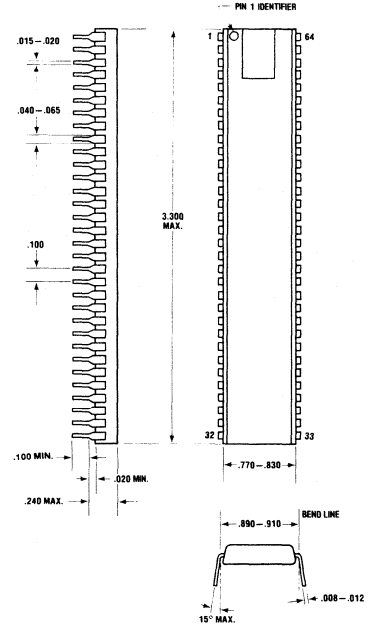


64-Pin Ceramic



NOTE A. Each pin centerline is located within 0.010 of its true longitudinal position.

64-Pin Plastic

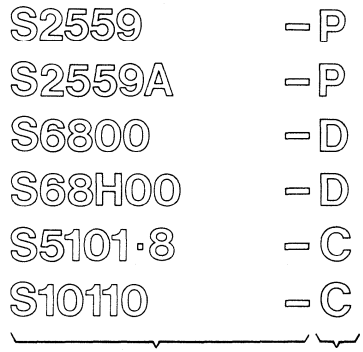


Standard Products:

Any product in this MOS Products Catalog can be ordered using the simple system described below. With this system it is possible to completely specify any standard device in this catalog in a manner that is compatible with AMI's order processing methods. The example below shows how this ordering system works and will help you to order your parts in a manner that can be expedited rapidly and accurately.

All orders (except those in sample quantities) are normally shipped in plastic carriers or aluminum tube containers, which protect the devices from static electricity damage under all normal handling conditions. Either container is compatible with standard automatic IC handling equipment.

Any device described in this catalog is an AMI Standard Product. However, ROM devices that require mask preparation or programming to the requirements of a particular user, devices that must be tested to other than AMI Quality Assurance standard procedures, or other devices requiring special masks are sold on a negotiated price basis.



Device Number — prefix S, followed by four (or five*) numeric digits that define the basic device type. Versions to the basic device are indicated by an additional alpha or numeric digit as shown in the above examples.

*Organ Circuits

Package Type — a single letter designation which identifies the basic package type. The letters are coded as follows:

P — Plastic package

D — Cerdip package

C — Ceramic (three-layer) package

Microprocessor/Microcomputer Development Support:

Consult your local sales office.

Custom Circuits:

Consult your local sales office.

Military Products:

Parts Numbering Format

Examples
MBC 6802
LBC 68A00
MBL UA-3

X X X NNNNN

NNNNN — Four to seven alpha numerics specifying the basic part number (die type) and including a power/speed selection as applicable. For example, 6802 indicates an 8-bit microprocessor with clock and RAM; 5101L-4 specifies a CMOS 256×4 static RAM with 0.055mW maximum standby power and 650ns maximum access time; and UA-3, a 540 gate CMOS uncommitted logic array.

X — Designates the package and utilizes one of the following letters regardless of the number of leads:

C — Ceramic dual in-line
L — Leadless chip carrier, ceramic, 50 mil pin spacing

X — Designates the screening level:

B — Class B, MIL-STD-883, Method 5004.5
C — Class C, MIL-STD-883, Method 5004.5

X — Designates the operating temperature range and utilizes one of the letters M or L. Definitions:

M — Full military temperature range, −55°C to +125°C
L — Limited military temperature range, −55°C to +85°C

Ordering Information

Please specify part numbers in accordance with the parts numbering format above.

Terms of Sale

1. ACCEPTANCE: THE TERMS OF SALE CONTAINED HEREIN APPLY TO ALL QUOTATIONS MADE AND PURCHASE ORDERS ENTERED INTO BY THE SELLER. SOME OF THE TERMS SET OUT HERE MAY DIFFER FROM THOSE IN BUYER'S PURCHASE ORDER AND SOME MAY BE NEW. THIS ACCEPTANCE IS CONDITIONAL ON BUYER'S ASSENT TO THE TERMS SET OUT HERE IN LIEU OF THOSE IN BUYER'S PURCHASE ORDER. SELLER'S FAILURE TO OBJECT TO PROVISIONS CONTAINED IN ANY COMMUNICATION FROM BUYER SHALL NOT BE DEEMED A WAIVER OF THE PROVISIONS OF THIS ACCEPTANCE. ANY CHANGES IN THE TERMS CONTAINED HEREIN MUST SPECIFICALLY BE AGREED TO IN WRITING BY AN OFFICER OF THE SELLER BEFORE BECOMING BINDING ON EITHER THE SELLER OR THE BUYER. All orders or contracts must be approved and accepted by the Seller at its home office. These terms shall be applicable whether or not they are attached to or enclosed with the products to be sold or sold hereunder. Prices for the items called for hereby are not subject to audit.

2. PAYMENT:

(a) Unless otherwise agreed, all invoices are due and payable thirty (30) days from date of invoice. No discounts are authorized. Shipments, deliveries, and performance of work shall at all times be subject to the approval of the Seller's credit department and the Seller may at any time decline to make any shipments or deliveries or perform any work except upon receipt of payment or upon terms and conditions or security satisfactory to such department.

(b) If, in the judgment of the Seller, the financial condition of the Buyer at any time does not justify continuation of production or shipment on the terms of payment originally specified, the Seller may require full or partial payment in advance and, in the event of the bankruptcy or insolvency of the Buyer or in the event any proceeding is brought by or against the Buyer under the bankruptcy or insolvency laws, the Seller shall be entitled to cancel any order then outstanding and shall receive reimbursement for its cancellation charges.

(c) Each shipment shall be considered a separate and independent transaction, and payment therefor shall be made accordingly. If shipments are delayed by the Buyer, payments shall become due on the date when the Seller is prepared to make shipment. If the work covered by the purchase order is delayed by the Buyer, payments shall be made based on the purchase price and the percentage of completion. Products held for the Buyer shall be at the risk and expense of the Buyer.

3. TAXES: Unless otherwise provided herein, the amount of any present or future sales, revenue, excise or other taxes, fees, or other charges of any nature, imposed by any public authority, (national, state, local or other) applicable to the products covered by this order, or the manufacture or sale thereof, shall be added to the purchase price and shall be paid by the Buyer, or in lieu thereof, the Buyer shall provide the Seller with a tax exemption certificate acceptable to the taxing authority.

4. F.O.B. POINT: All sales are made F.O.B. point of shipment. Seller's title passes to Buyer, and Seller's liability as to delivery ceases upon making delivery of material purchased hereunder to carrier at shipping point, the carrier acting as Buyer's agent. All claims for damages must be filed with the carrier. Shipments will normally be made by Parcel Post, Railway Express, Air Express, or Air Freight. Unless specific instructions from Buyer specify which of the foregoing methods of shipment is to be used, the Seller will exercise his own discretion.

5. DELIVERY: Shipping dates are approximate and are based upon prompt receipt from Buyer of all necessary information. In no event will Seller be liable for any re-procurement costs, nor for delay or non-delivery, due to causes beyond its reasonable control including, but not limited to, acts of God, acts of civil or military authority, priorities, fires, strikes, lockouts, slow-downs, shortages, factory or labor conditions, yield problems, and inability due to causes beyond the Seller's reasonable control to obtain necessary labor, materials, or manufacturing facilities. In the event of any such delay, the date of delivery shall, at the request of the Seller, be deferred for a period equal to the time lost by reason of the delay.

In the event Seller's production is curtailed for any of the above reasons so that Seller cannot deliver the full amount released hereunder, Seller may allocate production deliveries among its various customers then under contract for similar goods. The allocation will be made in a commercially fair and reasonable manner. When allocation has been made, Buyer will be notified of the estimated quota made available.

6. PATENTS: The Buyer shall hold the Seller harmless against any expense or loss resulting from infringement of patents, trademarks, or unfair competition arising from compliance with Buyer's designs, specifications, or instructions. The sale of products by the Seller does not convey any license, by implication, estoppel, or otherwise, under patent claims covering combinations of said products with other devices or elements.

Except as otherwise provided in the preceding paragraph, the Seller shall defend any suit or proceeding brought against the Buyer, so far as based on a claim that any product, or any part thereof, furnished under this contract constitutes an infringement of any patent of the United States, if notified promptly in writing and given authority, information, and assistance (at the Seller's expense) for defense of same, and the Seller shall pay all damages and costs awarded therein against the Buyer. In case said product, or any part thereof, is, in such suit, held to constitute infringement of patent, and the use of said product is enjoined, the Seller shall, at its own expense, either procure for the Buyer the right to continue using said product or part, replace same with non-infringing product, modify it so it becomes non-infringing, or remove said product and refund the purchase price and the transportation and installation costs thereof. In no event shall Seller's total liability to the Buyer under or as a result of compliance with the provisions of this paragraph exceed the aggregate sum paid by the Buyer for the allegedly infringing product. The foregoing states the entire liability of the Seller for patent infringement by the said products or any part thereof. THIS PROVISION IS STATED IN LIEU OF ANY OTHER EXPRESSED, IMPLIED, OR STATUTORY WARRANTY AGAINST INFRINGEMENT AND SHALL BE THE SOLE AND EXCLUSIVE REMEDY FOR PATENT INFRINGEMENT OF ANY KIND.

7. INSPECTION: Unless otherwise specified and agreed upon, the material to be furnished under this order shall be subject to the Seller's standard inspection at the place of manufacture. If it has been agreed upon and specified in this order that Buyer is to inspect or provide for inspection at place of manufacture such inspection shall be so conducted as to not interfere unreasonably with Seller's operations and consequent approval or rejection shall be made before shipment of the material. Notwithstanding the foregoing, if, upon receipt of such material by Buyer, the same shall appear not to conform to the contract, the Buyer shall immediately notify the Seller of such conditions and afford the Seller a reasonable opportunity to inspect the material. No material shall be returned without Seller's consent. Seller's Return Material Authorization form must accompany such returned material.

8. LIMITED WARRANTY: The Seller warrants that the products to be delivered under this purchase order will be free from defects in material and workmanship under normal use and service. Seller's obligations under this Warranty are limited to replacing or repairing or giving credit for, at its option, at its factory, any of said products which shall, within one (1) year after shipment, be returned to the Seller's factory of origin, transportation charges prepaid, and which are, after examination, disclosed to the Seller's satisfaction to be thus defective. THIS WARRANTY IS EXPRESSED IN LIEU OF ALL OTHER WARRANTIES EXPRESSED, STATUTORY, OR IMPLIED, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, AND OF ALL OTHER OBLIGATIONS OR LIABILITIES ON THE SELLER'S PART, AND IT NEITHER ASSUMES NOR AUTHORIZES ANY OTHER PERSON TO ASSUME FOR THE SELLER ANY OTHER LIABILITIES IN CONNECTION WITH THE SALE OF THE SAID ARTICLES. This Warranty shall not apply to any of such products which shall have been repaired or altered, except by the Seller, or which shall have been subjected to misuse, negligence, or accident. The aforementioned provisions do not extend the original warranty period of any product which has either been repaired or replaced by Seller.

It is understood that if this order calls for the delivery of semiconductor devices which are not finished and fully encapsulated, that no warranty, statutory, expressed or implied, including the implied warranty of merchantability and fitness for a particular purpose, shall apply. All such devices are sold as is where is.

9. PRODUCTS NOT WARRANTED BY SELLER: The second paragraph of Paragraph 6, Patents, and Paragraph 8, Limited Warranty, above apply only to integrated circuits of Seller's own manufacture. IN THE CASE OF PRODUCTS OTHER THAN INTEGRATED CIRCUITS OF SELLER'S OWN MANUFACTURE, SELLER MAKES NO WARRANTIES EXPRESSED, STATUTORY OR IMPLIED INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY, FREEDOM FROM PATENT INDEMNITY AND FITNESS FOR A PARTICULAR PURPOSE. Such products may be warranted by the original manufacturer of such products. For further information regarding the possible warranty of such products contact Seller.

10. PRICE ADJUSTMENTS: Seller's unit prices are based on certain material costs. These materials include, among other things, gold packages and silicon. Adjustments shall be as follows:

(a) Gold. The price at the time of shipment shall be adjusted for increases in the cost of gold in accordance with Seller's current Gold Price Adjustment List. This adjustment will be shown as a separate line item on each invoice.

(b) Other Materials. In the event of significant increases in other materials, Seller reserves the right to renegotiate the unit prices. If the parties cannot agree on such increase, then neither party shall have any further obligations with regard to the delivery or purchase of any units not then scheduled for production.

11. VARIATION IN QUANTITY: If this order calls for a product not listed in Seller's current catalog, or for a product which is specially programmed for Buyer, it is agreed that Seller may ship a quantity which is five percent (5%) more or less than the ordered quantity and that such quantity shipped will be accepted and paid for in full satisfaction of each party's obligation hereunder for the quantity order.

12. CONSEQUENTIAL DAMAGES: In no event shall Seller be liable for special, incidental or consequential damages.

13. GENERAL:

(a) The validity, performance and construction of these terms and all sales hereunder shall be governed by the laws of the State of California.

(b) The Seller represents that with respect to the production of articles and/or performance of the services covered by this order it will fully comply with all requirements of the Fair Labor Standards Act of 1938, as amended, Williams-Steiger Occupational Safety and Health Act of 1970, Executive Orders 11375 and 11246, Section 202 and 204.

(c) The Buyer may not unilaterally make changes in the drawings, designs or specifications for the items to be furnished hereunder without Seller's prior consent.

(d) Except to the extent provided in Paragraph 14, below, this order is not subject to cancellation or termination for convenience.

(e) If Buyer is in breach of its obligations under this order, Buyer shall remain liable for all unpaid charges and sums due to Seller and will reimburse Seller for all damages suffered or incurred by Seller as a result of Buyer's breach. The remedies provided herein shall be in addition to all other legal means and remedies available to Seller.

14. GOVERNMENT CONTRACT PROVISIONS: If Buyer's original purchase order indicates by contract number, that it is placed under a government contract, only the following provisions of the current Defense Acquisition Regulations are applicable in accordance with the terms thereof, with an appropriate substitution of parties, as the case may be - i.e., "Contracting Officer" shall mean "Buyer", "Contractor" shall mean "Seller", and the term "Contract" shall mean this order:

7-103.1, Definitions; 7-103.3, Extras; 7-103.4, Variation in Quantity; 7-103.8, Assignment of Claims; 7-103.9, Additional Bond Security; 7-103.13, Renegotiation; 7-103.15, Rhodesia and Certain Communist Areas; 7-103.16, Contract Work Hours and Safety Standards Act - Overtime Compensation; 7-103.17, Walsh-Healey Public Contracts Act; 7-103.18, Equal Opportunity Clause; 7-103.19, Officials Not to Benefit; 7-103.20, Covenant Against Contingent Fees; 7-103.21, Termination for Convenience of the Government (only to the extent that Buyer's contract is terminated for the convenience of the government); 7-103.22, Authorization and Consent; 7-103.23, Notice and Assistance Regarding Patent Infringement; 7-103.24, Responsibility for Inspection; 7-103.25, Commercial Bills of Lading Covering Shipments Under FOB Origin Contracts; 7-103.27, Listing of Employment Openings; 7-104.4, Notice to the Government of Labor Disputes; 7-104.11, Excess Profit; 7-104.15, Examination of Records by Comptroller General; 7-104.20, Utilization of Labor Surplus Area Concerns.

Worldwide Sales Offices

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TWX: 910-341-7668

Santa Clara, California
Tel: (408) 738-4151
TWX: 910-338-2022

Arvada, Colorado
Tel: (303) 420-1236

Battle Ground, Washington
Tel: (206) 687-3101

CENTRAL AREA

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Tel: (312) 437-6496
TWX: 910-222-2853

Noblesville, Indiana
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TWX: 810-260-1753

Wayne, Michigan
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TWX: 810-242-2919

Richardson, Texas
Tel: (214) 231-5721
(214) 231-5285
TWX: 910-867-4766

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Altamonte Springs, Florida
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TWX: 810-853-0269

Lexington, Massachusetts
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TWX: 710-326-1174

Monsey, New York
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TWX: 710-577-2827

Ambler, Pennsylvania
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TWX: 510-661-3878

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Tel: (793) 37852
TLX: 851-449349

France
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Tel: (01) 374 00 90
TLX: 842-670500

Italy
Milano
Tel: 29-37-45 or 29-24-19
TLX: 311644

Japan
Minato-ku, Tokyo
Tel: 586-8131
TLX: 781-242-2180 AMI J

West Germany
Munich
Tel: (89) 483081
TLX: 841-522743
Rapifax: (89) 486591

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Hecht, Henschen & Assoc., Inc.
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TWX: 910-951-0635

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Tel: (408) 996-9889
TWX: 910-338-2018
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Ed Landa Co.
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TWX: 910-342-6343
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Hadden Associates
Tel: (714) 565-9445
TWX: 910-335-2057

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TWX: 053-3198
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TWX: 610-491-3728
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Vitel Electronics
Tel: 514-331-7393
TWX: 610-421-3124
Vancouver, B.C.
Vitel Electronics
Tel: (604) 438-6121
TWX: 610-953-4925

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TLX: 956050

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Rep, Inc.
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TWX: 810-766-0822

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Elk Grove Village
Oasis Sales
Tel: (312) 640-1850
TWX: 910-222-2170

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Comstrand, Inc.
Tel: (319) 377-1575

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Minneapolis
Comstrand, Inc.
Tel: (612) 788-9234
TWX: 910-576-0924

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Nashua
ENJAY Electronics
Tel: (603) 883-9380

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Advanced Components
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Advanced Components
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Advanced Components
Tel: (716) 554-7017
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Advanced Components
Tel: (716) 889-1429
W. Babylon
Astrorep
Tel: (516) 422-2500;
(201) 624-4408; (203) 324-4208
TWX: 510-227-8114

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Raleigh
Rep, Inc.
Tel: (919) 851-3007

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TWX: 810-459-1647
Shaker Heights
S.A.I. Marketing
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TWX: 810-421-8289
Zanesville
S.A.I. Marketing
Tel: (614) 454-8942

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Oklahoma City
Ammon & Rizos
Tel: (405) 942-2552

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Austin
Ammon & Rizos
Tel: (512) 454-5131
TWX: 910-374-1369
Dallas
Ammon & Rizos
Tel: (214) 233-5591
TWX: 910-860-5137
Houston
Ammon & Rizos
Tel: (713) 781-6240
TWX: 910-881-6382

TENNESSEE
Jefferson City
Rep, Inc.
Tel: (615) 475-4105
TWX: 810-570-4203

WASHINGTON
Bellevue
SD-R^2 Products & Sales
Tel: (206) 747-9424 or (206) 624-2621
TWX: 810-443-2483

WISCONSIN
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Oasis Sales
Tel: (414) 782-6660

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Kierulff Electronics (602) 624-9986

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Schweber Electronics (714) 556-3880
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Kierulff Electronics (213) 725-0325
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Kierulff Electronics (415) 968-6292
San Diego
Anthem Electronics (714) 279-5200
Arrow Electronics (714) 565-4800
Kierulff Electronics (714) 278-2112
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Anthem Electronics (408) 946-8000
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Schweber Electronics (408) 496-0200
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Arrow Electronics (408) 745-6600
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Kierulff (714) 731-5711

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Arrow Electronics (303) 758-2100
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Arrow Electronics (612) 830-1800

MISSOURI
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Arrow Electronics (314) 567-6888

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Arrow Electronics (215) 928-1800
Saddlebrook
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or (516) 293-6363
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Arrow Electronics (516) 231-1000
Liverpool
Arrow Electronics (315) 652-1000
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Arrow Electronics (716) 275-0300
Schweber Electronics (716) 424-2222
Westbury
Schweber Electronics (516) 334-7474

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Arrow Electronics (216) 248-3990

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Schweber Electronics (215) 441-0600
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Arrow Electronics (713) 491-4100

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Kierulff Electronics (206) 575-4420
Tukwila
Arrow Electronics (206) 575-0907

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Arrow Electronics (414) 764-6600
Waukesha
Kierulff Electronics (414) 784-8160

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Ontario
Downsview
Cesco Electronics, Ltd. (416) 661-0220
Future Electronics, Inc. (416) 663-5563
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Future Electronics, Inc. (613) 820-8313
Quebec
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Cesco Electronics, Ltd. (514) 735-5511
Future Electronics, Inc. (514) 731-7441
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Cesco Electronics, Ltd. (418) 687-4231

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YEL S.R.L.
Buenos Aires
Tel: 46 2211
TLX: 18605 YEL Arg

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Rifa Pty. Ltd.
Preston, Victoria
Tel: (03) 480 1211
TLX: AA31001

AUSTRIA
PCS Handelsgescellschaft M.B.H.
A-1100 Vienna
Tel: (222) 62 71 97
TLX: 0131208

BELGIUM
Betea Automation S.A./N.V.
B-1140 Brussels
Tel: (02) 7368050
TLX: 23188

BRAZIL
Datatronix Electronica Ltda.
Sao Paulo
Tel: 209-0134
TLX: 391-1131889 DAEL BR

DENMARK
Ditz Schweitzer A/S
Clostrup
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TWX: 33257

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Quarndon Electronics Ltd.
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TLX: 37163
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Carroll House
West Drayton Mtddx
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TLX: 21958
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Werneth, Oldham
Greater Manchester
Tel: (061) 652-6316
TWX: 668250
VSI Electronics (UK) Ltd.
Harlow, Essex
Tel: (0279) 2935477
TWX: 81387

FINLAND
OY Atomica AB
Espoo
Tel: (080) 423533
TLX: 12-1080

FRANCE
Produits Electronique
Professionals S.A.R.L. (P.E.P.)
Montrouge
Tel: (01) 7353320
TLX: 204534
Tekelec Airtronic
Sevres
Tel: (01) 534-75-35
TLX: 204552

HONGKONG
Electrocon Products Ltd.
Kowloon
Tel: 3-679557 or 3-679269
TLX: 84996 TGRAF HX

ITALY
C.I.D. s.r.l.
Roma
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TWX: 680474
Mesa SpA
Milano
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TLX: 334022

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Tokyo
Logic House, Inc.
Tokyo
Logic Systems International, Inc. Ltd.
Tokyo
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Matsushita Electric Trading
Company, Ltd.
Osaka
Tel: (06) 204-5510
TLX: 781-63417
Taiyo Electric Co.
Tokyo
Tel: (03) 379-2926
TLX: 24904

KOREA
Kwang Won Park Assoc.
c/o KMI Korea
Inchon
Tel: Inchon-56412
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Col Napoles
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Rotterdam
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Singapore
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TLX: RS 26283 DYNAMA

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Transvaal
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TLX: 51508

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Spanga
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TLX: 52042

TAIWAN
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Taipai
Tel: Taipai (02) 536-4057
TLX: TAIPEI 27271 COMMOTEK

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Berlin
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TLX: 185327

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TLX: 725-5638

Gleichmannn & Co. Electronics GmbH
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TWX: 8518714

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